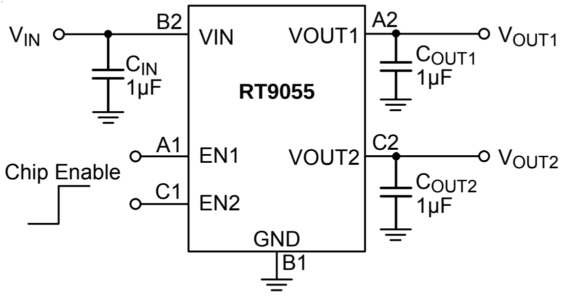
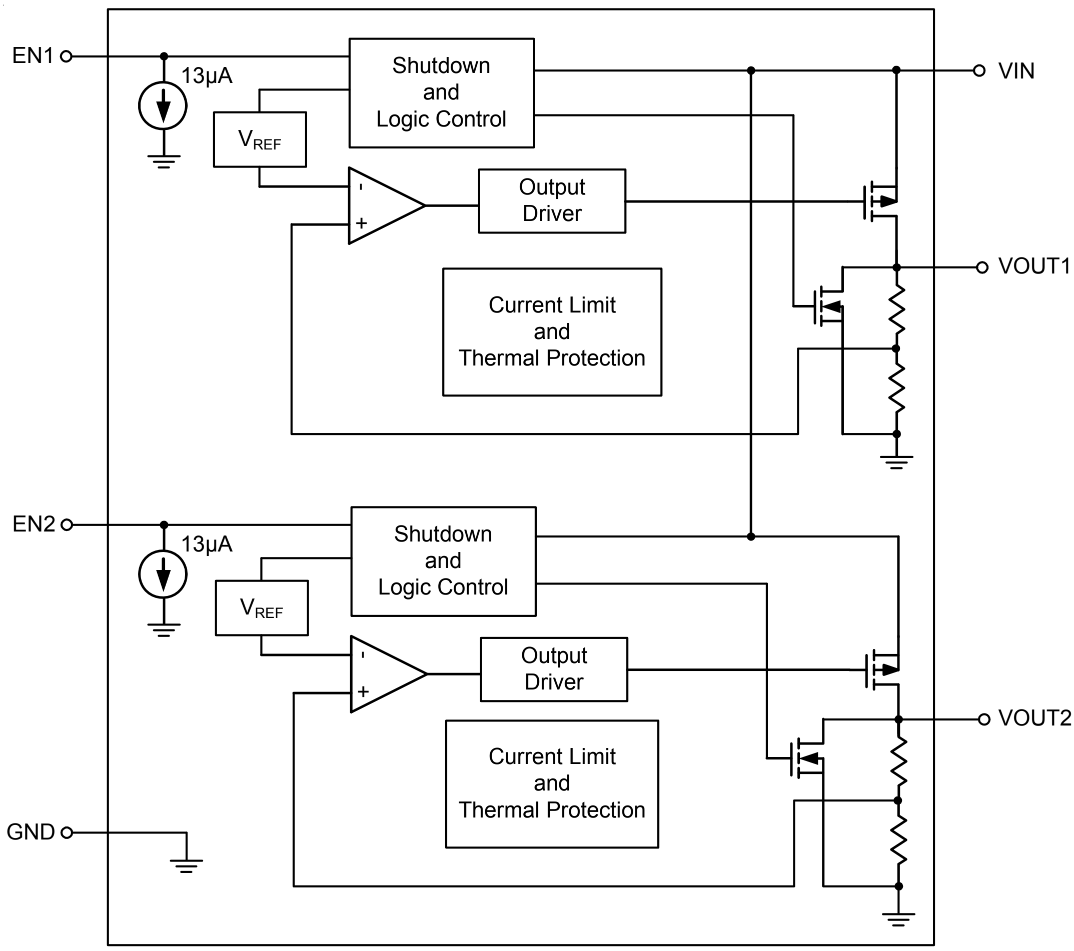
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	EN1	LDO1 Enable (Active High).
A2	VOUT1	LDO1 Output Voltage.
B1	GND	Ground.
B2	VIN	Supply Input.
C1	EN2	LDO2 Enable (Active High).
C2	VOUT2	LDO2 Output Voltage.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN -- –0.3V to 6V
- Other I/O Pins Voltages -- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-6B 0.8x1.2 -- 0.670W
- Package Thermal Resistance (Note 2)
  WL-CSP-6B 0.8x1.2, θ_{JA} -- 148°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) -- 2kV
  MM (Machine Model) -- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN -- 1.5V to 5.5V
- Junction Temperature Range -- –40°C to 125°C
- Ambient Temperature Range -- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} = 1μF, T_A = –40°C to 85°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply							
Dropout Voltage (Note 5)		V_{DROP}	V_{OUT} = 1.2V to 1.4V, I_{OUT} = 300mA	50	--	550	mV
			V_{OUT} = 1.5V to 2.4V, I_{OUT} = 300mA	40	--	400	
			V_{OUT} = 2.5V to 3.5V, I_{OUT} = 300mA	20	--	300	
Output Voltage Range		V_{OUT}		0.9	--	3.5	V
V_{OUT} Accuracy		ΔV	I_{OUT} = 1mA to 300mA	–2	--	2	%
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1) to 5.5V, I_{OUT} = 1mA	–2	--	2	%
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 300mA	–1.5	--	1.5	%
Current Limit		I_{LIM}	R_{LOAD} = 0Ω	350	600	--	mA
Quiescent Current		I_Q	V_{EN} > 1.5V	--	58	--	μA
Shutdown Current		I_{SHDN}	V_{EN} < 0.4V	--	--	1	μA
EN Input Threshold Voltage	Logic-High	V_{IH}	V_{IN} = 2.5V to 5.5V, Power On	1.2	--	--	V
	Logic-Low	V_{IL}	V_{IN} = 2.5V to 5.5V, Shutdown	--	--	0.4	
V_{OUT} Discharge Resistance in Shutdown (Note 6)			V_{IN} = 5V, EN1 = EN2 = GND	--	3	--	kΩ
EN Pull Low Current		I_{EN}		8	13	18	μA
Thermal Shutdown		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	40	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Rejection Ratio	PSRR	f = 100Hz, V_{IN} = V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	70	--	dB
		f = 1kHz, V_{IN} = V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	70	--	
		f = 10kHz, V_{IN} = V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	70	--	
		f = 100kHz, V_{IN} =V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	54	--	
		f = 200kHz, V_{IN} = V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	45	--	
		f = 300kHz, V_{IN} = V_{OUT} + 1V, C_{OUT} = 2.2μF, I_{LOAD} = 50mA	--	38	--	
Output Voltage Noise		C_{OUT1} = C_{OUT2} = 10μF, 10Hz to100kHz, I_{OUT1} = I_{OUT2} = 1mA	--	100	--	μV_{RMS}

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. The CSP balls connect directly to the internal GND copper plane by 2 vias, the via diameter is about 1mm.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

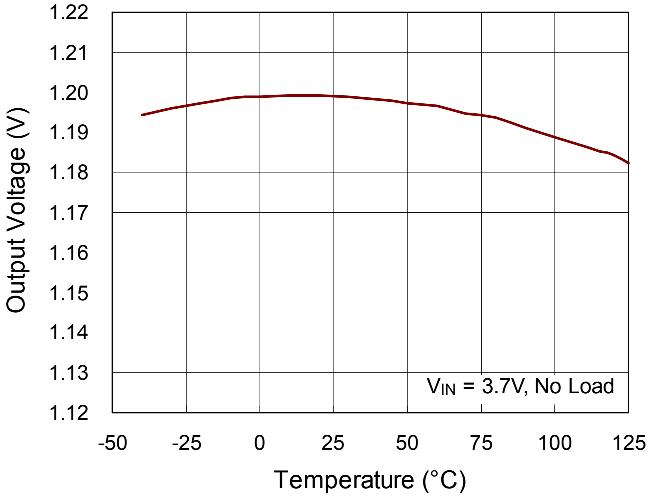
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The dropout voltage is defined as V_{IN} – V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ – 100mV.

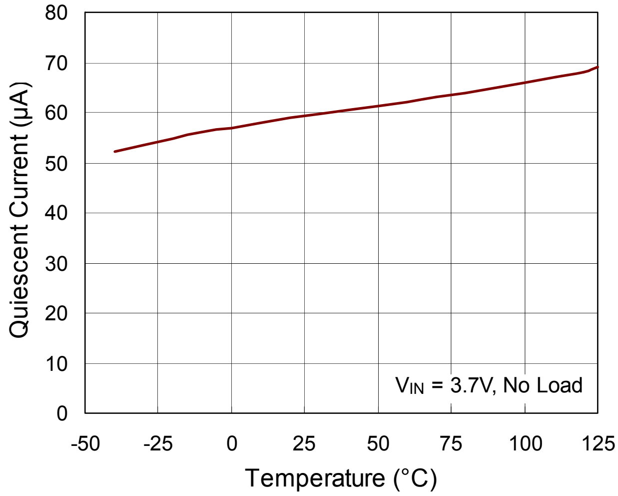
Note 6. It is guaranteed by design.

Typical Operating Characteristics

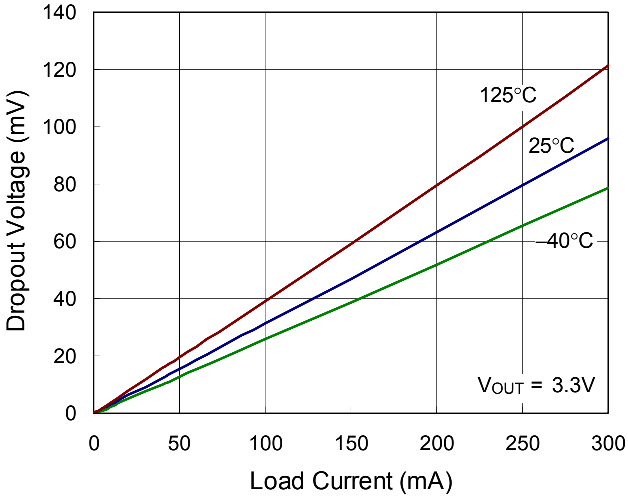
Output Voltage vs. Temperature



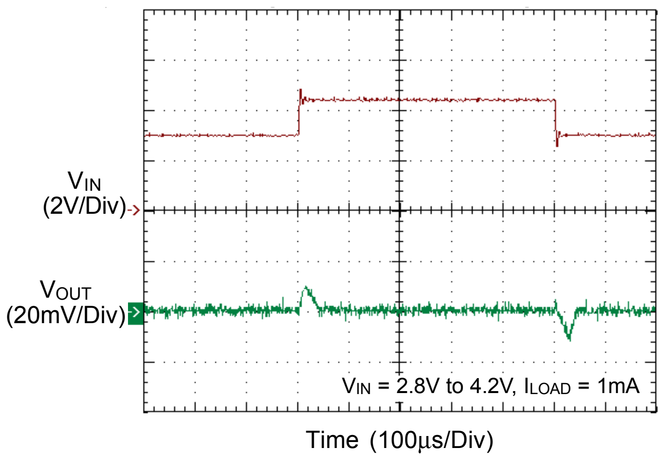
Quiescent Current vs. Temperature



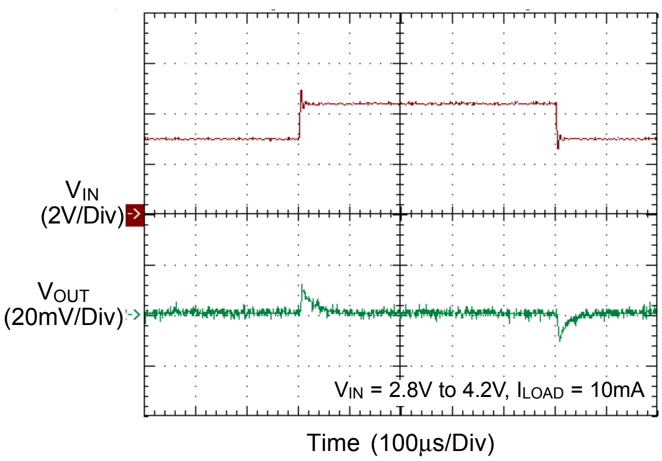
Dropout Voltage vs. Load Current



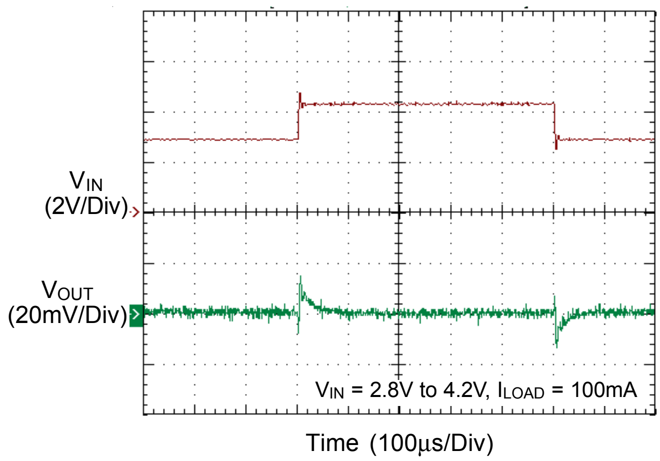
Line Transient Response



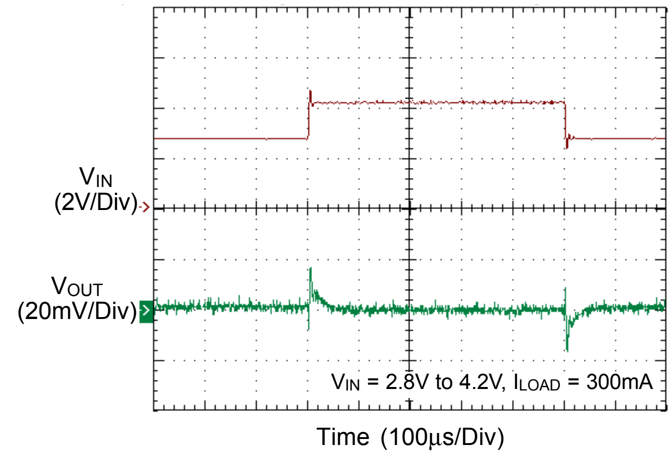
Line Transient Response



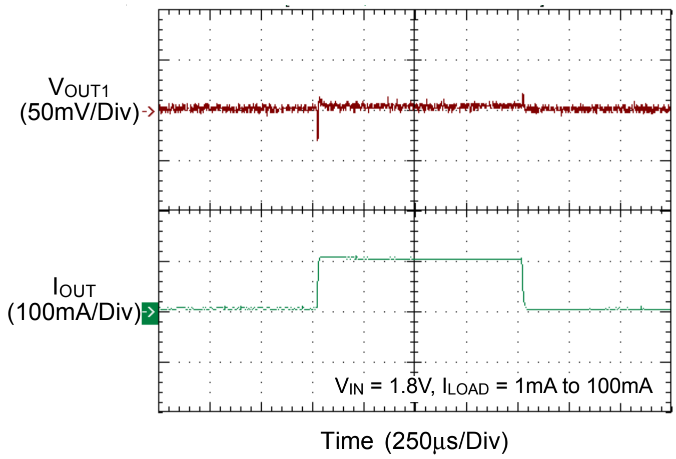
Line Transient Response



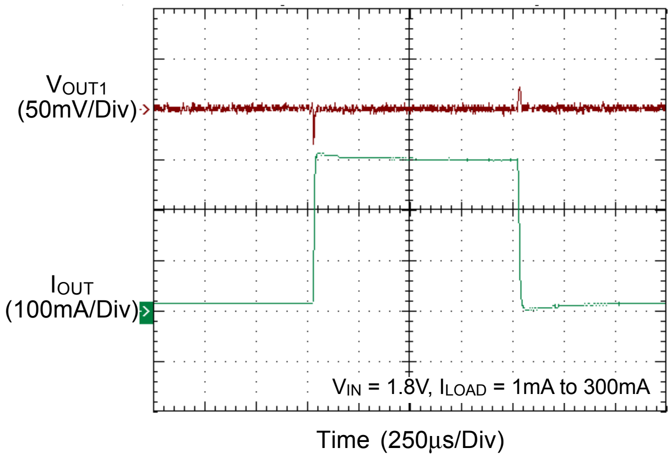
Line Transient Response



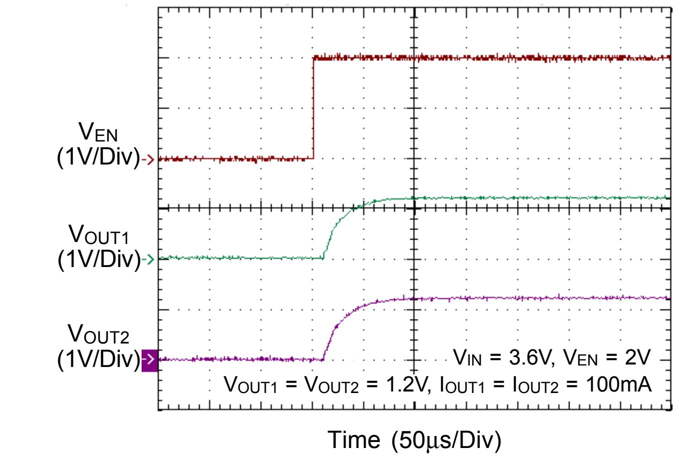
Load Transient Response



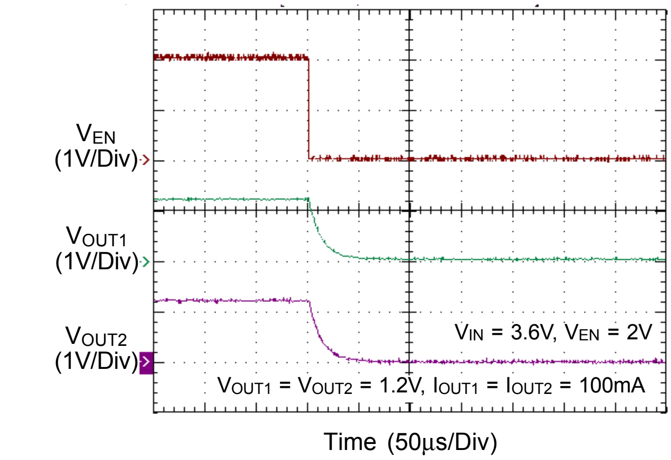
Load Transient Response



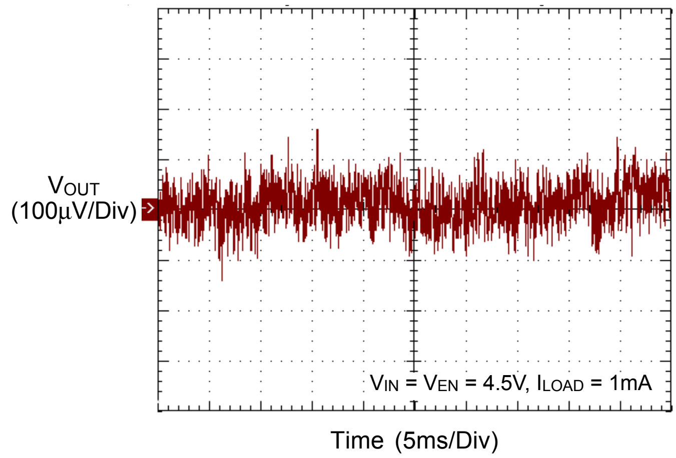
Power On from EN



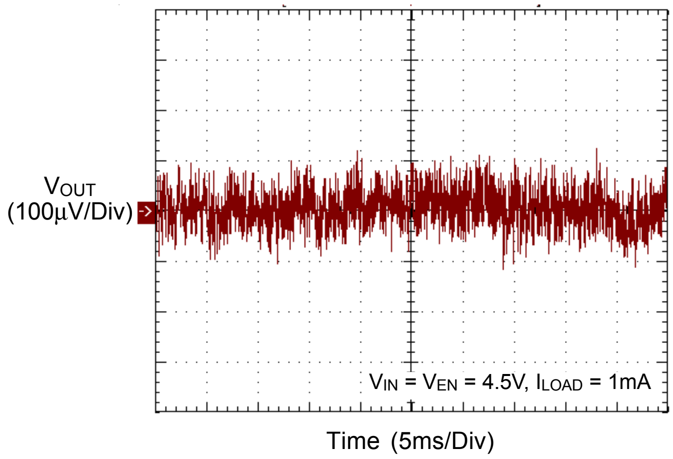
Power Off from EN



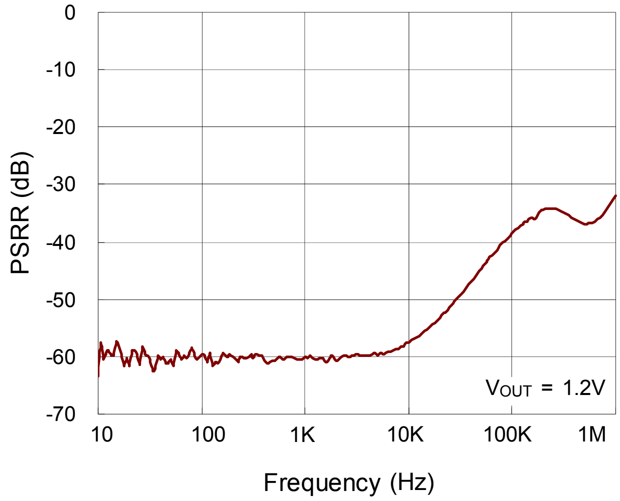
VOUT1 Noise



VOUT2 Noise



PSRR



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9055 must be carefully selected for regulator stability and performance. Using a capacitor whose value is >1μF on the RT9055 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9055 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the RT9055 output ensures stability. The RT9055 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9055 and returned to a clean analog ground.

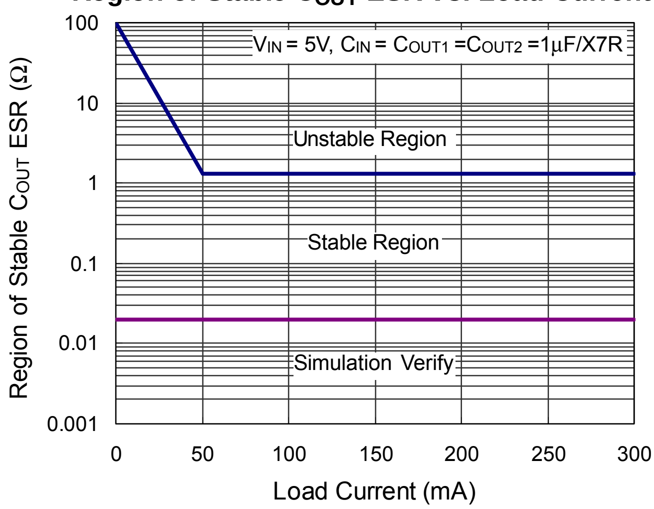


Figure 1. Stable C_{OUT} ESR Range

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. For WL-CSP-6B 0.8x1.2 package, the thermal resistance, θ_{JA}, is 148°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (148°C/W) = 0.670W for WL-CSP-6B 0.8x1.2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J\,(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

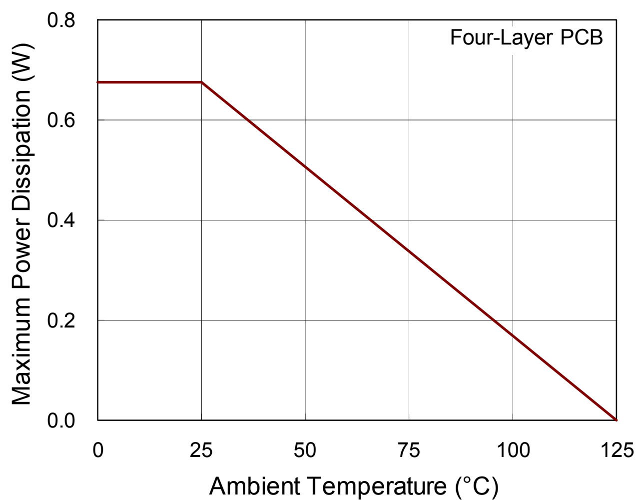
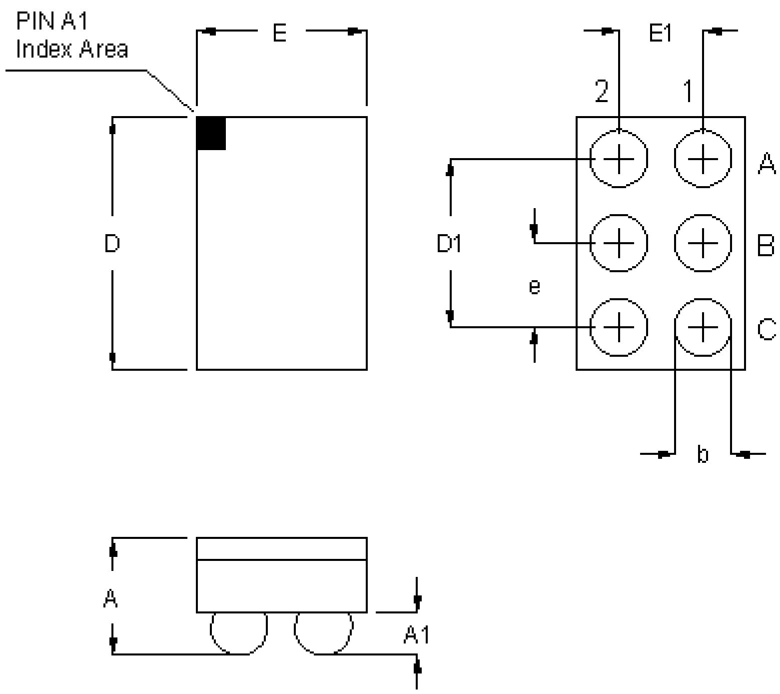


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.150	1.250	0.045	0.049
D1	0.800		0.031	
E	0.750	0.850	0.030	0.033
E1	0.400		0.016	
e	0.400		0.016	

6B WL-CSP 0.8x1.2 Package (BSC)

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789