Typical Application Circuit

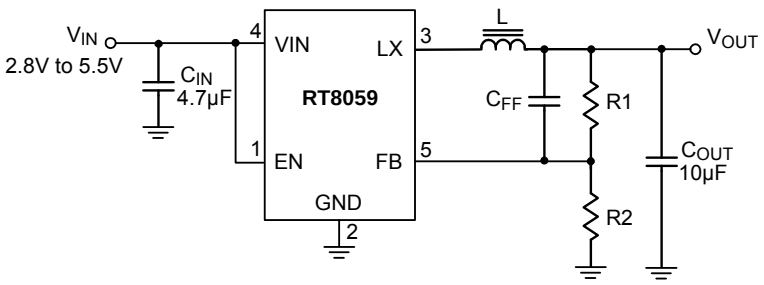


Table 1. Suggested Component Values

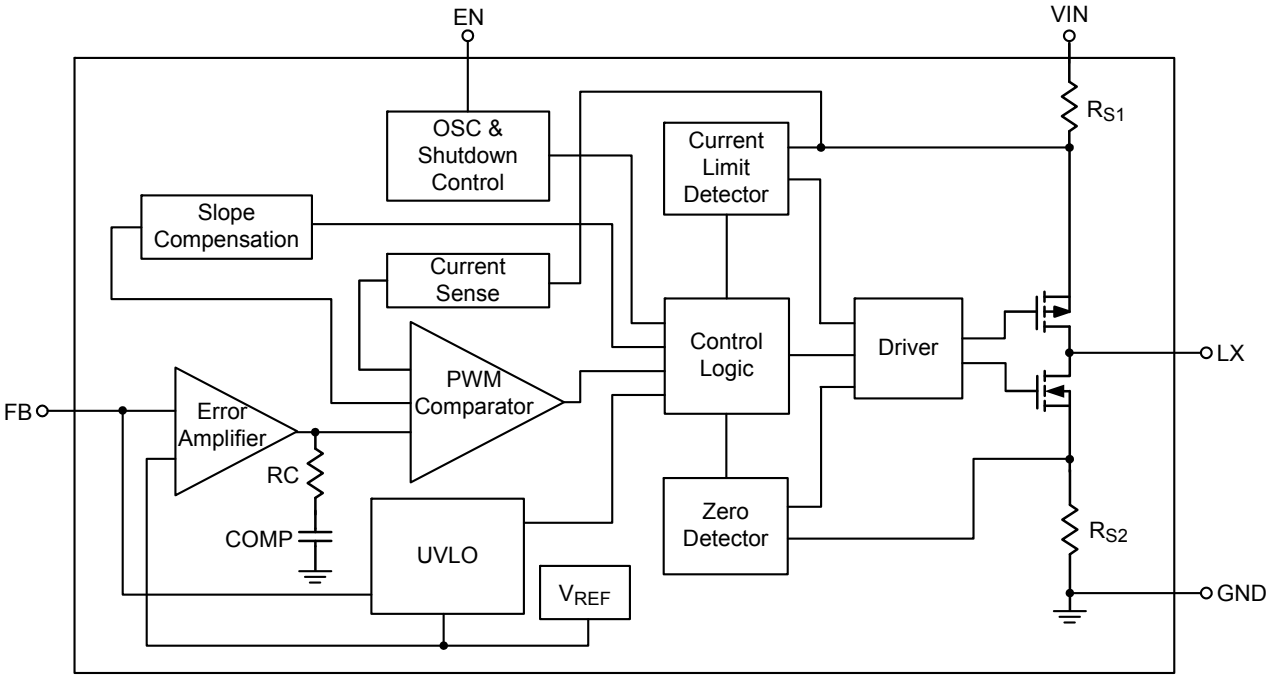
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF) X5R 16V 0805
1	38.3	56.2	22 to 39	1.5	10
1.2	56	56	15 to 39	1.5	10
1.8	113	56.2	0 to 8.2	2.2	10
2.5	178	56	0 to 12	2.2	10
3.3	249	54.9	0 to 8.2	2.2	10

Note : All the input and output capacitors are the suggusted values, refering to the effective capacitances, subject to any de-rating effect, like a DC Bias.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High). Do not leave the EN pin floating.
2	GND	Ground.
3	LX	Switch Node.
4	VIN	Power Input.
5	FB	Feedback Input Pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- 6.5V
- LX to GND ---------- –0.3V to (V_{IN} + 0.3V)
  < 30ns ---------- –5V to 7.5V
- EN, FB to GND ---------- V_{IN} + 0.6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-5 ---------- 0.392W
- Package Thermal Resistance (Note 2)
  TSOT-23-5, θ_{JA} ---------- 255°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%	--	78	--	µA
Shutdown Current		I_{SHDN}	EN = GND	--	0.1	1	µA
Reference Voltage		V_{REF}		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}	(Note 5)	V_{REF}	--	V_{IN} – 0.2	V
Adjustable Output Voltage Accuracy		ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V, 0A < I_{OUT} < 1A, (Note 6)	–3	--	3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}	–50	--	50	nA
P-MOSFET R_{ON}		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	--	0.28	--	Ω
N-MOSFET R_{ON}		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	--	0.25	--	
P-Channel Current Limit		I_{LM_P}	V_{IN} = 2.8V to 5.5V	--	1.5	--	A
EN Input Threshold Voltage	Logic-High	V_{IH}	V_{IN} = 2.8V to 5.5V	1.5	--	--	V
	Logic-Low	V_{IL}	V_{IN} = 2.8V to 5.5V	--	--	0.4	
Under Voltage Lockout Threshold		V_{UVLO}		--	2.3	--	V
Under Voltage Lockout Hysteresis		ΔV_{UVLO}		--	0.2	--	V
Oscillator Frequency		f_{OSC}	I_{OUT} = 100mA	1.2	1.5	1.8	MHz
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Max. Duty Cycle		D_{MAX}		100	--	--	%

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

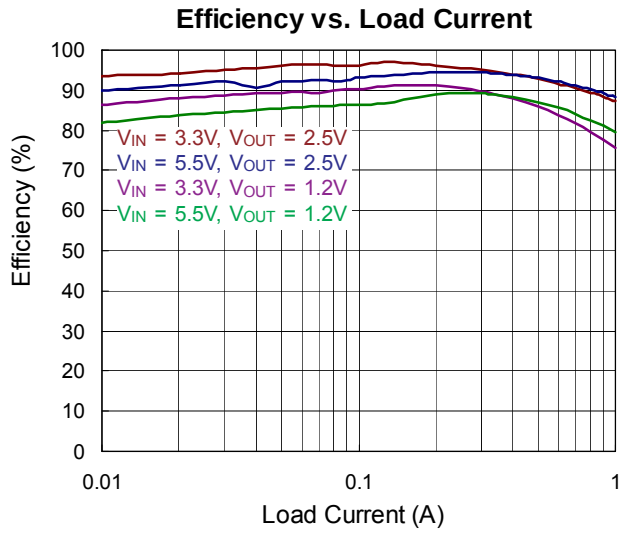
Note 3. Devices are ESD sensitive. Handling precaution recommended.

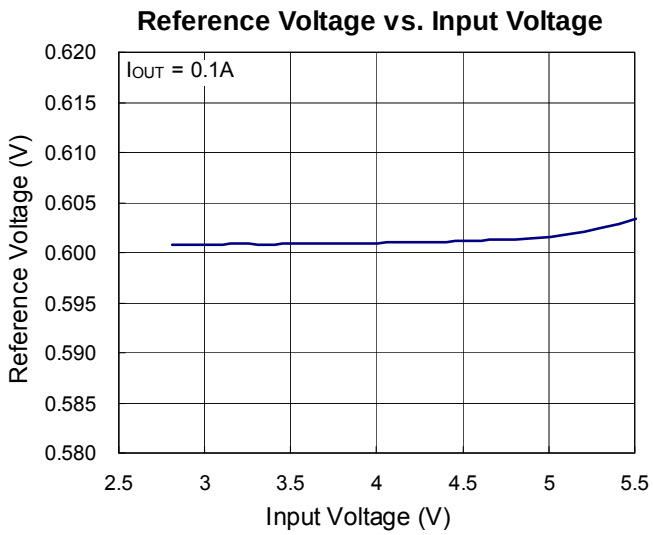
Note 4. The device is not guaranteed to function outside its operating conditions.

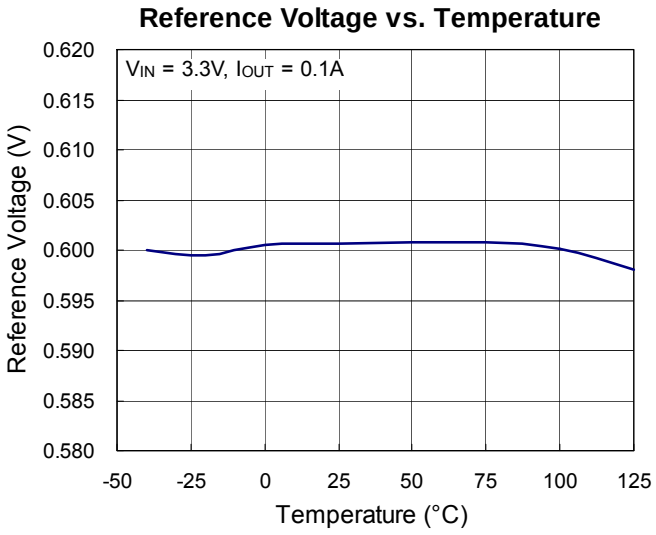
Note 5. Guaranteed by design.

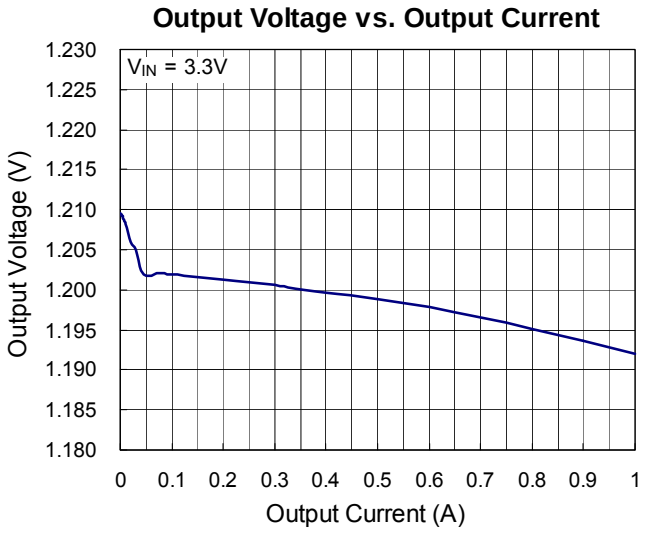
Note 6. $\Delta V = I_{OUT} \times R_{DS(ON)}$

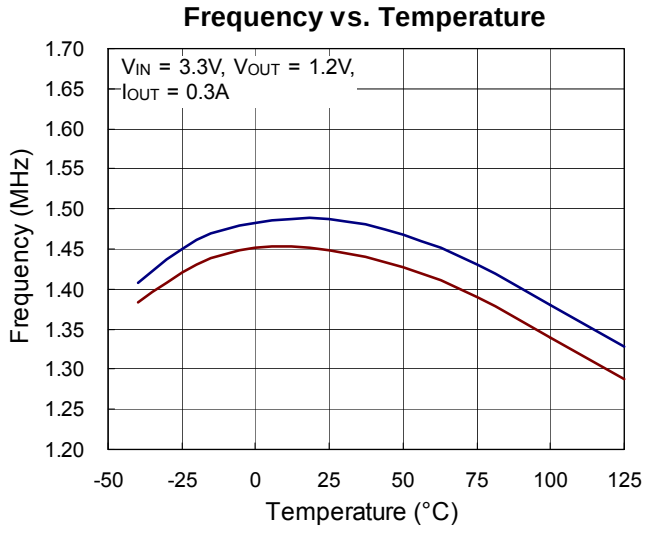
Typical Operating Characteristics

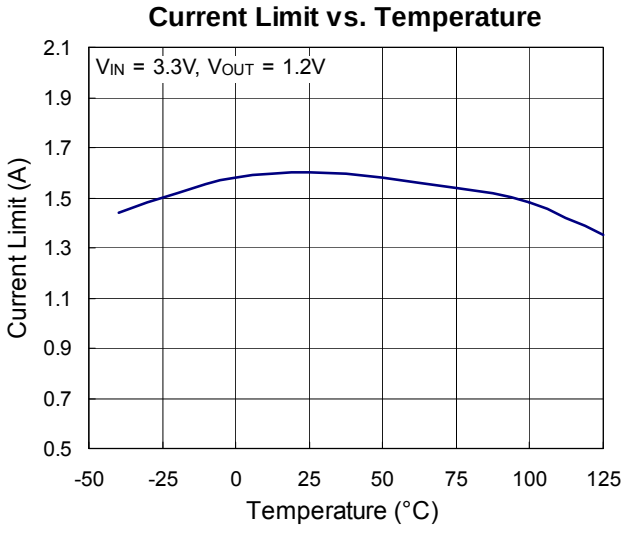




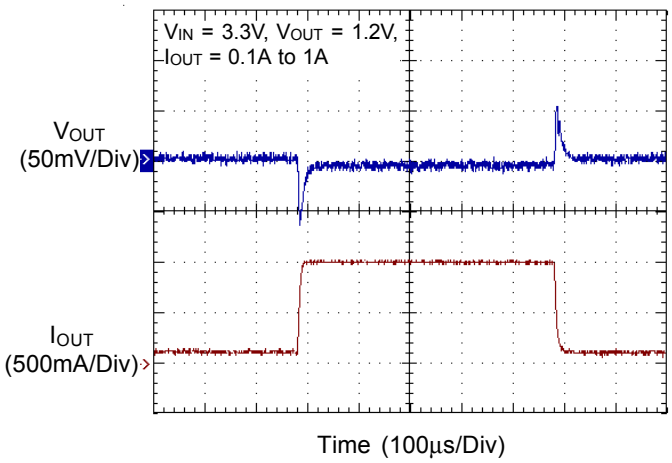




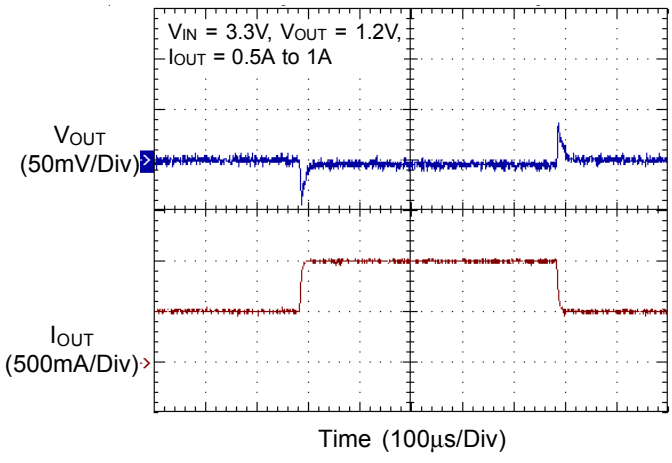




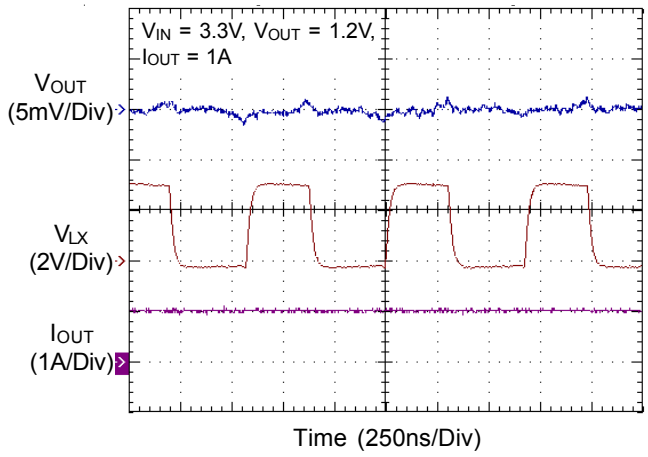
Load Transient Response



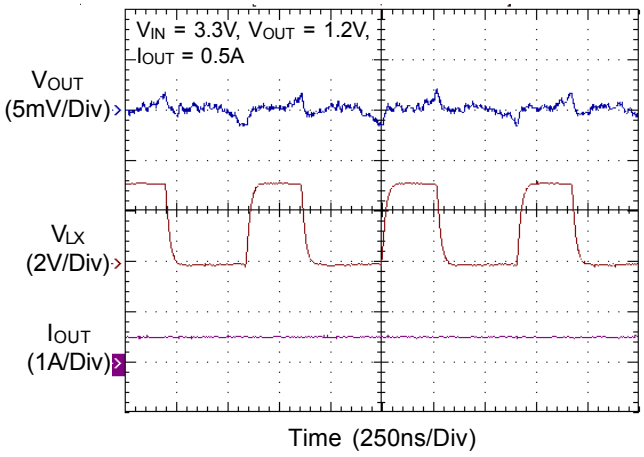
Load Transient Response



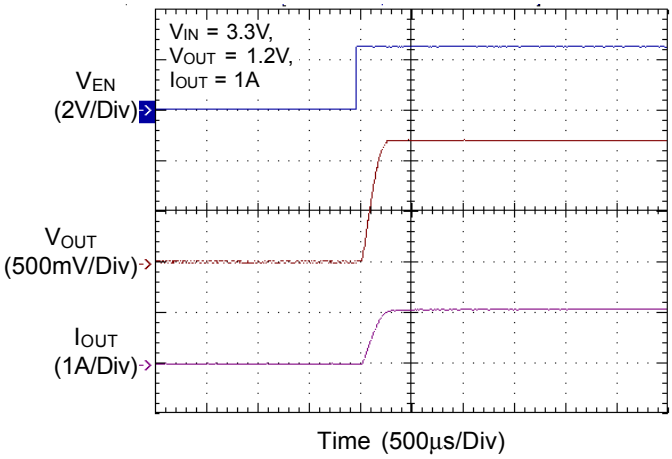
Switching



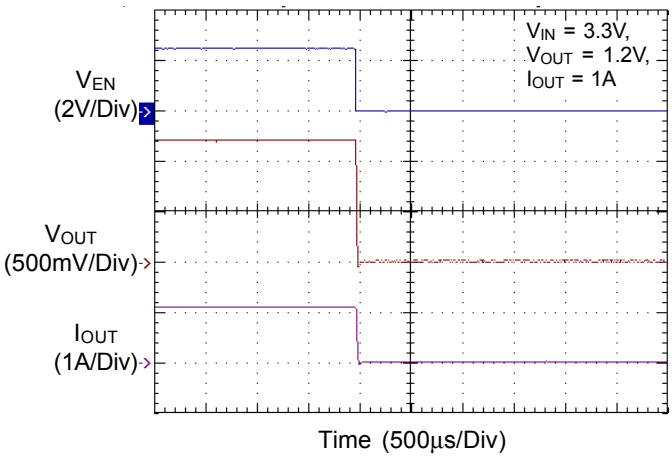
Switching



Power On from EN



Power Off from EN



Applications Information

The basic RT8059 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta IL(MAX)}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor can be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore, results in higher copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not result in much difference. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

where f is the switching frequency and ΔI_L is the inductor ripple current.

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Setting

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

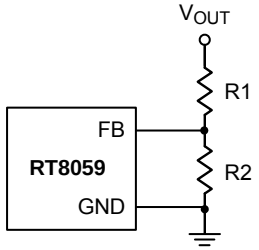


Figure 1. Setting Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}(1+\frac{R1}{R2})$$

where V_{REF} is the internal reference voltage (0.6V typ.)

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8059, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSOT-23-5 packages, the thermal resistance, θ_{JA}, is 255°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (255°C/W) = 0.392W for TSOT-23-5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8059 package, the derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

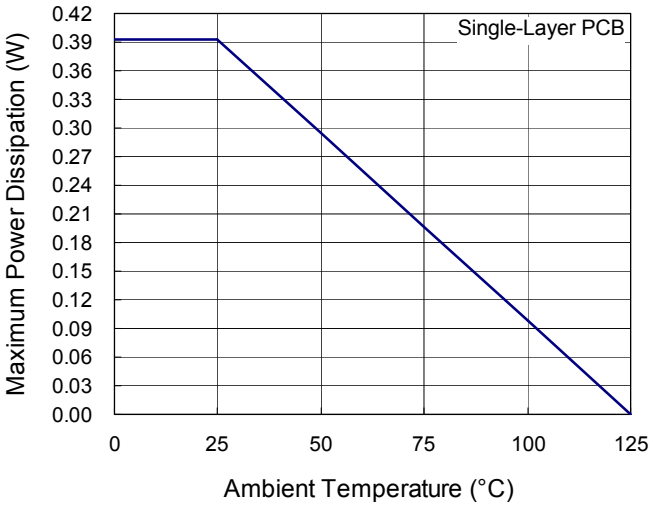


Figure 2. Derating Curves for RT8059 Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8059.

- Keep the trace of the main current paths as short and wide as possible.
- Place the input capacitor as close as possible to the device pins (VIN and GND).
- LX node experiences high frequency voltage swings and should be kept in a small area. Keep analog components away from the LX node to prevent stray capacitive noise pick-up.
- Place the feedback components as close as possible to the FB pin.
- GND and Exposed Pad must be connected to a strong ground plane for heat sinking and noise protection.

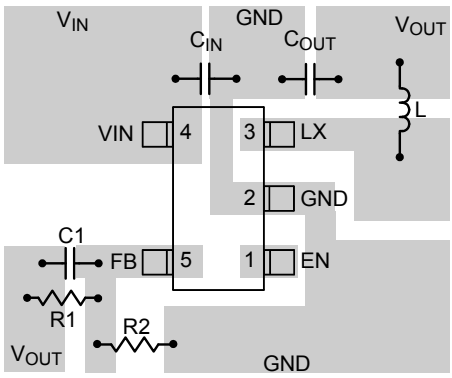
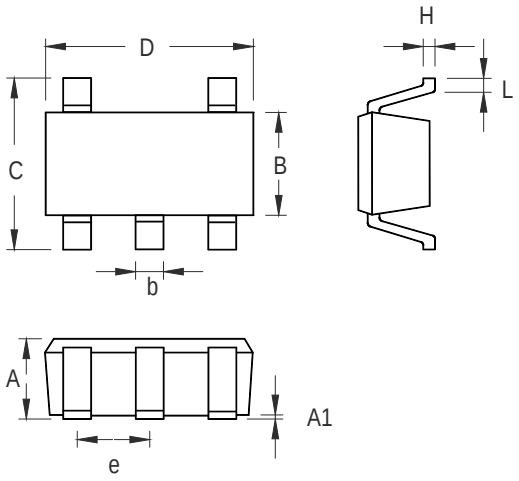


Figure 3. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package

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