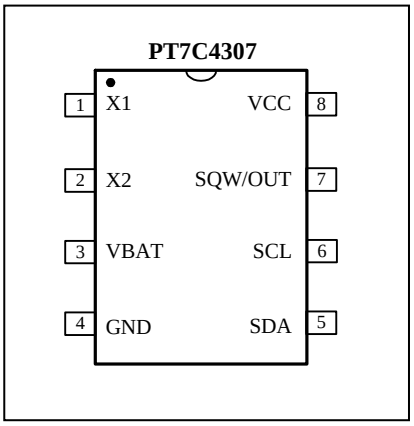
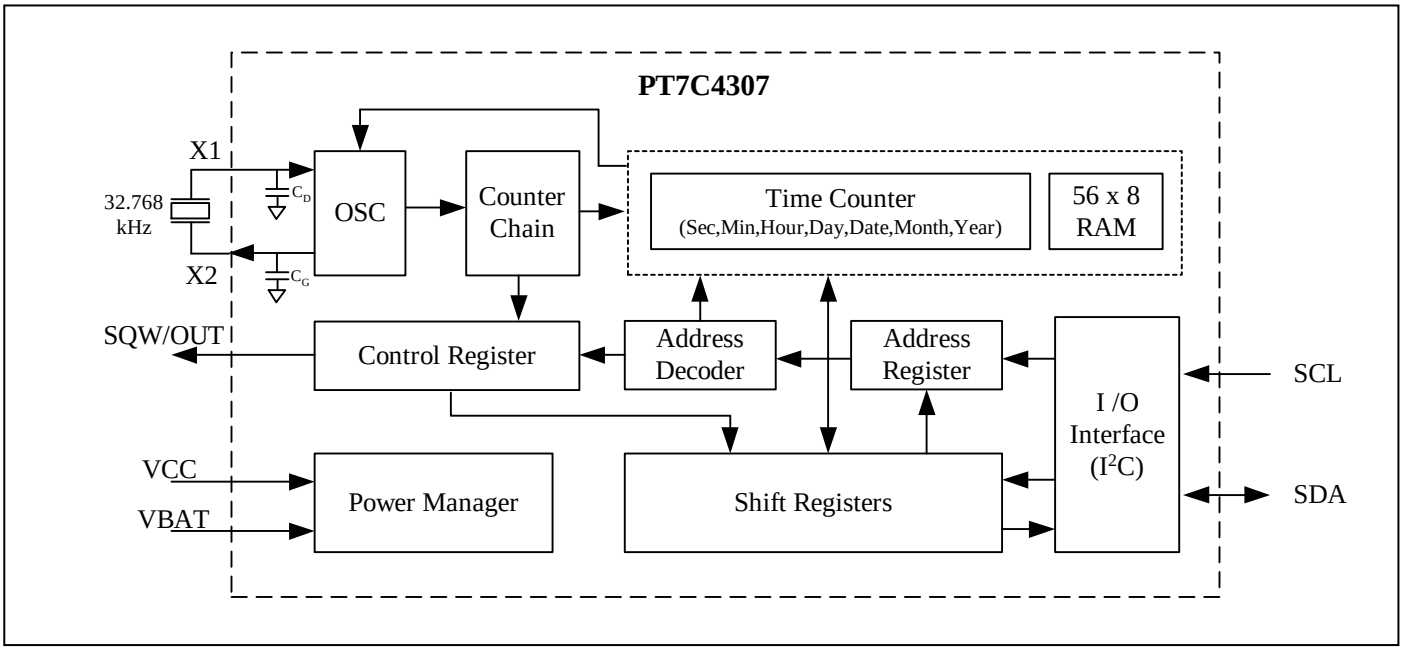
Pin Configuration



Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
7	SQW/OUT	O	**Square Wave/Output Driver.** Open drain. Four frequencies selectable: 32.768k, 8.192k, 4.096k, 1Hz when SQWE bit is set to 1.
8	VCC	P	**Power.** Primary power for PT7C4307.
3	VBAT	P	**+3V Battery Power.**
4	GND	P	**Ground.**

Function Block



Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Supply Voltage to Ground Potential (Vcc to GND) ..... -0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND) ..... -0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins) ..... -0.3V to +6.5V
DC Output Current (FOUT) ..... -0.3V to (V_{cc}+0.3V)
Power Dissipation ..... 320mW (depend on package)
Junction Temperature ..... 125°C max

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Part No.	Symbol	Description	Min	Type	Max	Unit
PT7C4307	V_{CC}	Power voltage	4.5	5	5.5	V
	V_{BAT}	Battery voltage	2	-	3.5	
	V_{IH}	Input high level	2.2	-	V_{CC}+0.3	
	V_{IL}	Input low level	-0.3	-	0.8	
	T_A	Operating temperature	-40	-	85	℃

DC Electrical Characteristics

Unless otherwise specified, V_{DD} = 4.5 ~ 5.5 V, T_A = -40 ℃ to +85 ℃

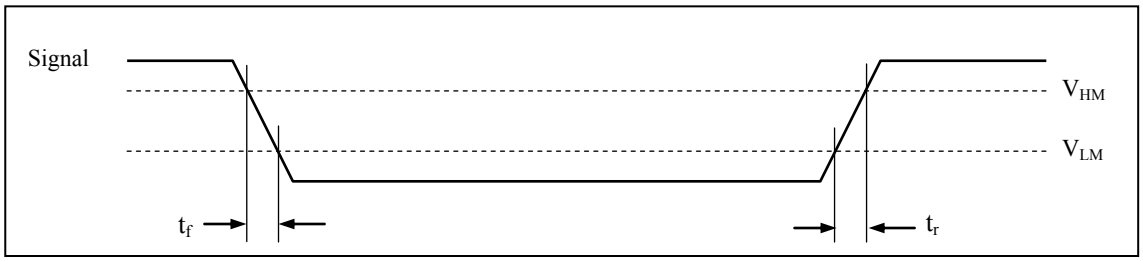
Sym.	Item	Pin	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	V_{CC}		4.5	5.0	5.5	V
V_{BAT}	Supply voltage	V_{BATT}		2.0	-	3.5	
V_{PF}	Power fail voltage		Note 4	1.216× V_{BAT}	1.25× V_{BAT}	1.284× V_{BAT}	V
I_{CC}	Current consumption	V_{CC}	OSC on, Note 3	-	-	1.5	mA
			OSC off, Note 1	-	-	200	µA
I_{BAT}	Current consumption	V_{BAT}	OSC on, SQW/OUT off, Note 2	-	300	500	nA
			OSC on, SQW/OUT on (32kHz)	-	480	800	
V_{IL}	Low-level input voltage	SCL		-	-	0.8	V
V_{IH}	High-level input voltage	SCL		2.0	-	-	
V_{OL}	Low-level output voltage	SDA	I_{OL} = 5mA	-	-	0.4	V
I_{IL}	Input leakage current	SCL		-	-	1	µA
I_{OZ}	Output current when OFF	SDA		-	-	1	µA

Note:

1. V_{CC} = 5.0V and SDA, SCL = 5.0V.
2. V_{CC} = 0V, V_{BAT} = 3V.
3. SCL clocking at max frequency = 400 kHz. SDA pin open, /EOSC bit = 0 (oscillator enabled)
4. V_{PF} measured at V_{BAT} = 3.0V.

AC Electrical Characteristics

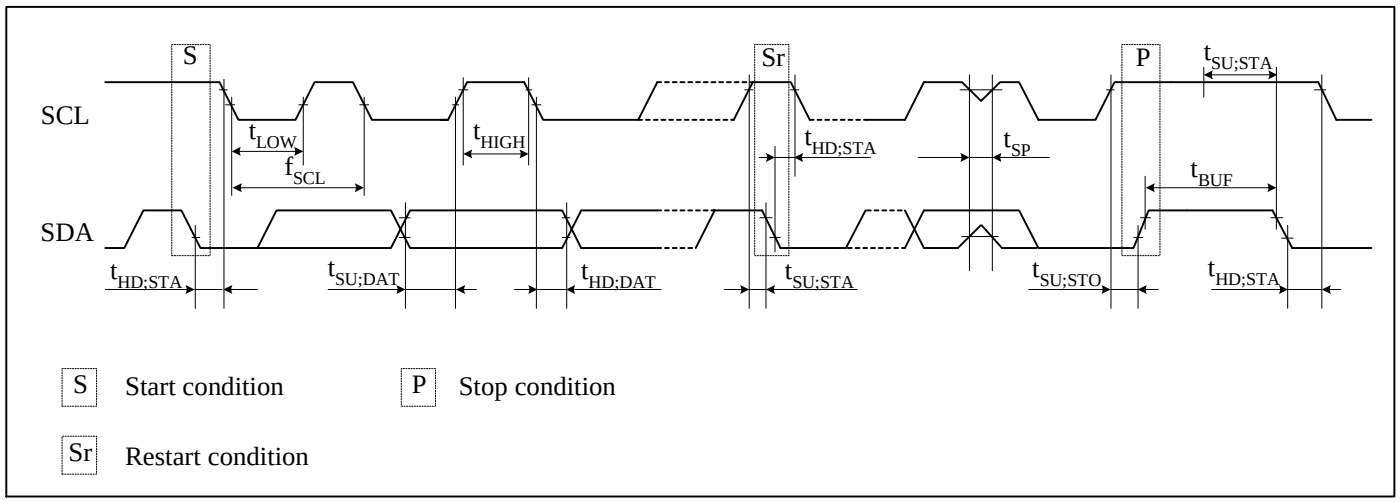
Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



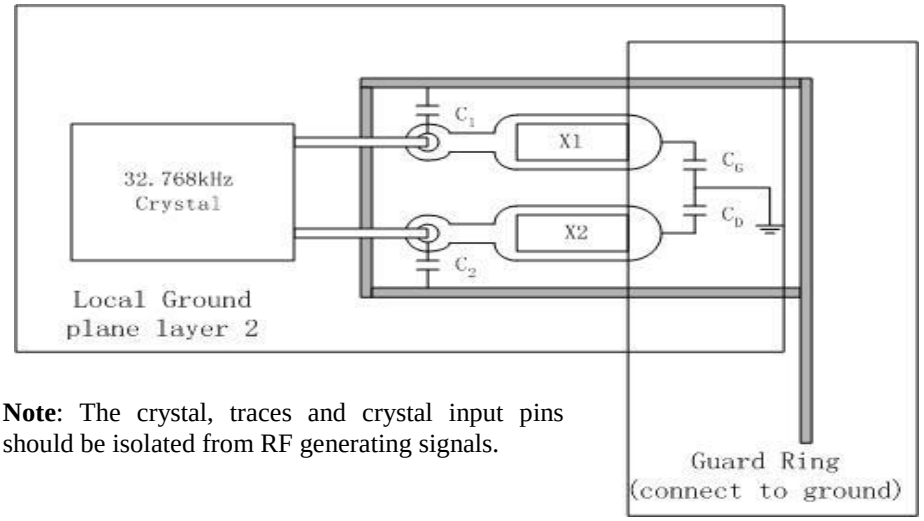
Over the operating range

Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	-	-	µs
$t_{HD;STA}$	START condition hold time	0.6	-	-	µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200	-	-	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	µs
$t_{SU;STO}$	STOP condition setup time	0.6	-	-	µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	µs
t_{LOW}	When SCL = "L"	1.3	-	-	µs
t_{HIGH}	When SCL = "H"	0.6	-	-	µs
t_r	Rise time for SCL and SDA	-	-	0.3	µs
t_f	Fall time for SCL and SDA	-	-	0.3	µs
t_{SP}*	Allowable spike time on bus	-	-	50	ns
C_B	Capacitance load for each bus line	-	-	400	pF

*** Note:** only reference for design



Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	20	pF
	X2 to GND	C_D	20	pF
Recommended External capacitors	X1 to GND	C_1	4	pF
	X2 to GND	C_2	4	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768Hz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	12.5	-	pF

Function Description

Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

Oscillator enable/disable

Oscillator can be enabled or disabled by /EOSC bit. But time count chain does not shut down when the bit is logic 1.

RAM

56×8 nonvolatile RAM are available for customer use.

Registers

Allocation of registers

Addr. (hex)*1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	/EOSC*2	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Control*3	OUT*4	0	0	SQWE*5	0	0	RS1*6	RS0*6
08~3F	RAM*7	-	-	-	-	-	-	-	-

Caution points:

*1. PT7C4307 uses 6 bits for address. That is if write data to 41H, the data will be written to 01H address register.
*2. Oscillator Enable bit. When this bit is set to 1, oscillator is stopped but time count chain is still active.
*3. Control register was used to select SQW/OUT pin output square wave with one of 4 kinds of frequency or DC level.
*4. Control SQW/OUT pin output DC level when square wave is disabled.
*5. Square wave outputs enable at SQW/OUT pin.
*6. Square wave output frequency select.
*7. PT7C4307 has 56×8 static RAM for customer use. It is volatile RAM.
*8. All bits marked with "0" are read-only bits. Their value when read is always "0". All bits marked with "-" are customer using space.

Control and Status Register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control	OUT	0	0	SQWE	0	0	RS1	RS0
	(default)	0	0	0	0	0	0	1	1

- **OUT**

It controls the output level of the SQW/OUT pin when the square wave output is disabled.

OUT	Data	Description
Read / Write	0	When SQWE = 0, SQW/OUT pin output low. Default
	1	When SQWE = 0, SQW/OUT pin output high.

- **SQWE (Square Wave Enable)**

This bit, when set to a logic 1, will enable the oscillator output. The frequency of the square wave output depends upon the value of the RS0 and RS1 bits. With the square wave output set to 1Hz, the clock registers update on the falling edge of the square wave.

- **RS (Rate Select)**

These bits control the frequency of the square wave output when the square wave output has been enabled.

RS1, RS0	Data	SQW output freq. (Hz)
Read / Write	00	1
	01	4.096k
	10	8.192k
	11	32.768k Default

Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	/EOSC*	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

*** Note:** /EOSC bit must be written into 0 to start the time count.

- **12, /24 bit**

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour system
	1	12-hour system

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	52 (AM 12)	12	72 (PM 12)
01	41 (AM 01)	13	61 (PM 01)
02	42 (AM 02)	14	62 (PM 02)
03	43 (AM 03)	15	63 (PM 03)
04	44 (AM 04)	16	64 (PM 04)
05	45 (AM 05)	17	65 (PM 05)
06	46 (AM 06)	18	66 (PM 06)
07	47 (AM 07)	19	67 (PM 07)
08	48 (AM 08)	20	68 (PM 08)
09	49 (AM 09)	21	69 (PM 09)
10	50 (AM 10)	22	70 (PM 10)
11	51 (AM 11)	23	71 (PM 11)

***** Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

Days of the week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
05	Months	0	0	0	M10	M8	M4	M2	M1
	(default)	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced by correct time, otherwise it will cause the clock counter malfunction.

I²C Bus Interface

Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.

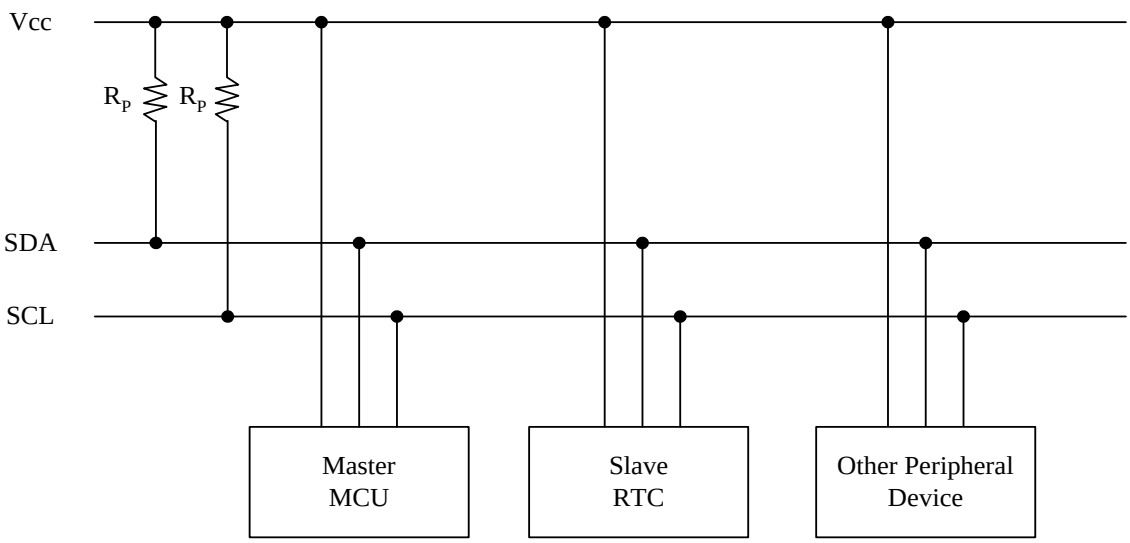
Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

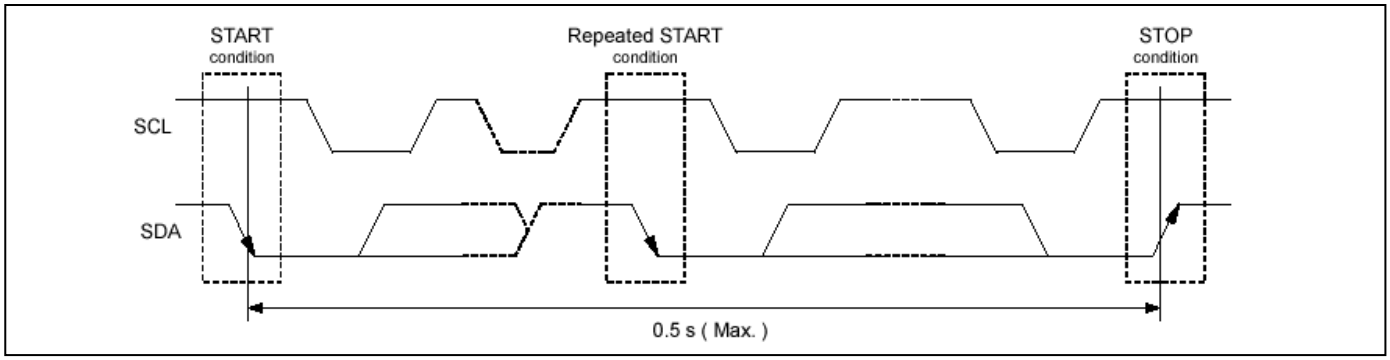
Figure 1. System Configuration



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_P of SCL may not required.

Starting and Stopping I²C Bus Communications

Figure 2. Starting and Stopping on I²C Bus



1) START Condition, Repeated START Condition, and STOP Condition

a) START condition
SDA level changes from high to low while SCL is at high level

b) STOP condition
SDA level changes from low to high while SCL is at high level

c) Repeated START condition (RESTART condition)
In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

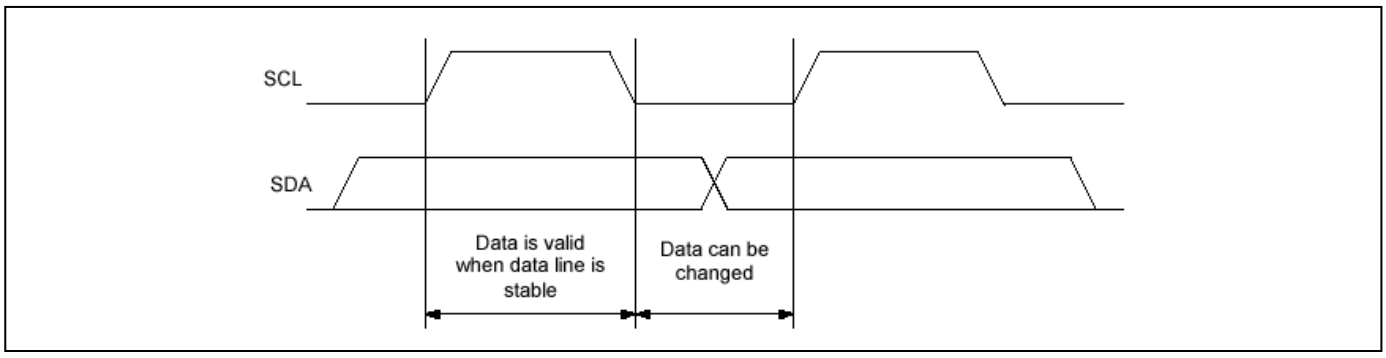
2) Data Transfers and Acknowledge Responses during I²C-BUS Communication

a) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

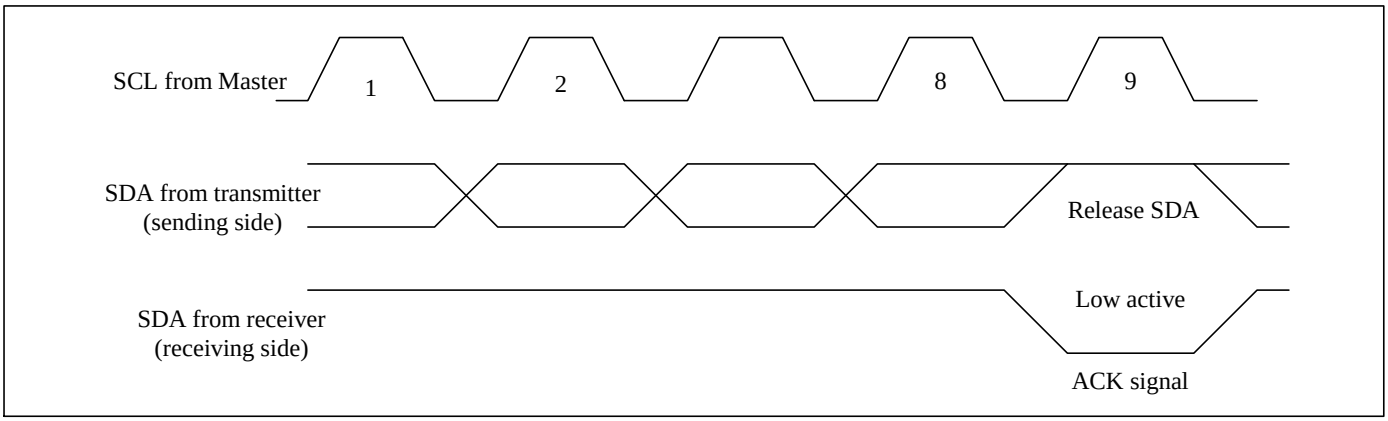


*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

b) Data Acknowledge Response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

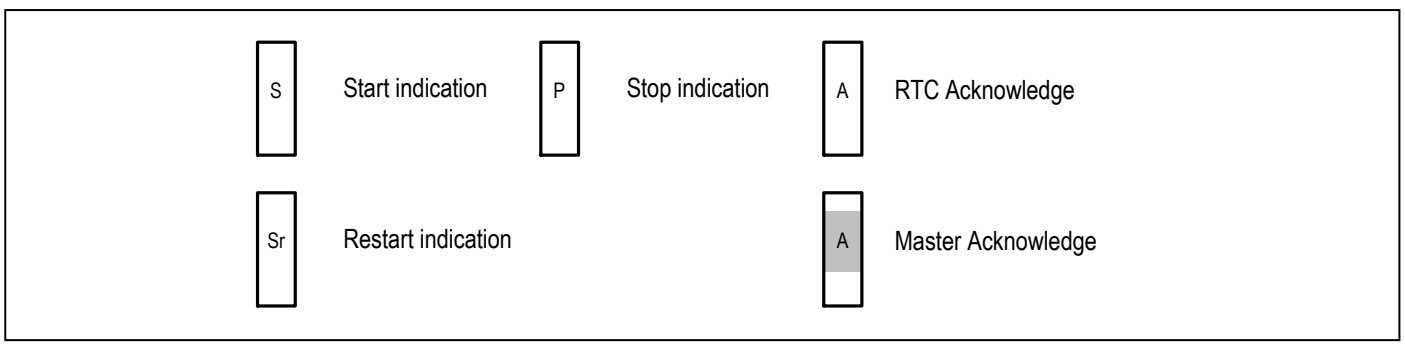
All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. See table for the details.

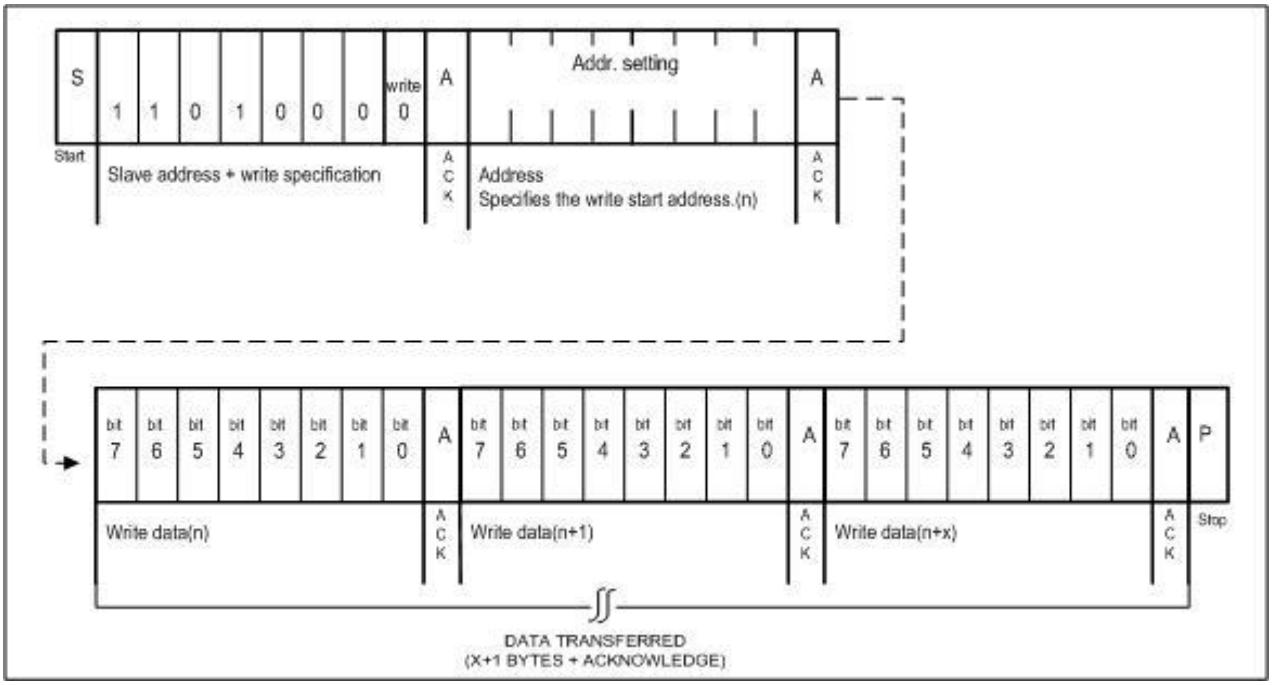
An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

Operation	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	D1 h	1	1	0	1	0	0	0	1 (= Read)
Write	D0 h								0 (= Write)

I²C Bus's Basic Transfer Format

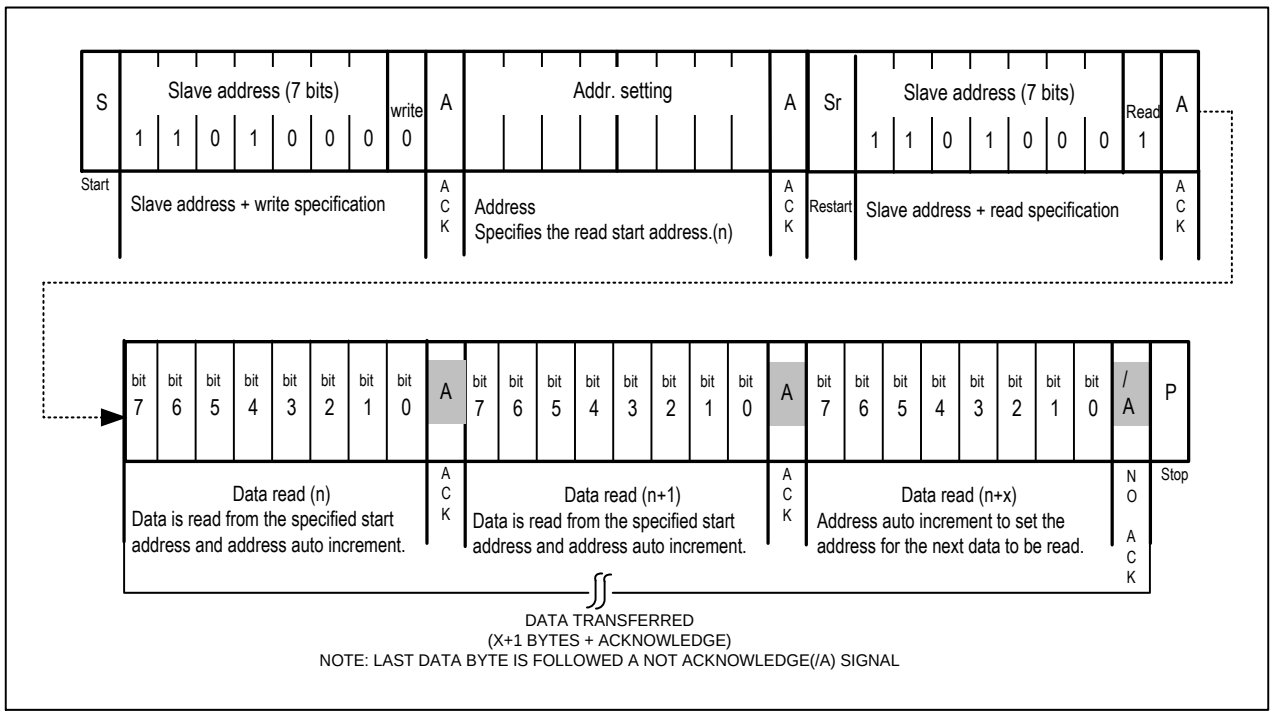


1) Write via I²C Bus

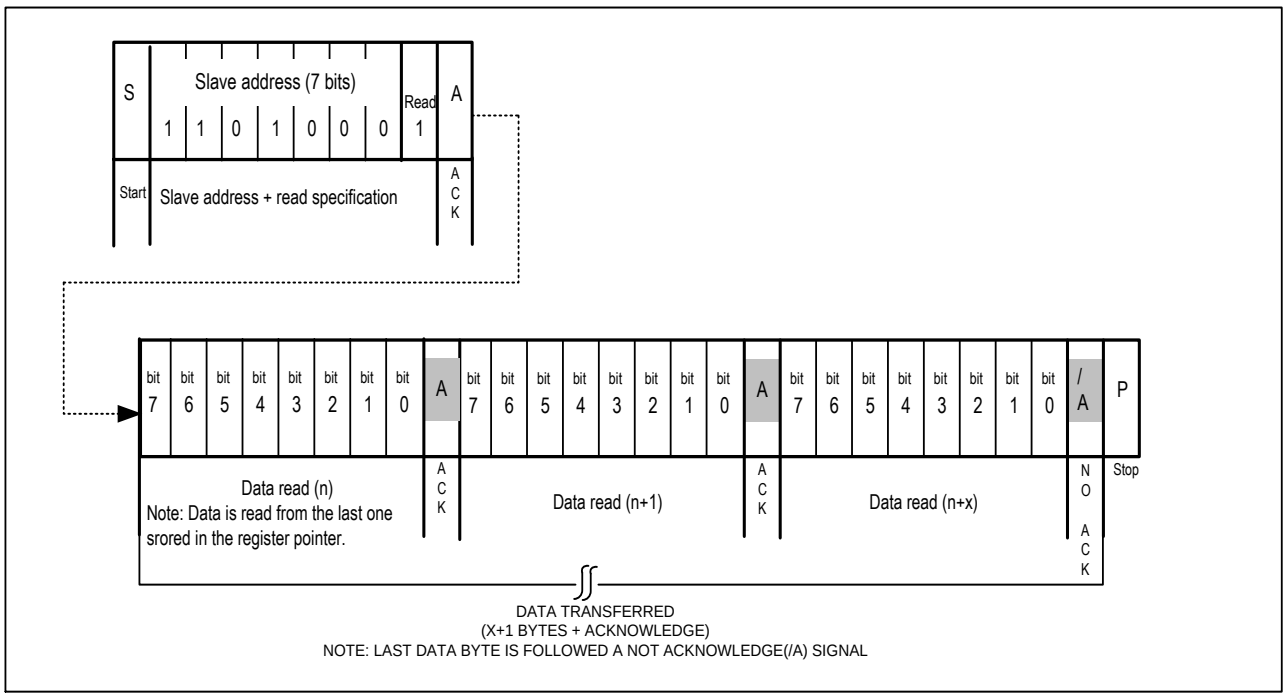


2) Read via I²C Bus

a) Standard Read



b) Simplified Read



N

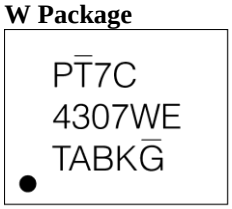
ote:

1.The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.

2.49H, 4AH are used as test mode address. Customer should not use the addresses.

Part Marking

W Package



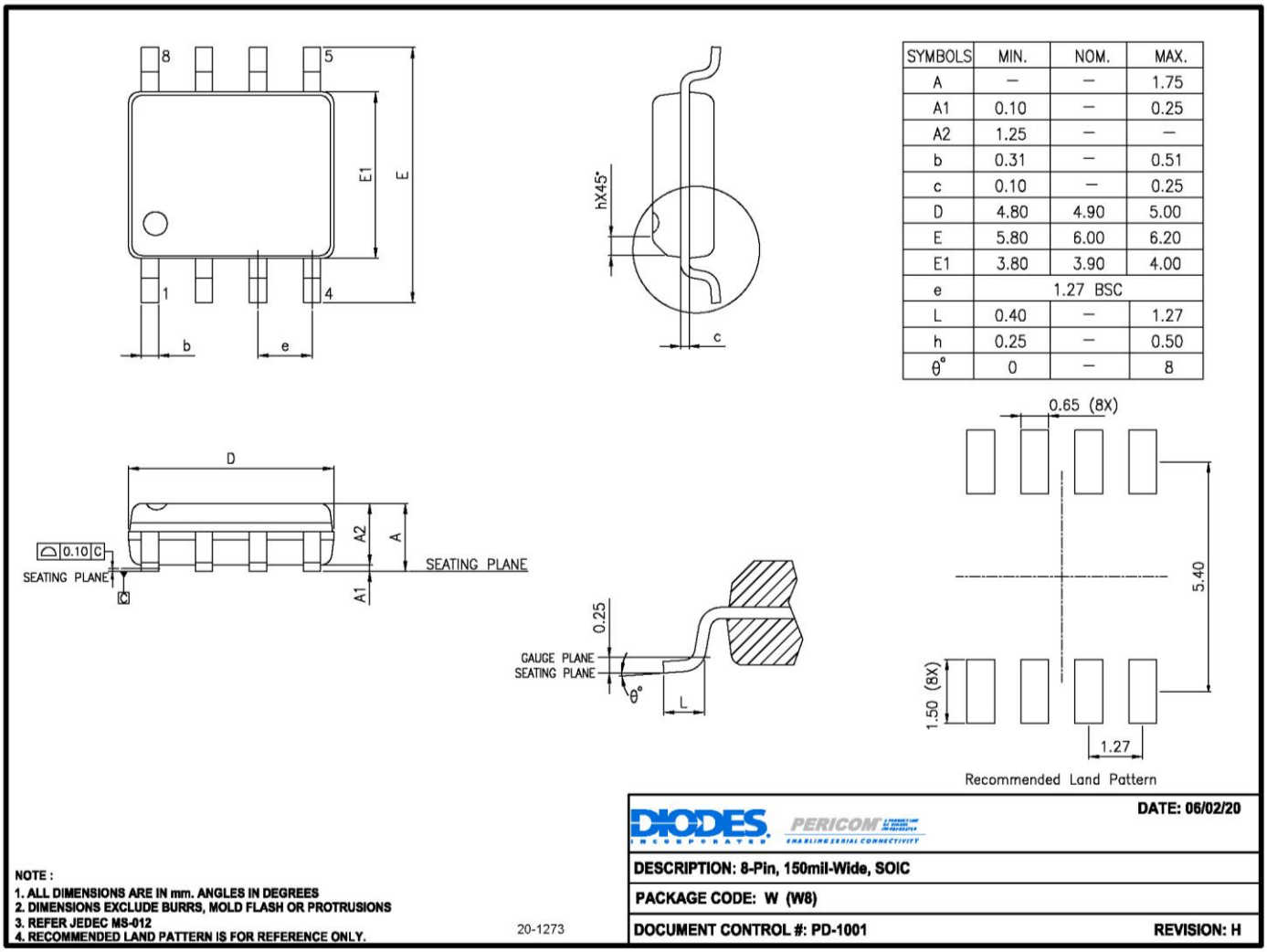
T: Die Rev
AB: Date Code (Year & Workweek)
K: Assembly Site Code
G: Wafer Fab Site Code
Bar above "T" means Fab3 of MGN
Bar above "G" means Cu wire

ZE Package

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical

8- SOIC (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

20-1273

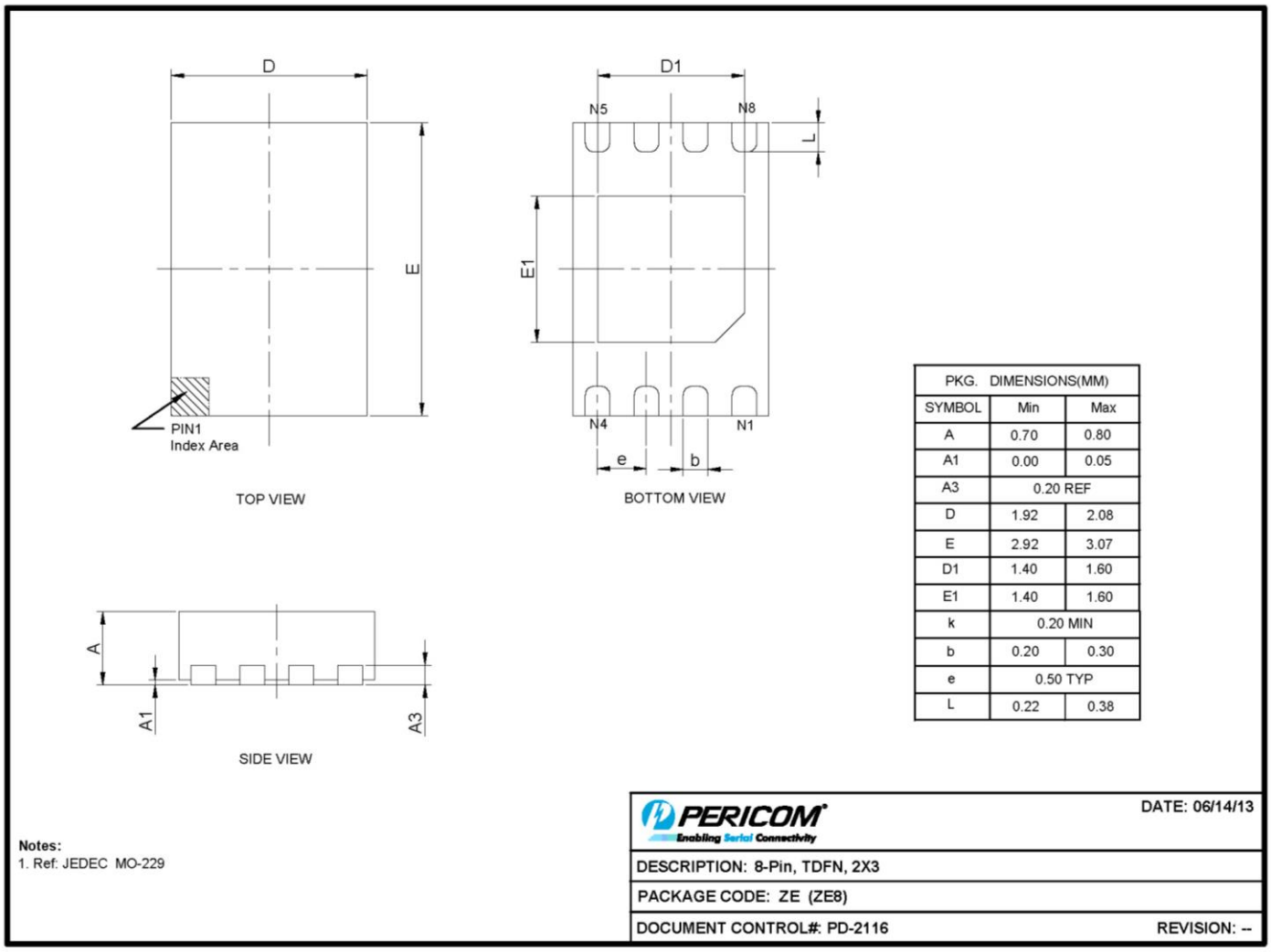
DATE: 06/02/20

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: H

8- TDFN (ZE)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

13-0155

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package Description
PT7C4307WEX	W	8-Pin, 150mil-Wide (SOIC)
PT7C4307ZEEX	ZE	8-Pin, 2x3 (TDFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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