Figure 3. Pin Configuration

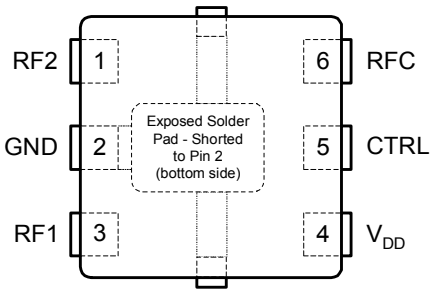


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF2	RF2 port.[1]
2	GND	Ground Connection. Traces should be physically short and connected to the ground plane. This pin is connected to the exposed solder pad that also must be soldered to the ground plane for best performance.
3	RF1	RF1 port.[1]
4	V_{DD}	Nominal 3 V supply connection.
5	CTRL	CMOS or TTL logic level: High = RFC to RF1 signal path Low = RFC to RF2 signal path
6	RFC	Common RF port for switch.[1]

Notes: 1. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CTRL} = 3V)		29	35	µA
T_{OP} Operating temperature range	-40		85	°C
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4237 in the 6-lead 8x3 DFN package is MSL1.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for the CTRL input	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		5.0	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50 Ω)		35	dBm
V_{ESD}	ESD voltage (Human Body Model)		250	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Control Logic Input

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a standard 5-volt TTL control signal. This TTL control signal input must not exceed 5-volts or damage to the switch could result.

Table 5. Control Logic Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFC to RF1
CTRL = CMOS or TTL Low	RFC to RF2

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss - RFC to RF1

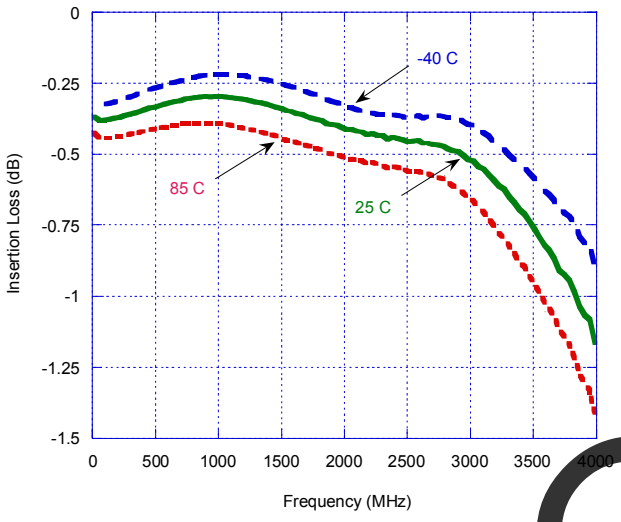


Figure 5. Input 1dB Compression Point

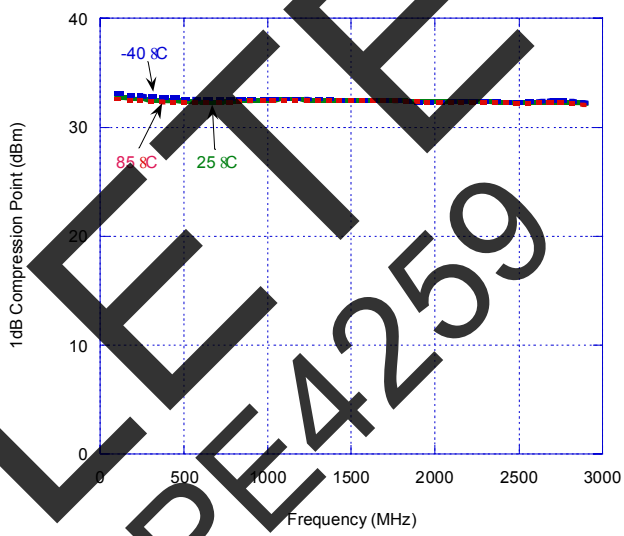


Figure 6. Insertion Loss - RFC to RF2

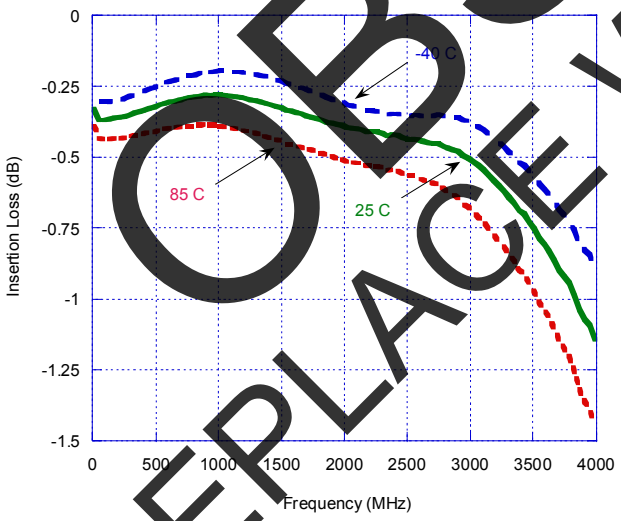
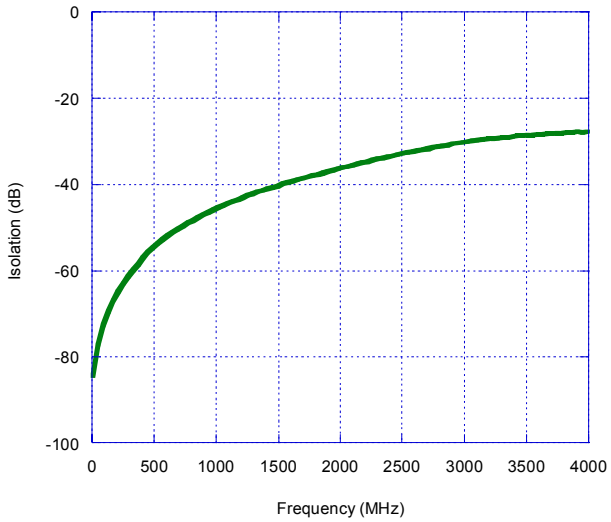


Figure 7. Isolation - RFC to RF1
T = 25 °C



Typical Performance Data @ 25 °C

Figure 8. Isolation – RFC to RF2

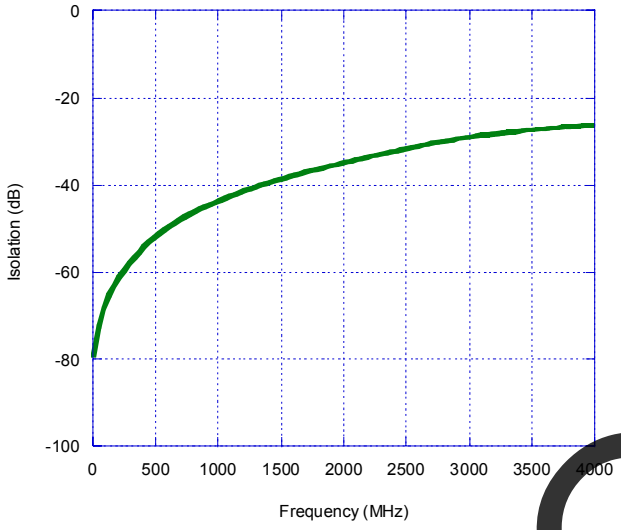


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

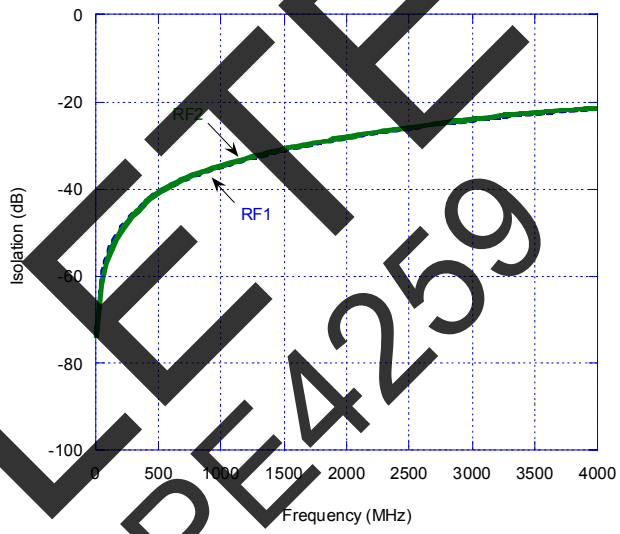


Figure 10. Return Loss – RFC to RF1, RF2

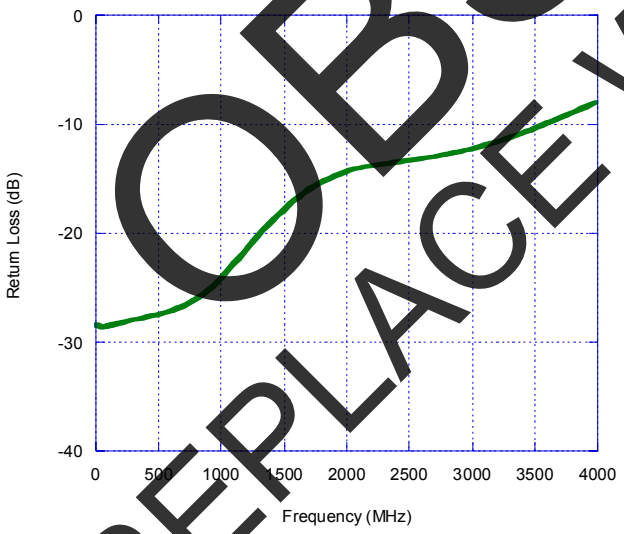
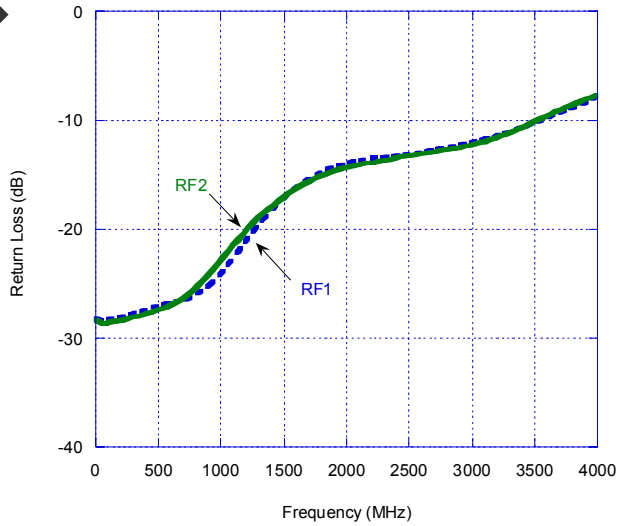


Figure 11. Return Loss – RF1, RF2



Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4237 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50 Ω transmission lines to the top two SMA connectors on the right side of the board, J2 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device CNTL input. The fourth pin to the right (J6-7) is connected to the device V_{DD} input. A decoupling capacitor (100 pF) is provided on both CTRL and V_{DD} traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 12. Evaluation Board Layouts
Peregrine Specification 101/0085

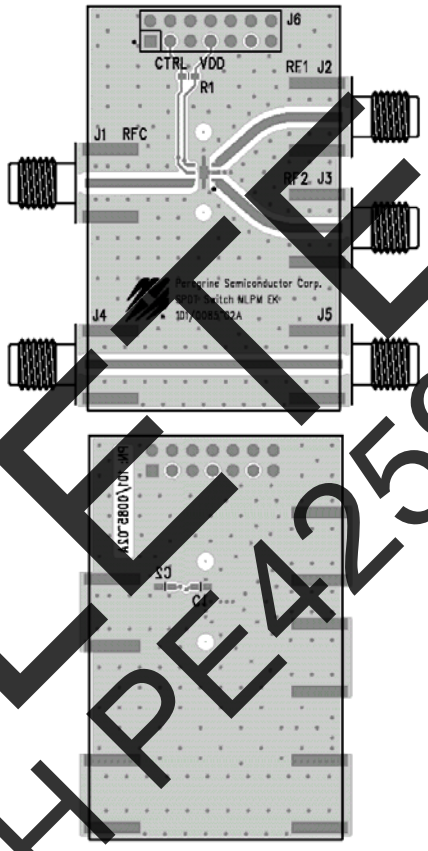


Figure 13. Evaluation Board Schematic
Peregrine Specification 102/0110

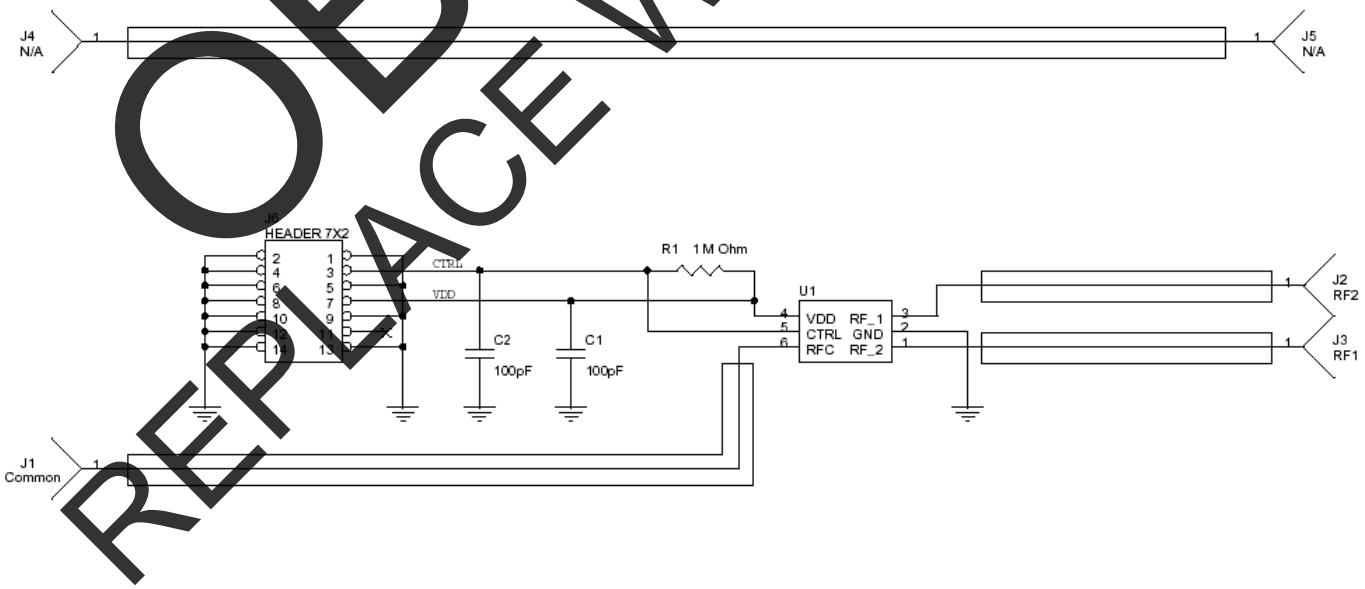
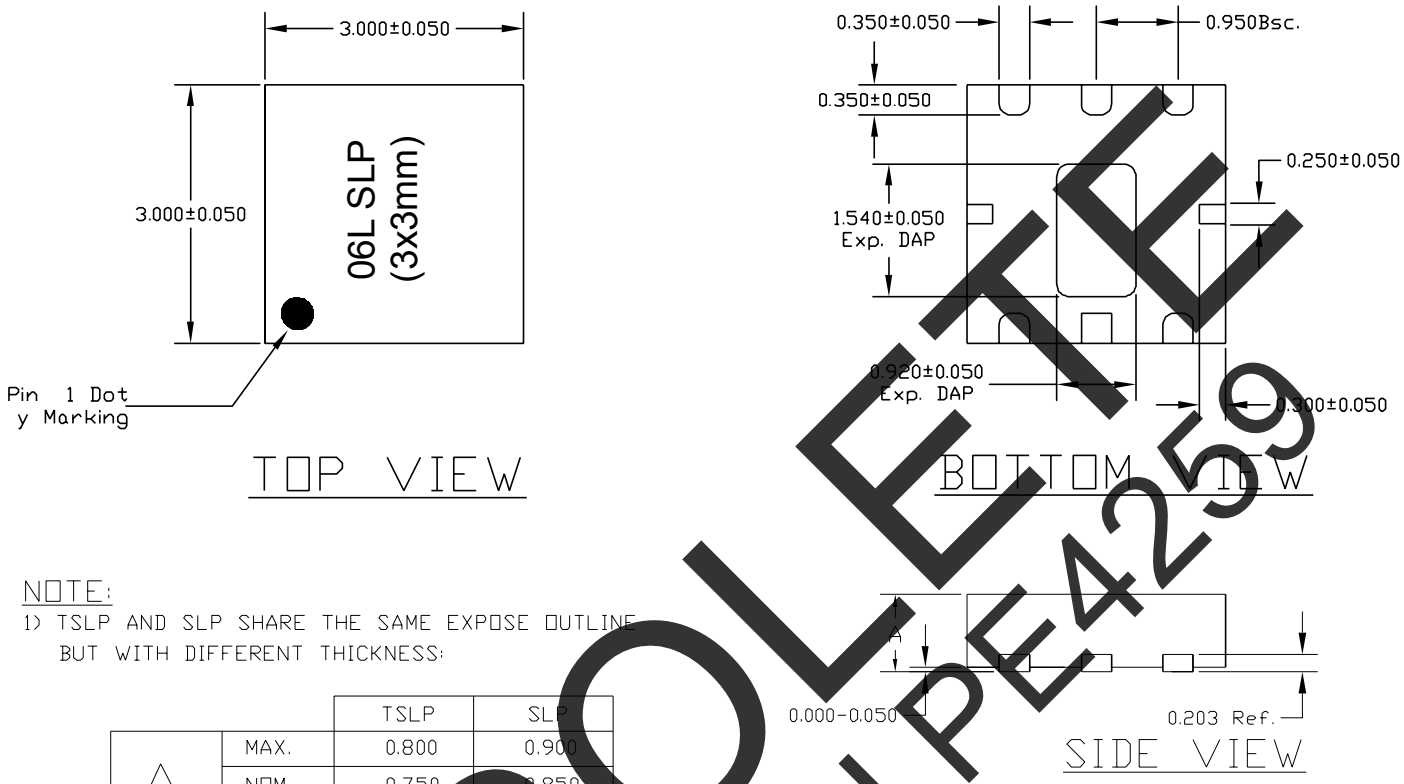


Figure 14. Package Drawing

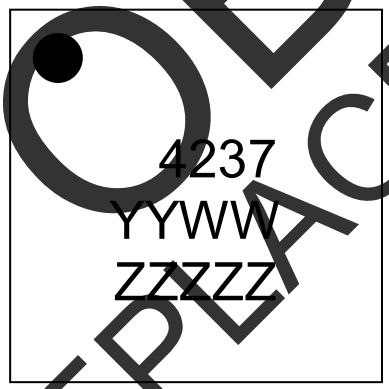
6-lead DFN



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

NOTE: The exposed solder pad (on the bottom of the package) is electrically connected to pin 2 (fused.)

Figure 15. Marking Specifications



YYWW = Date Code (last two digits of year and work week)
ZZZZZ = Last five digits of Lot Number

Figure 16. Tape and Reel Specifications

6-lead DFN

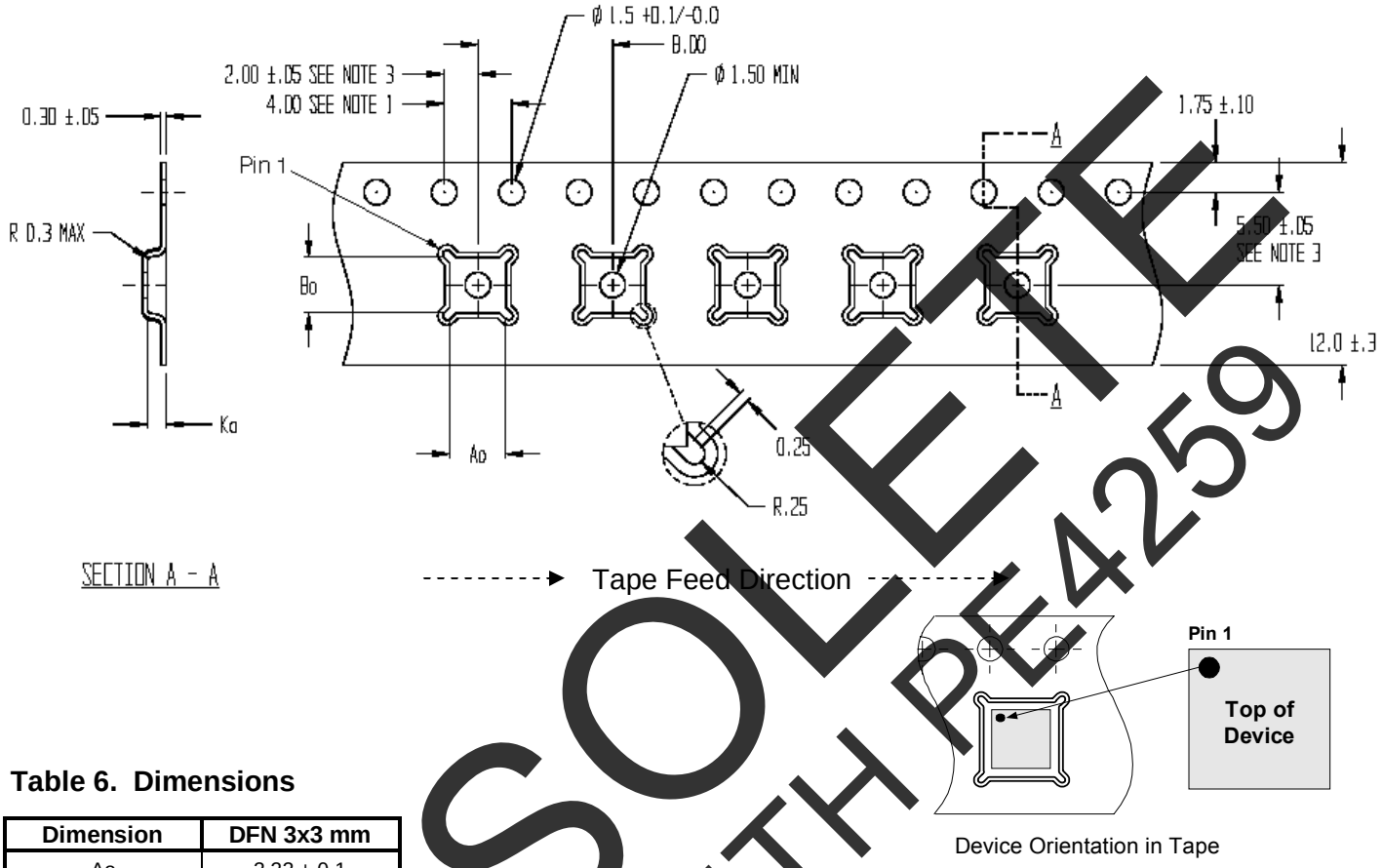


Table 6. Dimensions

Dimension	DFN 3x3 mm
Ao	3.23 ± 0.1
Bo	3.17 ± 0.1
Ko	1.37 ± 0.1
P	4 ± 0.1
W	8 +0.3, -0.1
T	0.254 ± 0.02
R7 Quantity	3000
R13 Quantity	N.A.

Note: R7 = 7 inch Lock Reel, R13 = 13 inch Lock Reel

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4237-51	4237	PE4237G-06DFN 3x3mm-12800F	Green 6-lead 3x3 mm DFN	Tape or loose
4237-52	4237	PE4237G-06DFN 3x3mm-3000C	Green 6-lead 3x3 mm DFN	3000 units / T&R
4237-00	PE4237-EK	PE4237-06DFN 3x3mm-EK	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9380 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

High-Reliability and Defense Products

Americas
San Diego, CA, USA
Phone: 858-731-9475
Fax: 848-731-9499

Europe/Asia-Pacific
Aix-En-Provence Cedex 3, France
Phone: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea
#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

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