Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN	I	External reference Clock input.
2	FS	I	Frequency Select. Has an internal pull−down resistor. see *Frequency Selection table*
3	PD#	I	Power Down. Pull LOW to enable Power Down. Pull HIGH to disable power down. Output Clock will be LOW when power down is enabled. Has an internal pull−up resistor
4	GND	P	Ground
5	ModOUT	O	Buffered modulated Timing−Safe clock output
6	MR	I	Modulation Rate Select. When LOW selects Low Modulation Rate. Selects High Modulation Rate when pulled HIGH. Has an internal pull−up resistor.
7	SSEXTR	I	Analog Frequency Deviation Selection through external resistor to GND.
8	VDD	P	1.8 V Supply Voltage

Table 2. FREQUENCY SELECTION TABLE

FS	Frequency (MHz)
0	15−30
1	30−60

Table 3. ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.3	+2.7	V
DC Input Voltage(CLKIN)	−0.3	+2.7	V
DC Input Voltage (Except CLKIN)	−0.3	V_{DD} + 0.3	V
Storage Temperature	−65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD22−A114−B)		2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	1.6	2	V
T_A	Operating Temperature	−20	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 5. DC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 1.8 V ± 0.2 V

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
VDD	Supply Voltage			1.6	1.8	2	V
V_{IH}	Input HIGH Voltage			0.65 * V_{DD}			V
V_{IL}	Input LOW Voltage					0.35 * V_{DD}	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}				5	μA
I_{IL}	Input LOW Current	V_{IN} = 0 V				5	μA
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA (P3PSL450A)		0.75 * V_{DD}			V
		I_{OH} = −16 mA (P3PSL450AH)					
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA (P3PSL450A)				0.25 * V_{DD}	V
		I_{OL} = 16 mA (P3PSL450AH)					
I_{CC}	Static Supply Current	CLKIN & PD# pins pulled to GND				10	μA
I_{DD}	Dynamic Supply Current	Unloaded Output	FS = 0, @ 15 MHz		1.7	2.2	mA
			FS = 0, @ 30 MHz		3.0	3.7	
			FS = 1, @ 30 MHz		2.6	3.7	
			FS = 1, @ 60 MHz		4.3	6.4	
Z_o	Output Impedance	P3PSL450A			23		Ω
		P3PSL450AH			17		

Table 6. AC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 1.8 V ± 0.2 V

Parameter	Test Conditions			Min	Typ	Max	Unit
Input Frequency	FS = 0			15		30	MHz
	FS = 1			30		60	
ModOUT	FS = 0			15		30	
	FS = 1			30		60	
Duty Cycle (Notes 1 and 2)	Measured at V_{DD} / 2			45	50	55	%
Rise Time (Notes 1 and 2)	Measured between 20% to 80%	P3PSL450A			1.3	2.1	ns
		P3PSL450AH			1	1.7	
Fall Time (Notes 1 and 2)	Measured between 80% to 20%	P3PSL450A			1.3	2.1	ns
		P3PSL450AH			1	1.7	
Cycle−to−Cycle Jitter (Note 2)	Unloaded output with SSEXTR pin OPEN	FS = 0	15 MHz		±150	±250	ps
			24 MHz		±100	±150	
			30 MHz		±80	±150	
		FS = 1	30 MHz		±150	±250	
			60 MHz		±100	±150	
PLL Lock Time [2]	Stable power supply, valid clock presented on CLKIN pin, PD# toggled from Low to High					1	ms

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

SWITCHING WAVEFORMS

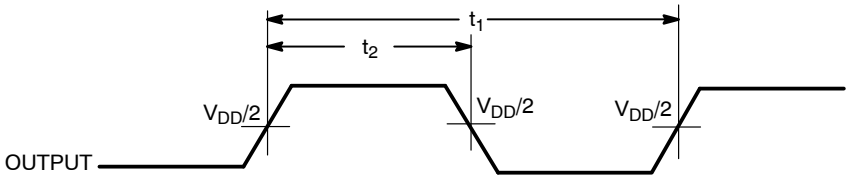


Figure 2. Duty Cycle Timing

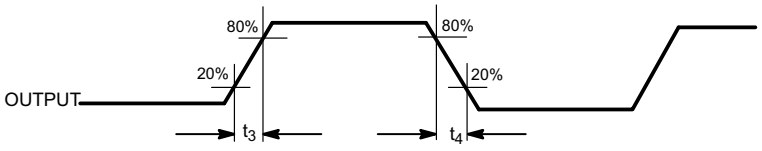
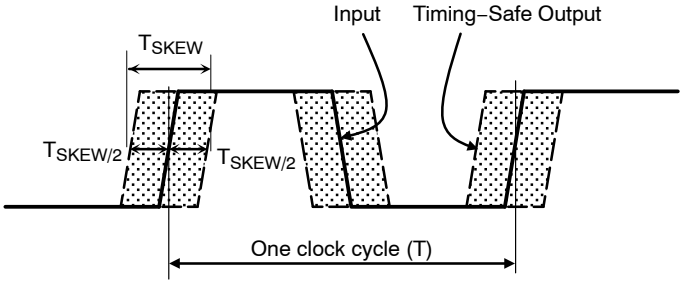


Figure 3. Output Rise/Fall Time



T_{SKEW} represents input−output skew when spread spectrum is ON
For example, $T_{SKEW/2}$ = ±0.20 * T for an Input clock of 24 MHz, translates in to (1/24 MHz) * 0.20 = 8.33 ns

Figure 4. Input−Output Skew

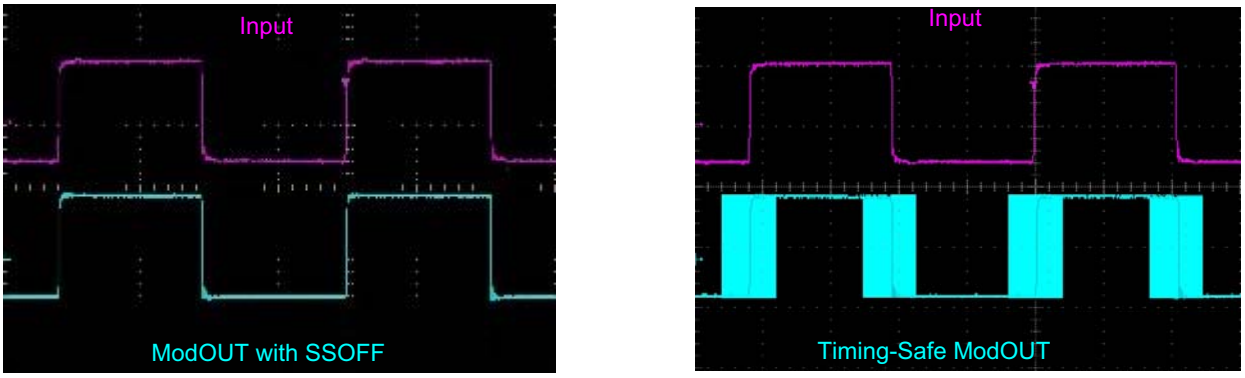


Figure 5. Typical Example of Timing−Safe Waveform

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

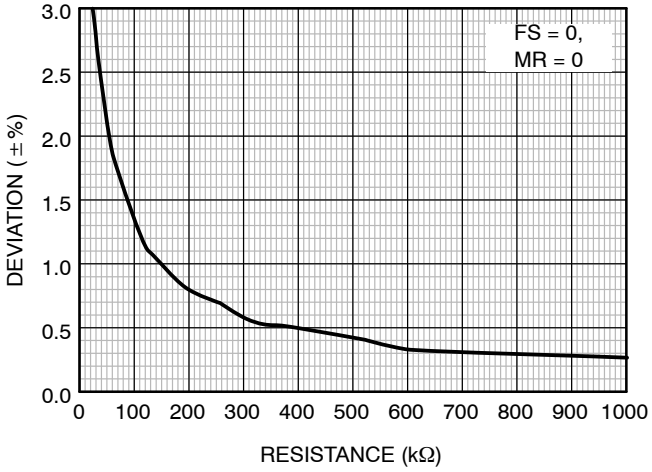


Figure 6. Deviation vs SSEXTR Chart (CLKIN = 15 MHz)

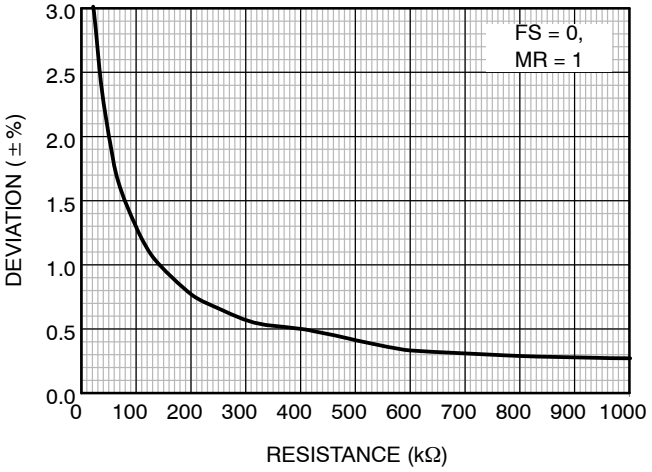


Figure 7. Deviation vs SSEXTR Chart (CLKIN = 15 MHz)

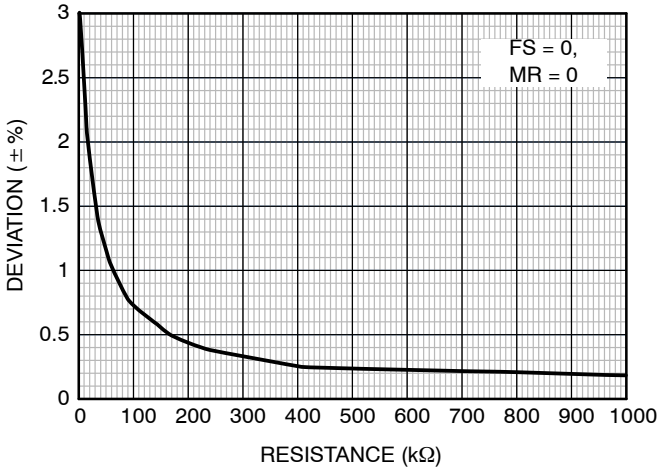


Figure 8. Deviation vs SSEXTR Chart (CLKIN = 24 MHz)

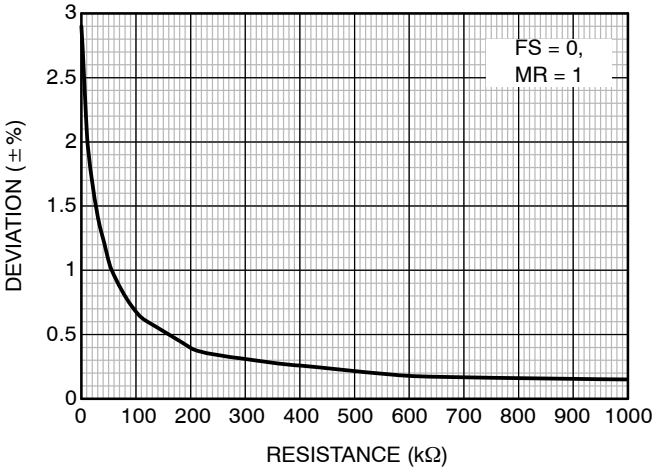


Figure 9. Deviation vs SSEXTR Chart (CLKIN = 24 MHz)

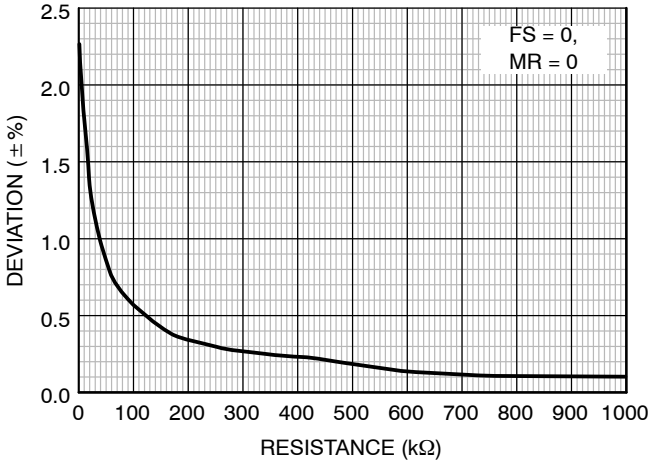


Figure 10. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

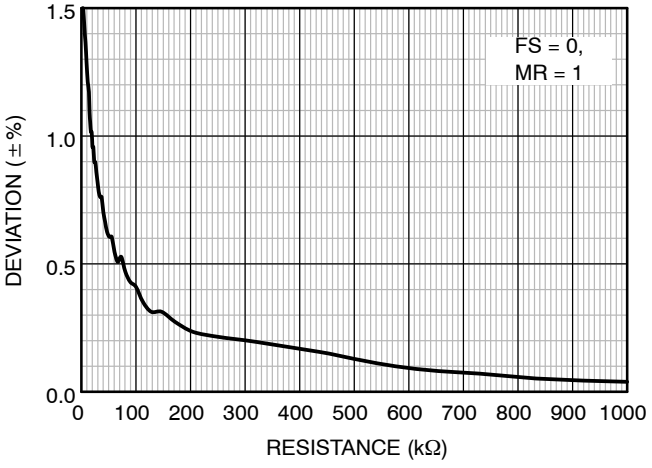


Figure 11. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

DEVIATION VERSUS SSEXTR RESISTANCE CHARTS

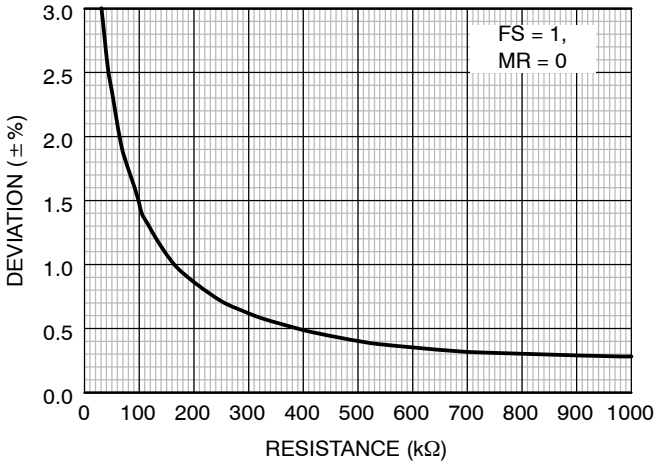


Figure 12. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

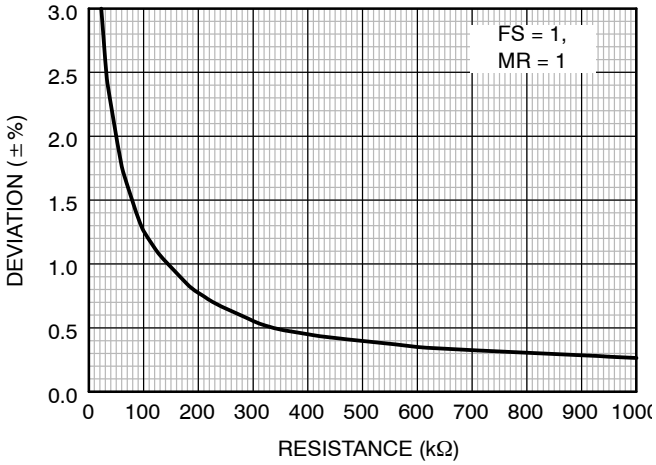


Figure 13. Deviation vs SSEXTR Chart (CLKIN = 30 MHz)

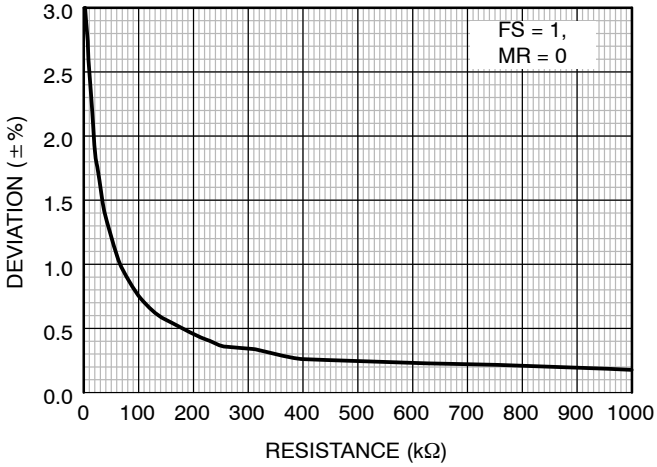


Figure 14. Deviation vs SSEXTR Chart (CLKIN = 48 MHz)

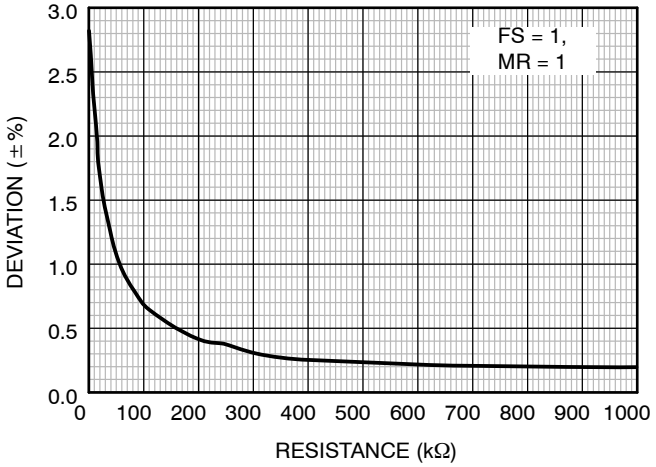


Figure 15. Deviation vs SSEXTR Chart (CLKIN = 48 MHz)

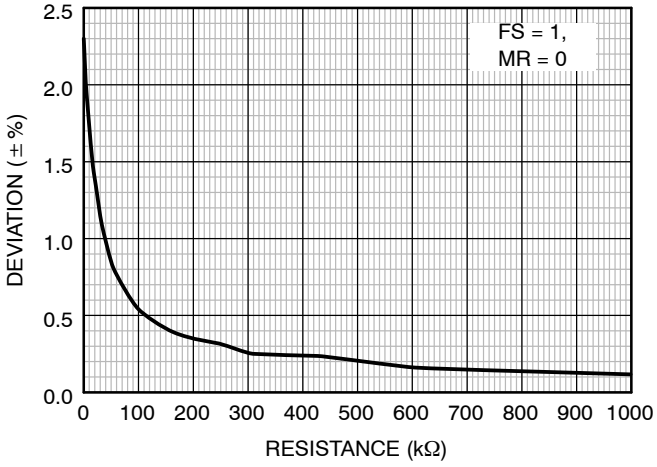


Figure 16. Deviation vs SSEXTR Chart (CLKIN = 60 MHz)

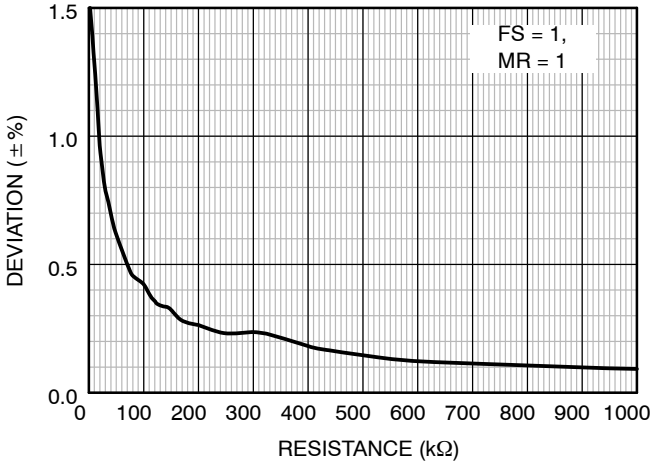
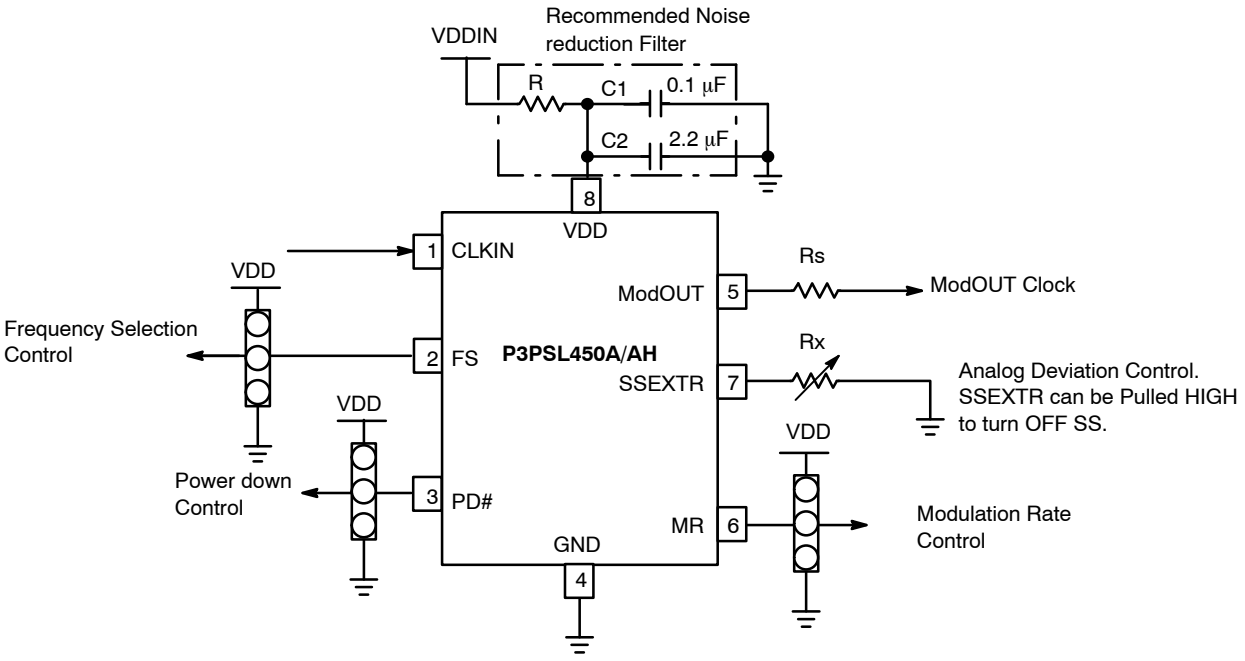


Figure 17. Deviation vs SSEXTR Chart (CLKIN = 60 MHz)



NOTE: Refer to Pin Description table for Functionality details

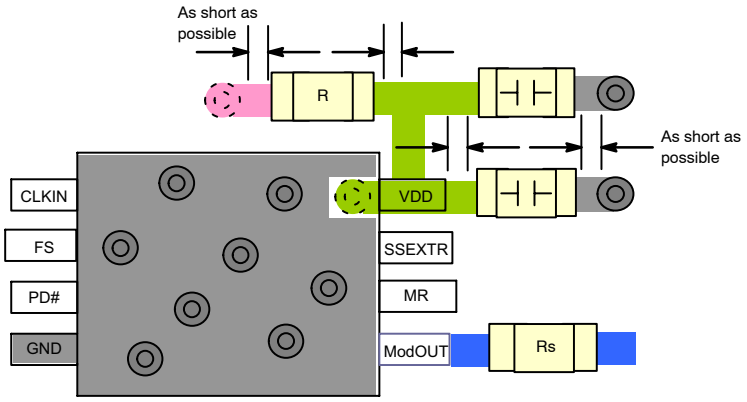
Figure 18. Typical Application Schematic

PCB LAYOUT RECOMMENDATION

For optimum device performance, following guidelines are recommended.

- Dedicated V_{DD} and GND planes.
- The device must be isolated from system power supply noise. A 0.1 μF and a 2.2 μF decoupling capacitor should be mounted on the component side of the board as close to the V_{DD} pin as possible. No vias should be used between the decoupling capacitor and V_{DD} pin. The PCB trace to V_{DD} pin and the ground via should be kept as short as possible. All the V_{DD} pins should have decoupling capacitors.
- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the Figure below:



ORDERING INFORMATION

Ordering Code	Marking	Temperature	Package Type	Shipping†
P3PSL450AG−08CR	FA	−20°C to +85°C	8− pin (2 mm x 2 mm) WDFN (Pb−Free)	Tape & Reel
P3PSL450AHG−08CR	FC	−20°C to +85°C	8− pin (2 mm x 2 mm) WDFN (Pb−Free)	Tape & Reel

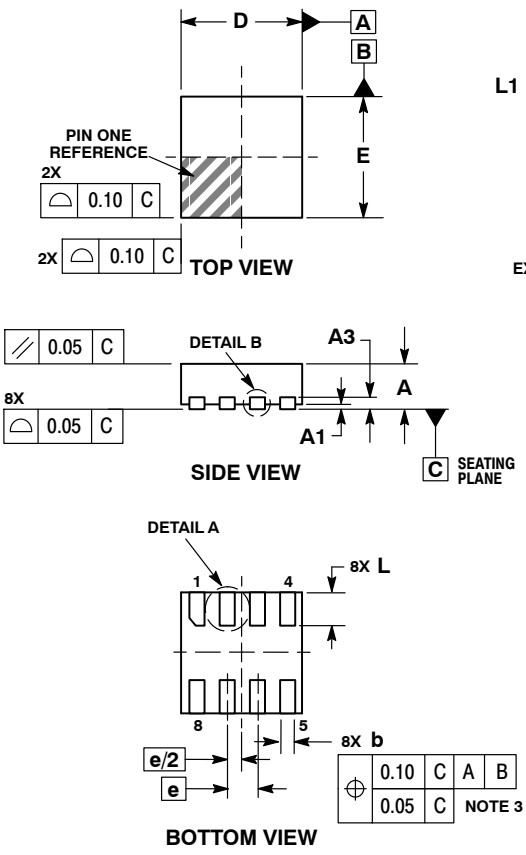
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

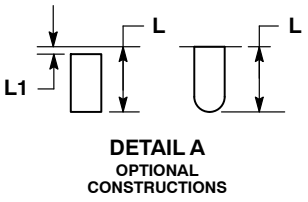
*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

P3PSL450A

PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511AQ−01
ISSUE A

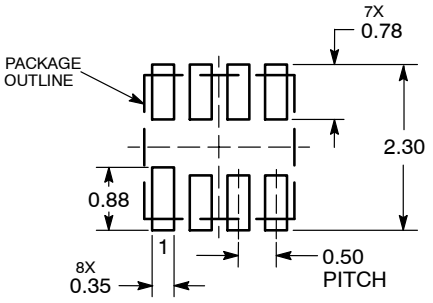




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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