TABLE OF CONTENTS

REVISION HISTORY

1/15—Rev. C to Rev. D

Changed Minimum Output Voltage Swing High Parameter from 4.0 V to 3.9 V; Table 2 ... 4
Changes to Ordering Guide ... 18

9/09—Rev. B to Rev. C

Updated Format ... Universal
Deleted OP493 ... Universal
Changes to Features and General Description Sections ... 1
Deleted 8-Lead Epoxy DIP Pin Configurations for OP193 and OP293, and 14-Lead Epoxy DIP and 16-Lead Wide Body SOL Pin Configurations for OP493 ... 1
Changes to Offset Voltage Parameter and Large Signal Voltage Gain, R_L = 100 kΩ, −10 V ≤ V_{OUT} ≤ +10 V Parameter, and Power Supply Rejection Ratio Parameter, Table 1 ... 3
Changes to Offset Voltage Parameter and Power Supply Rejection Ratio Parameter, Table 2 ... 4
Changes to Offset Voltage Parameter and Power Supply Rejection Ratio Parameter, Table 3 ... 6
Changes to Offset Voltage Parameter and Power Supply Rejection Ratio Parameter, Table 4 ... 7
Changes to Table 5 and Table 6 ... 8
Changes to Figure 3 to Figure 6 ... 9
Changes to Figure 10 and Figure 12 ... 10
Changes to Functional Description Section and Figure 26 ... 13
Deleted A Micropower, Single-Supply Quad Voltage Output 8-Bit DAC Section ... 13
Deleted Figure 13; Renumbered Sequentially ... 14
Deleted A Single-Supply Micropower Quad Programmable-Gain Amplifier Section ... 14
Changes to Output Phase Reversal—OP293 Section, Battery-Powered Applications Section, and Figure 27 ... 14
Deleted Figure 14 ... 15
Changes to Figure 31, A Single-Supply Current Monitor Section, and Figure 32 ... 15
Changes to A Low Power, Temperature to 4 mA to 20 mA Transmitter Section and Figure 35 ... 16
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

1/02—Rev. A to Rev. B

Deletion of Wafer Test Limits Table ... 5
Deletion of Dice Characteristics Images ... 6
Edits to Ordering Guide ... 6

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_S = ±15.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	E Grade			F Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193						150	μV
		OP193, −40°C ≤ T_A ≤ +125°C						250	μV
		OP293			100			250	μV
		OP293, −40°C ≤ T_A ≤ +125°C			200			350	μV
Input Bias Current	I_B	V_{CM} = 0 V, −40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, −40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		−14.9		+13.5	−14.9		+13.5	V
Common-Mode Rejection	CMRR	−14.9 V ≤ V_{CM} ≤ +14 V	100	116		97	116		dB
		−14.9 V ≤ V_{CM} ≤ +14 V, −40°C ≤ T_A ≤ +125°C	97			94			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,							
		−10 V ≤ V_{OUT} ≤ +10 V	500	600		500	600		V/mV
		−40°C ≤ T_A ≤ +85°C	300			300			V/mV
		−40°C ≤ T_A ≤ +125°C		300			300		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ,							
		−10 V ≤ V_{OUT} ≤ +10 V	350			350			V/mV
		−40°C ≤ T_A ≤ +85°C	200			200			V/mV
		−40°C ≤ T_A ≤ +125°C		150			150		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ,							
		−10 V ≤ V_{OUT} ≤ +10 V	200			200			V/mV
		−40°C ≤ T_A ≤ +85°C	125			125			V/mV
		−40°C ≤ T_A ≤ +125°C		100			100		V/mV
Long-Term Offset Voltage[1]	V_{OS}				150			300	μV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$			0.2	1.75				μV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 1 mA	14.1	14.2		14.1		14.2	V
		I_L = 1 mA, −40°C ≤ T_A ≤ +125°C	14.0			14.0			V
		I_L = 5 mA	13.9	14.1		13.9	14.1		V
Output Voltage Swing Low	V_{OL}	I_L = −1 mA		−14.7	−14.6		−14.7	−14.6	V
		I_L = −1 mA, −40°C ≤ T_A ≤ +125°C			−14.4			−14.4	V
		I_L = −5 mA		+14.2	−14.1		+14.2	−14.1	V
Short-Circuit Current	I_{SC}			±25			±25		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±18 V	100	120		97	120		dB
		−40°C ≤ T_A ≤ +125°C	97			94			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V, V_S = ±18 V, −40°C ≤ T_A ≤ +125°C, R_L = ∞			30			30	μA
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		μV p-p

Parameter	Symbol	Conditions	E Grade Min	E Grade Typ	E Grade Max	F Grade Min	F Grade Typ	F Grade Max	Unit
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		15			15		V/ms
Gain Bandwidth Product	GBP			35			35		kHz
Channel Separation		V_{OUT} = 10 V p-p, R_L = 2 kΩ, f = 1 kHz		120			120		dB

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125 °C, with an LTPD of 1.3.
[2] Offset voltage drift is the average of the −40°C to +25°C delta and the +25°C to +125°C delta.

V_S = 5.0 V, V_{CM} = 0.1 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	E Grade Min	E Grade Typ	E Grade Max	F Grade Min	F Grade Typ	F Grade Max	Unit
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193						150	µV
		OP193, −40°C ≤ T_A ≤ +125°C						250	µV
		OP293			100			250	µV
		OP293, −40°C ≤ T_A ≤ +125°C			200			350	µV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		0		4	0		4	V
Common-Mode Rejection	CMRR	0.1 V ≤ V_{CM} ≤ 4 V	100	116		96	116		dB
		0.1 V ≤ V_{CM} ≤ 4 V, −40°C ≤ T_A ≤ +125°C	92			92			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,							
		0.03 V ≤ V_{OUT} ≤ 4.0 V	200			200			V/mV
		−40°C ≤ T_A ≤ +85°C	125			125			V/mV
		−40°C ≤ T_A ≤ +125°C		130			130		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ,							
		0.03 V ≤ V_{OUT} ≤ 4.0 V	75			75			V/mV
		−40°C ≤ T_A ≤ +85°C	50			50			V/mV
		−40°C ≤ T_A ≤ +125°C		70			70		V/mV
Long-Term Offset Voltage[1]	V_{OS}				150			300	µV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$			0.2	1.25				µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 100 µA		4.4			4.4		V
		I_L = 1 mA	4.1	4.4		4.1	4.4		V
		I_L = 1 mA, −40°C ≤ T_A ≤ +125°C	4.0			4.0			V
		I_L = 5 mA	3.9	4.4		3.9	4.4		V
Output Voltage Swing Low	V_{OL}	I_L = −100 µA		140	160		140	160	mV
		I_L = −100 µA, −40°C ≤ T_A ≤ +125°C			220			220	mV
		No load		5			5		mV
		I_L = −1 mA		280	400		280	400	mV
		I_L = −1 mA, −40°C ≤ T_A ≤ +125°C			500			500	mV
		I_L = −5 mA		700	900		700	900	mV
Short-Circuit Current	I_{SC}			±8			±8		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±1.7 V to ±6.0 V	100	120		97	120		dB
		−40°C ≤ T_A ≤ +125°C	94			90			dB
Supply Current per Amplifier	I_{SY}	V_{CM} = 2.5 V, R_L = ∞		14.5			14.5		µA

Parameter	Symbol	Conditions	E Grade			F Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		µV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		12			12		V/ms
Gain Bandwidth Product	GBP			35			35		kHz

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125 °C, with an LTPD of 1.3.
[2] Offset voltage drift is the average of the −40°C to +25°C delta and the +25°C to +125°C delta.

V_S = 3.0 V, V_{CM} = 0.1 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	E Grade			F Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193						150	μV
		OP193, −40°C ≤ T_A ≤ +125°C						250	μV
		OP293			100			250	μV
		OP293, −40°C ≤ T_A ≤ +125°C			200			350	μV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		0		2	0		2	V
Common-Mode Rejection	CMRR	0.1 ≤ V_{CM} ≤ 2 V	97	116		94	116		dB
		0.1 ≤ V_{CM} ≤ 2 V, −40°C ≤ T_A ≤ +125°C	90			87			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,							
		0.03 V ≤ V_{OUT} ≤ 2 V	100			100			V/mV
		−40°C ≤ T_A ≤ +85°C	75			75			V/mV
		−40°C ≤ T_A ≤ +125°C		100			100		V/mV
Long-Term Offset Voltage[1]	V_{OS}				150			300	μV
Offset Voltage Drift[2]	$\Delta V_{OS}/\Delta T$			0.2	1.25				μV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 1 mA	2.1	2.14		2.1	2.14		V
		I_L = 1 mA, −40°C ≤ T_A ≤ +125°C	1.9			1.9			V
		I_L = 5 mA	1.9	2.1		1.9	2.1		V
Output Voltage Swing Low	V_{OL}	I_L = −1 mA		280	400		280	400	mV
		I_L = −1 mA, −40°C ≤ T_A ≤ +125°C			500			500	mV
		I_L = −5 mA		700	900		700	900	mV
Short-Circuit Current	I_{SC}			±8			±8		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = +1.7 V to +6 V	100			97			dB
		−40°C ≤ T_A ≤ +125°C	94			90			dB
Supply Current per Amplifier	I_{SY}	V_{CM} = 1.5 V, R_L = ∞		14.5	22		14.5	22	μA
		−40°C ≤ T_A ≤ +125°C			22			22	μA
Supply Voltage Range	V_S		+2		±18	+2		±18	V
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		μV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		10			10		V/ms
Gain Bandwidth Product	GBP			25			25		kHz
Channel Separation		V_{OUT} = 10 V p-p, R_L = 2 kΩ, f = 1 kHz		120			120		dB

[1] Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 125 °C, with an LTPD of 1.3.
[2] Offset voltage drift is the average of the −40°C to +25°C delta and the +25°C to +125°C delta.

V_S = 2.0 V, V_{CM} = 0.1 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	E Grade			F Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193						150	μV
		OP193, −40°C ≤ T_A ≤ +125°C						250	μV
		OP293			100			250	μV
		OP293, −40°C ≤ T_A ≤ +125°C			175			350	μV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		0		1	0		1	V
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,							
		0.03 V ≤ V_{OUT} ≤ 1 V	60			60			V/mV
		−40°C ≤ T_A ≤ +125°C		70			70		V/mV
Long-Term Offset Voltage	V_{OS}				150			300	μV
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = 1.7 V to 6 V	100			97			dB
		−40°C ≤ T_A ≤ +125°C	94			90			dB
Supply Current/Amplifier	I_{SY}	V_{CM} = 1.0 V, R_L = ∞		13.2	20		13.2	20	μA
		−40°C ≤ T_A ≤ +125°C			25			25	μA
Supply Voltage Range	V_S		+2		±18	+2		±18	V
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		μV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		10			25		V/ms
Gain Bandwidth Product	GBP			25					kHz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage[1]	±18 V
Input Voltage[1]	±18 V
Differential Input Voltage[1]	±18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±18 V, the input voltage is limited to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC_N (S)	158	43	°C/W

[1] θ_{JA} is specified for the worst-case conditions. θ_{JA} is specified for a device soldered in a circuit board for the SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

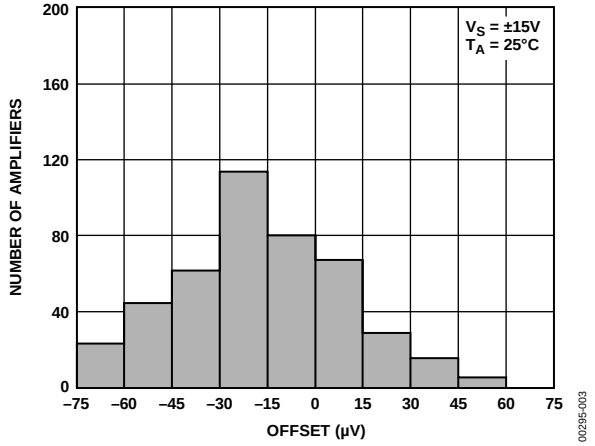

Figure 3. Offset Distribution, V_S = ±15 V

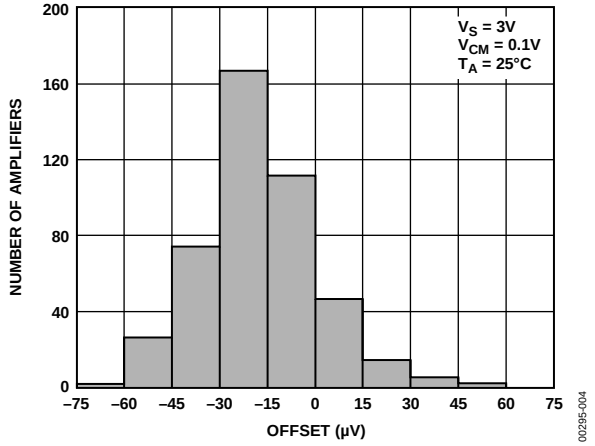

Figure 4. Offset Distribution, V_S = +3 V

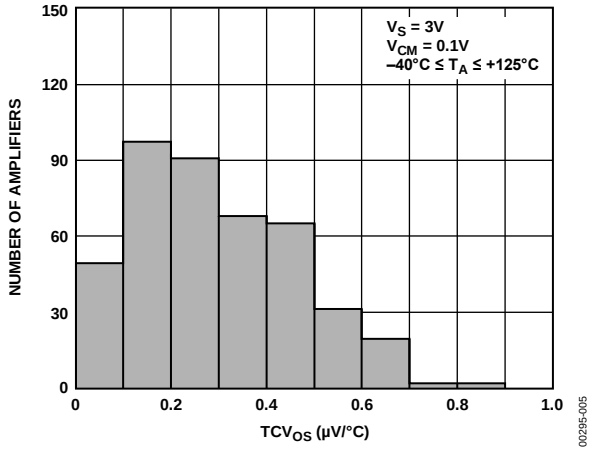

Figure 5. TCV_{OS} Distribution, V_S = +3 V

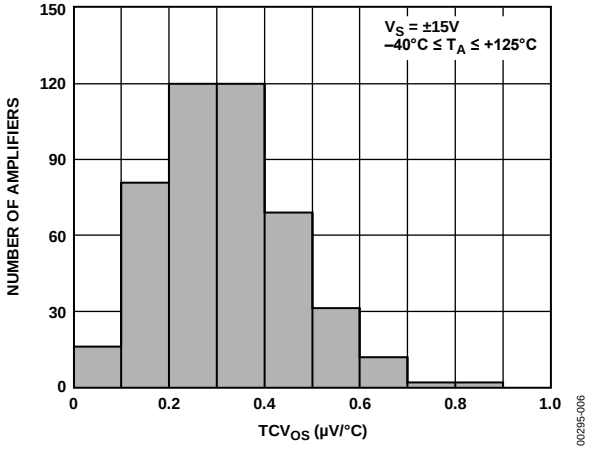

Figure 6. TCV_{OS} Distribution, V_S = ±15 V

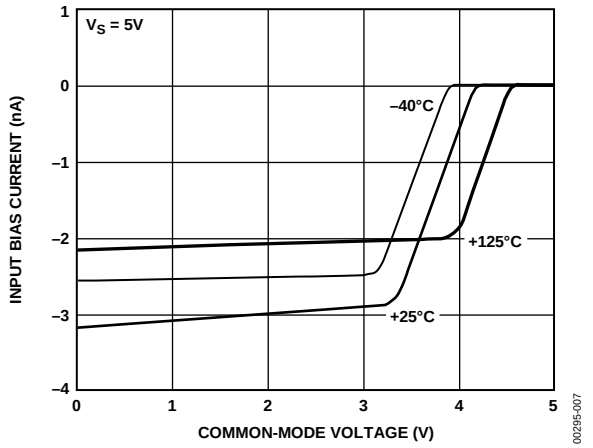

Figure 7. Input Bias Current vs. Common-Mode Voltage

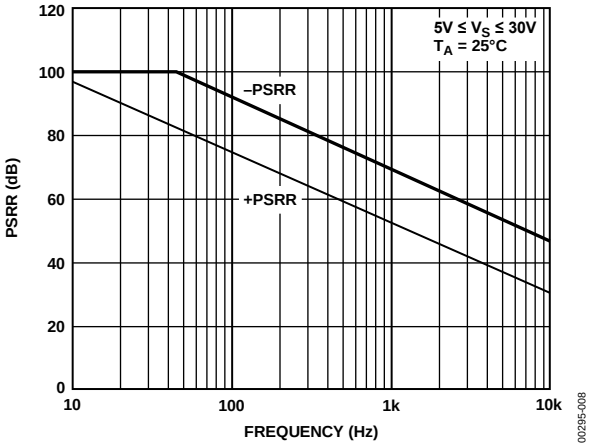

Figure 8. PSRR vs. Frequency

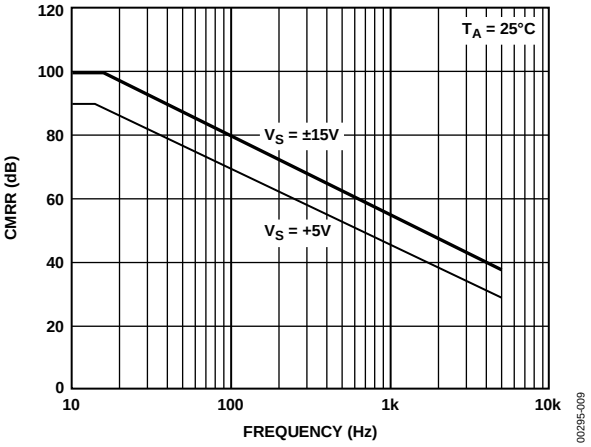

Figure 9. CMRR vs. Frequency

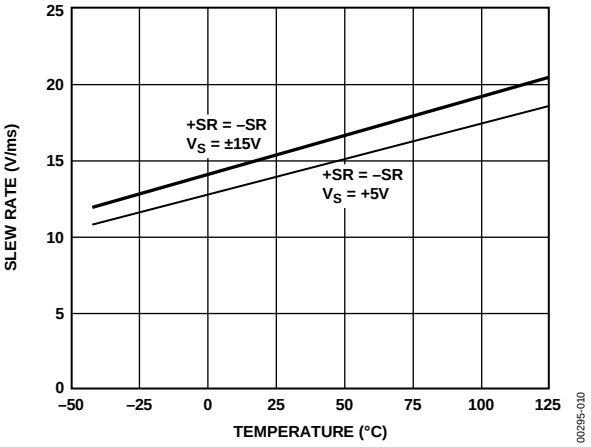

Figure 10. Slew Rate vs. Temperature

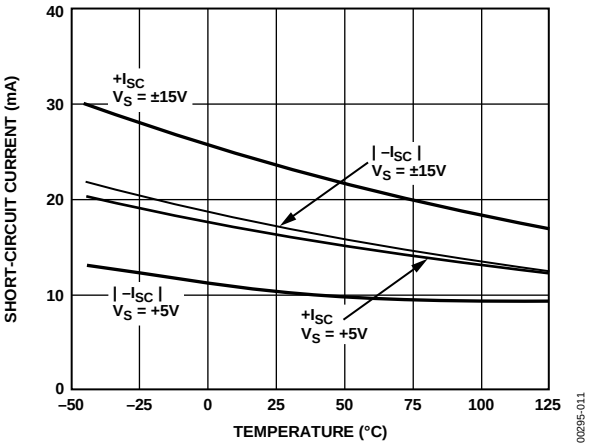

Figure 11. Short-Circuit Current vs. Temperature

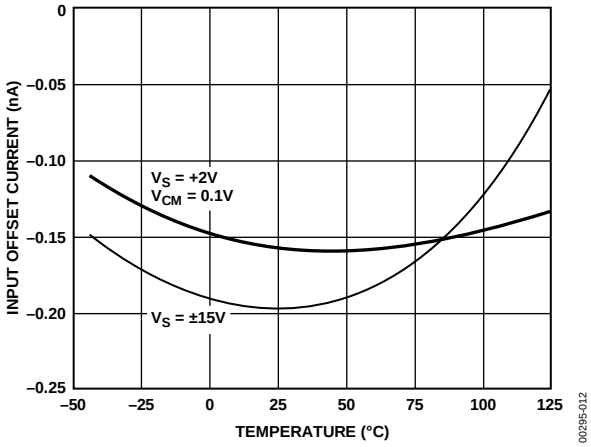

Figure 12. Input Offset Current vs. Temperature

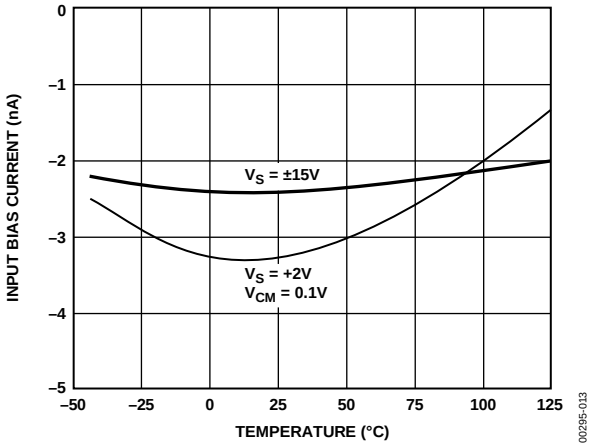

Figure 13. Input Bias Current vs. Temperature

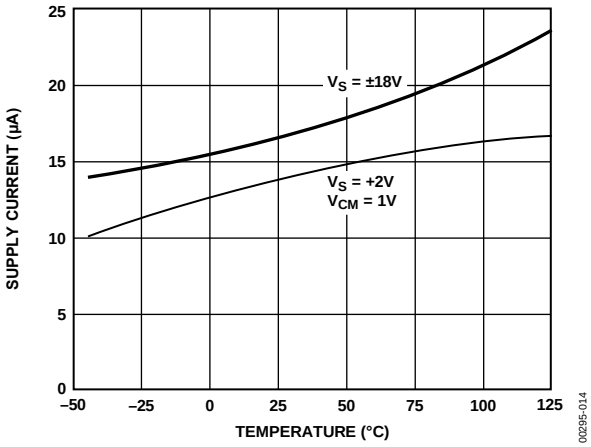

Figure 14. Supply Current vs. Temperature

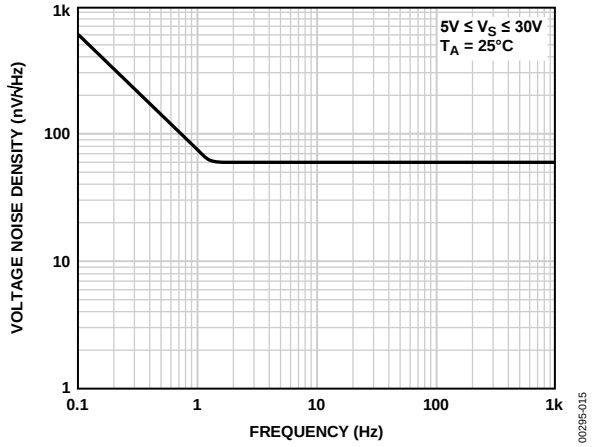

Figure 15. Voltage Noise Density vs. Frequency

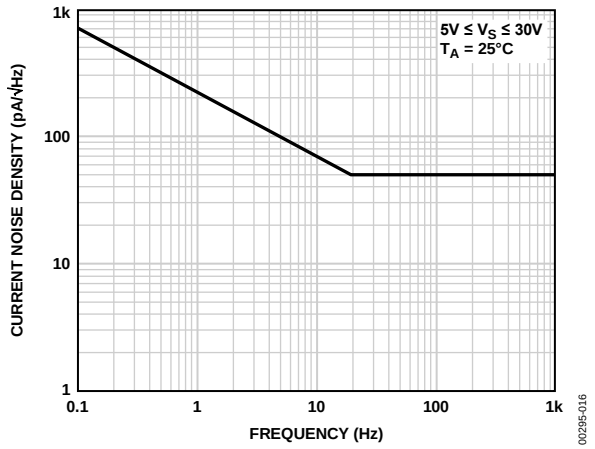

Figure 16. Current Noise Density vs. Frequency

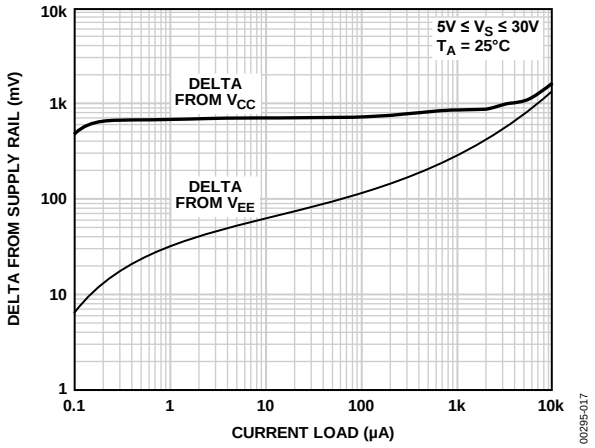

Figure 17. Delta Output Swing vs. Current Load

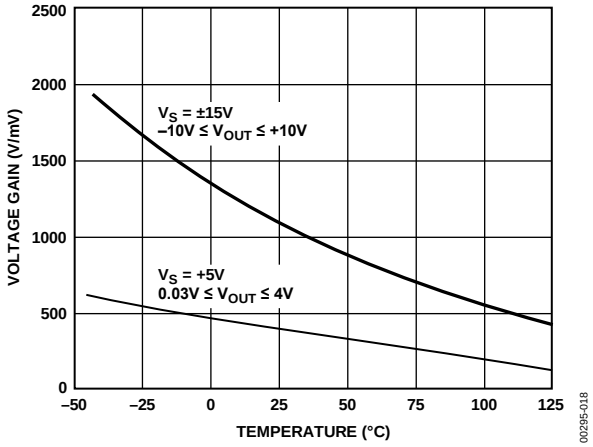

Figure 18. Voltage Gain (R_L = 100 kΩ) vs. Temperature

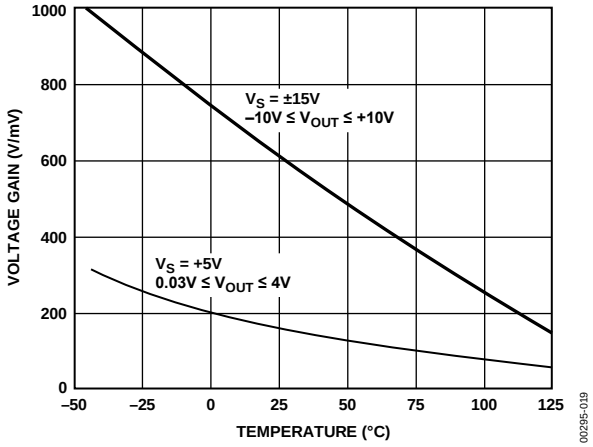

Figure 19. Voltage Gain (R_L = 10 kΩ) vs. Temperature

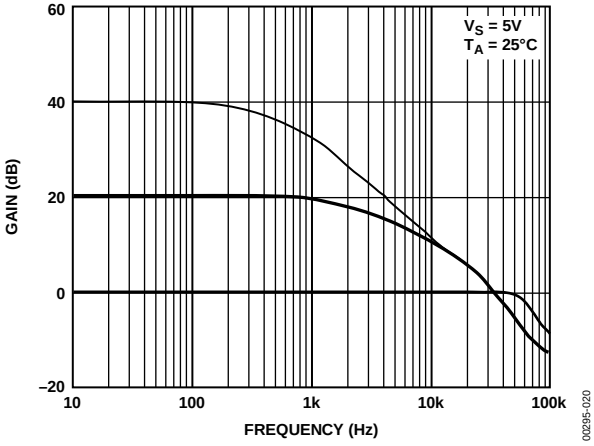

Figure 20. Closed-Loop Gain vs. Frequency, V_S = 5 V

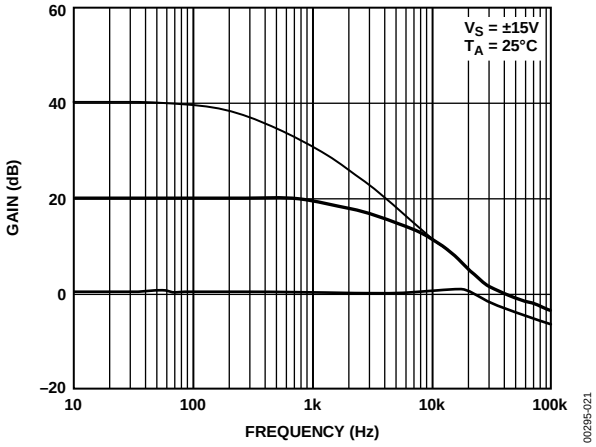

Figure 21. Closed-Loop Gain vs. Frequency, V_S = ±15 V

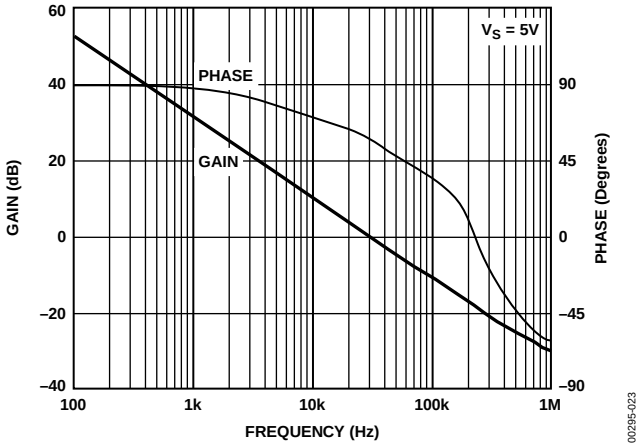

Figure 23. Open-Loop Gain and Phase vs. Frequency

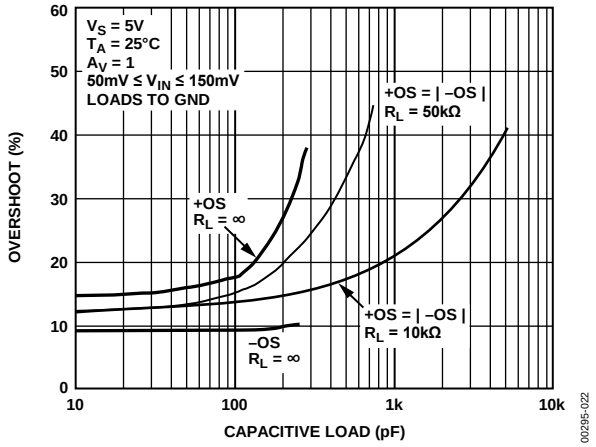

Figure 22. Small Signal Overshoot vs. Capacitive Load

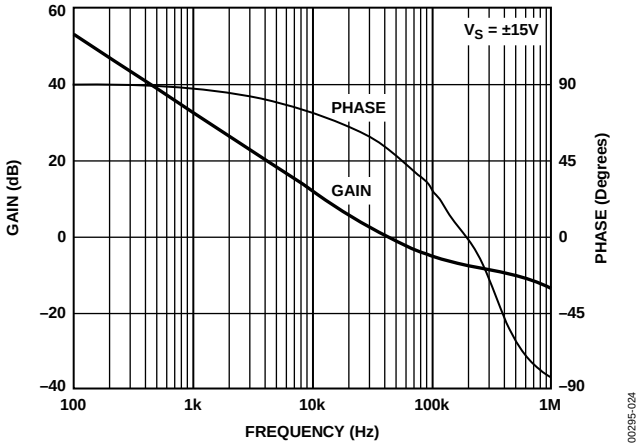

Figure 24. Open-Loop Gain and Phase vs. Frequency

FUNCTIONAL DESCRIPTION

The OP193/OP293 operational amplifiers are single-supply, micropower, precision amplifiers whose input and output ranges both include ground. Input offset voltage (V_{OS}) is only 100 µV maximum, while the output delivers ±5 mA to a load. Supply current is only 15 µA.

A simplified schematic of the input stage is shown in Figure 26. The input transistors, Q1 and Q2, are PNP devices, which permit the inputs to operate down to ground potential. The input transistors have resistors in series with the base terminals to protect the junctions from overvoltage conditions. The second stage is an NPN cascode that is buffered by an emitter follower before driving the final PNP gain stage.

The OP193 includes connections to taps on the input load resistors, which can be used to null the input offset voltage, V_{OS}. The OP293 have two additional transistors, Q7 and Q8. The behavior of these transistors is discussed in the Output Phase Reversal— and Output Phase Reversal— sections.

The output stage, shown in Figure 25, is a noninverting NPN totem-pole configuration. Current is sourced to the load by Emitter Follower Q1, while Q2 provides current sink capability. When Q2 saturates, the output is pulled to within 5 mV of ground without an external pull-down resistor. The totem-pole output stage supplies a minimum of 5 mA to an external load, even when operating from a single 3.0 V power supply.

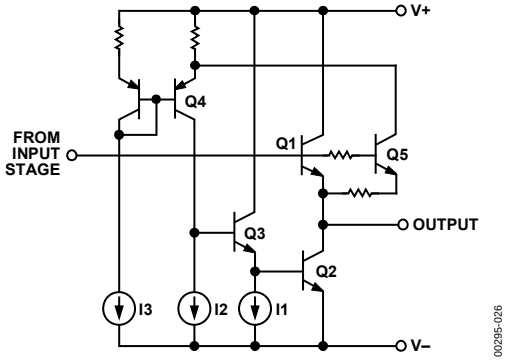

Figure 25. OP193/OP293 Equivalent Output Circuit

By operating as an emitter follower, Q1 offers a high impedance load to the final PNP collector of the input stage. Base drive to Q2 is derived by monitoring Q1's collector current. Transistor Q5 tracks the collector current of Q1. When Q1 is on, Q5 keeps Q4 off, and Current Source I1 keeps Q2 turned off. When Q1 is driven to cutoff (that is, the output must move toward V−), Q5 allows Q4 to turn on. Q4's collector current then provides the base drive for Q3 and Q2, and the output low voltage swing is set by Q2's $V_{CE,SAT}$, which is about 5 mV.

DRIVING CAPACITIVE LOADS

The OP193/OP293 amplifiers are unconditionally stable with capacitive loads less than 200 pF. However, the small signal, unity-gain overshoot improves if a resistive load is added. For example, transient overshoot is 20% when driving a 1000 pF, 10 kΩ load. When driving large capacitive loads in unity-gain configurations, an in-the-loop compensation technique is recommended, as illustrated in Figure 30.

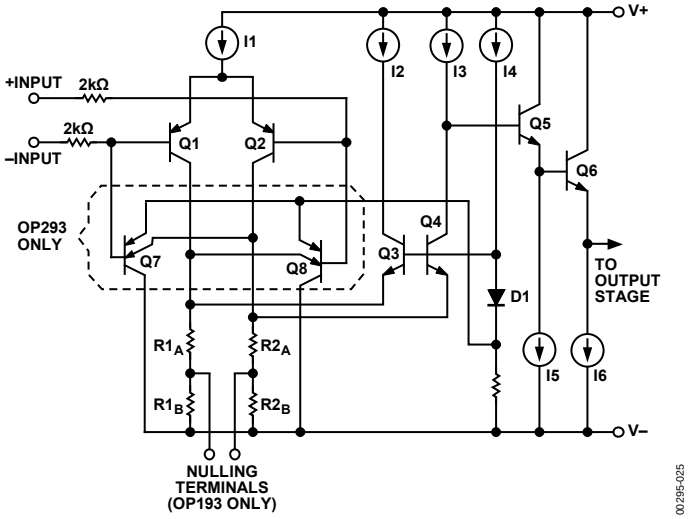

Figure 26. OP193/OP293 Equivalent Input Circuit

INPUT OVERVOLTAGE PROTECTION

As previously mentioned, the OP193/OP293 op amps use a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors, coupled with the protection resistors, provides a large amount of input protection from overvoltage conditions. The inputs can therefore be taken 20 V beyond either supply without damaging the amplifier.

OUTPUT PHASE REVERSAL—OP193

The OP193's input PNP collector-base junction can be forward-biased if the inputs are brought more than one diode drop (0.7 V) below ground. When this happens to the noninverting input, Q4 of the cascode stage turns on and the output goes high. If the positive input signal can go below ground, phase reversal can be prevented by clamping the input to the negative supply (that is, GND) with a diode. The reverse leakage of the diode does add to the input bias current of the amplifier. If input bias current is not critical, a 1N914 diode adds less than 10 nA of leakage. However, its leakage current doubles for every 10°C increase in ambient temperature. For critical applications, the collector-base junction of a 2N3906 transistor adds only about 10 pA of additional bias current. To limit the current through the diode under fault conditions, a 1 kΩ resistor is recommended in series with the input. (The OP193's internal current limiting resistors do not protect the external diode.)

OUTPUT PHASE REVERSAL—OP293

The OP293 includes two lateral PNP transistors, Q7 and Q8, to protect against phase reversal. If an input is brought more than one diode drop (≈0.7 V) below ground, Q7 and Q8 combine to level shift the entire cascode stage, including the bias to Q3 and Q4, simultaneously. In this case, Q4 does not saturate and the output remains low.

The OP293 does not exhibit output phase reversal for inputs up to −5 V below V− at +25°C. The phase reversal limit at +125°C is about −3 V. If the inputs can be driven below these levels, an external clamp diode, as discussed in the previous section, should be added.

BATTERY-POWERED APPLICATIONS

OP193/OP293 series op amps can be operated on a minimum supply voltage of 1.7 V, and draw only 13 µA of supply current per amplifier from a 2.0 V supply. In many battery-powered circuits, OP193/OP293 devices can be continuously operated for thousands of hours before requiring battery replacement, thus reducing equipment downtime and operating cost.

High performance portable equipment and instruments frequently use lithium cells because of their long shelf life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3 V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP193/OP293, combined with the flat discharge characteristic of the lithium cell, indicates that the OP193/OP293 can be operated over the entire useful life of the cell. Figure 27 shows the typical discharge characteristic of a 1 Ah lithium cell powering the OP193 and OP293, with each amplifier, in turn, driving 2.1 V into a 100 kΩ load.

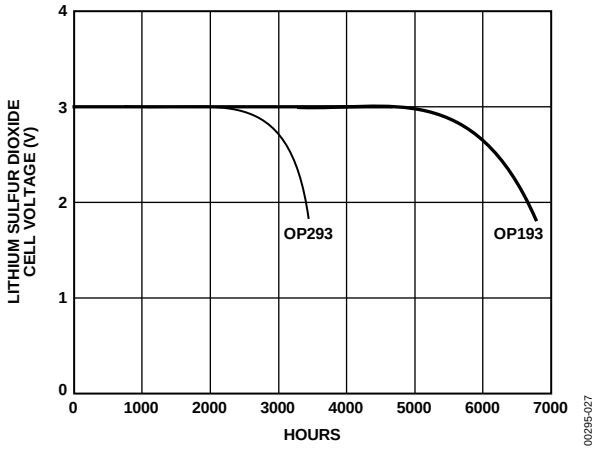

Figure 27. Lithium Sulfur Dioxide Cell Discharge Characteristic with OP193/OP293 and 100 kΩ Loads Input Offset Voltage Nulling

The OP193 provides two offset nulling terminals that can be used to adjust the OP193's internal V_{OS}. In general, operational amplifier terminals should never be used to adjust system offset voltages. The offset nulling circuit of Figure 28 provides about ±7 mV of offset adjustment range. A 100 kΩ resistor placed in series with the wiper arm of the offset null potentiometer, as shown in Figure 29, reduces the offset adjustment range to 400 µV and is recommended for applications requiring high null resolution. Offset nulling does not adversely affect TCV_{OS} performance, providing that the trimming potentiometer temperature coefficient does not exceed ±100 ppm/°C.

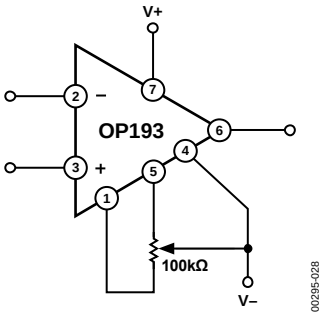

Figure 28. Offset Nulling Circuit

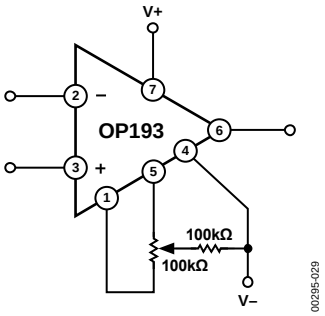

Figure 29. High Resolution Offset Nulling Circuit

A MICROPOWER FALSE-GROUND GENERATOR

Some single-supply circuits work best when inputs are biased above ground, typically at ½ of the supply voltage. In these cases, a false ground can be created by using a voltage divider buffered by an amplifier. One such circuit is shown in Figure 30.

This circuit generates a false-ground reference at ½ of the supply voltage, while drawing only about 27 µA from a 5 V supply. The circuit includes compensation to allow for a 1 µF bypass capacitor at the false-ground output. The benefit of a large capacitor is that not only does the false ground present a very low dc resistance to the load, but its ac impedance is low as well. The OP193 can both sink and source more than 5 mA, which improves recovery time from transients in the load current.

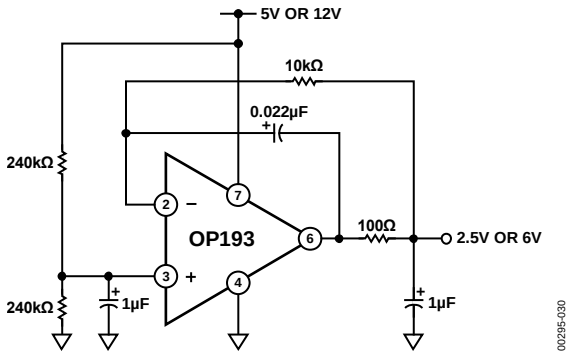

Figure 30. A Micropower False-Ground Generator

A BATTERY-POWERED VOLTAGE REFERENCE

The circuit of Figure 31 is a battery-powered voltage reference that draws only 17 µA of supply current. At this level, two AA alkaline cells can power this reference for more than 18 months. At an output voltage of 1.23 V at 25°C, drift of the reference is only 5.5 µV/°C over the industrial temperature range. Load regulation is 85 µV/mA with line regulation at 120 µV/V.

Design of the reference is based on the Brokaw band gap core technique. Scaling of Resistor R1 and Resistor R2 produces unequal currents in Q1 and Q2. The resulting ΔV_{BE} across R3 creates a temperature-proportional voltage (PTAT), which, in turn, produces a larger temperature-proportional voltage across R4 and R5, V1. The temperature coefficient of V1 cancels (first order) the complementary to absolute temperature (CTAT) coefficient of V_{BE1}. When adjusted to 1.23 V at 25°C, output voltage temperature coefficient is at a minimum. Band gap references can have start-up problems. With no current in R1 and R2, the OP193 is beyond its positive input range limit and has an undefined output state. Shorting Pin 5 (an offset adjust pin) to ground forces the output high under these circumstances and ensures reliable startup without significantly degrading the OP193's offset drift.

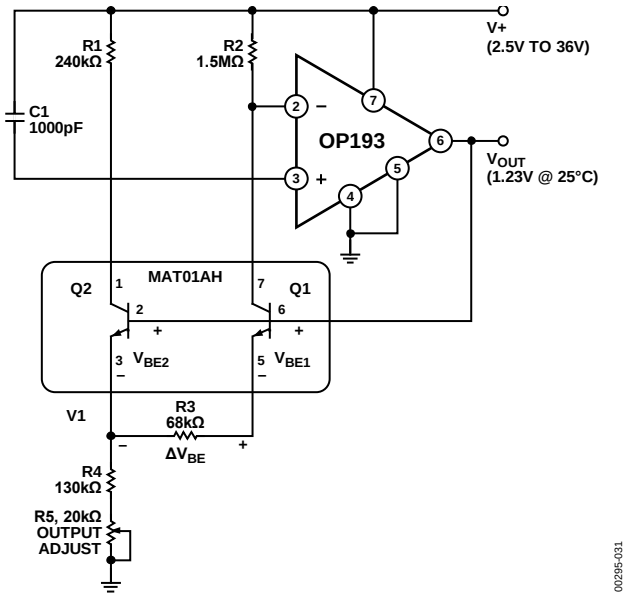

Figure 31. A Battery-Powered Voltage Reference

A SINGLE-SUPPLY CURRENT MONITOR

Current monitoring essentially consists of amplifying the voltage drop across a resistor placed in series with the current to be measured. The difficulty is that only small voltage drops can be tolerated, and with low precision op amps, this greatly limits the overall resolution. The single-supply current monitor of Figure 32 has a resolution of 10 µA and is capable of monitoring 30 mA of current. This range can be adjusted by changing the current sense resistor, R1. When measuring total system current, it may be necessary to include the supply current of the current monitor, which bypasses the current sense resistor, in the final result. This current can be measured and calibrated (together with the residual offset) by adjustment of the offset trim potentiometer, R2. This produces a deliberate temperature dependent offset. However, the supply current of the OP193 is also proportional to temperature, and the two effects tend to track. Voltage developed at the noninverting input and amplified by (1 + R4/R5) appears at V_{OUT}.

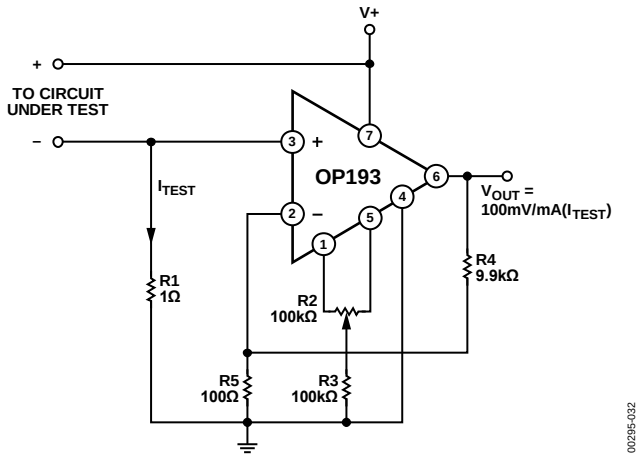

Figure 32. Single-Supply Current Monitor

A SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

Designing a true single-supply instrumentation amplifier with zero-input and zero-output operation requires special care. The traditional configuration, shown in Figure 33, depends upon Amplifier A1's output being at 0 V when the applied common-mode input voltage is at 0 V. Any error at the output is multiplied by the gain of A2. In addition, current flows through Resistor R3 as A2's output voltage increases. A1's output must remain at 0 V while sinking the current through R3, or a gain error results. With a maximum output voltage of 4 V, the current through R3 is only 2 µA, but this still produces an appreciable error.

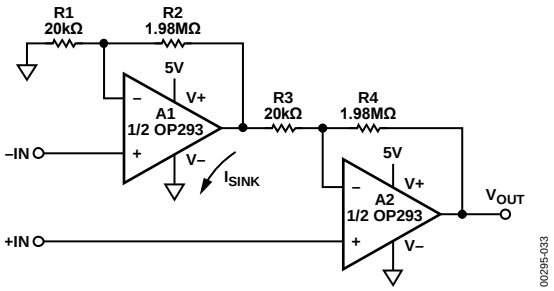

Figure 33. A Conventional Instrumentation Amplifier

One solution to this problem is to use a pull-down resistor. For example, if R3 = 20 kΩ, then the pull-down resistor must be less than 400 Ω. However, the pull-down resistor appears as a fixed load when a common-mode voltage is applied. With a 4 V common-mode voltage, the additional load current is 10 mA, which is unacceptable in a low power application.

Figure 34 shows a better solution. A1's sink current is provided by a pair of N-channel FET transistors, configured as a current mirror. With the values shown, the sink current of Q2 is about 340 µA. Thus, with a common-mode voltage of 4 V, the additional load current is limited to 340 µA vs. 10 mA with a 400 Ω resistor.

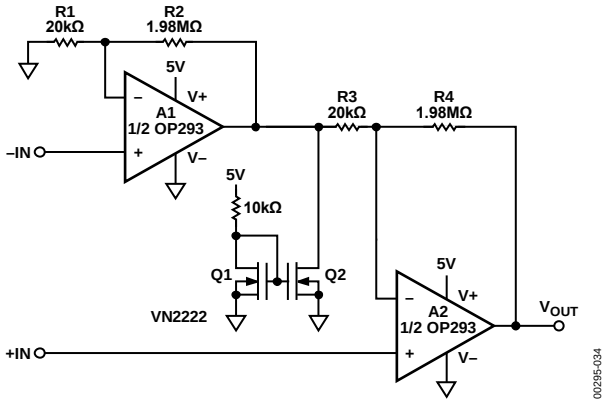

Figure 34. An Improved Single-Supply, 0 V_{IN}, 0 V_{OUT} Instrumentation Amplifier

A LOW POWER, TEMPERATURE TO 4 mA TO 20 mA TRANSMITTER

A simple temperature to 4 mA to 20 mA transmitter is shown in Figure 35. After calibration, this transmitter is accurate to ±0.5°C over the −50°C to +150°C temperature range. The transmitter operates from 8 V to 40 V with supply rejection better than 3 ppm/V. One half of the OP293 is used to buffer the TEMP pin, and the other half regulates the output current to satisfy the current summation at its noninverting input.

$$I_{OUT} + \frac{V_{TEMP} \times (R6 + R7)}{R2 \times R10} - V_{SET}\left(\frac{R2 + R6 + R7}{R2 \times R10}\right)$$

The change in output current with temperature is the derivative of the following transfer function:

$$\frac{\Delta I_{OUT}}{\Delta T} = \frac{\frac{\Delta V_{TEMP}}{\Delta T}(R6 + R7)}{R2 \times R10}$$

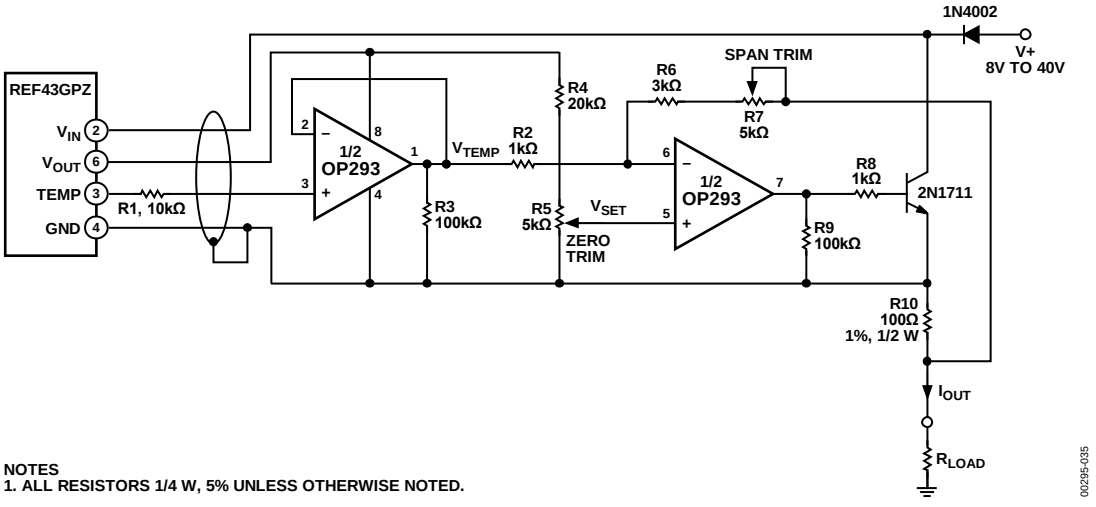

Figure 35. Temperature to 4 mA to 20 mA Transmitter

From the formulas, it can be seen that if the span trim is adjusted before the zero trim, the two trims are not interactive, which greatly simplifies the calibration procedure.

Calibration of the transmitter is simple. First, the slope of the output current vs. temperature is calibrated by adjusting the span trim, R7. A couple of iterations may be required to be sure the slope is correct.

When the span trim has been adjusted, the zero trim can be made. Adjusting the zero trim does not affect the gain.

The zero trim can be set at any known temperature by adjusting R5 until the output current equals:

$$I_{OUT} = \left(\frac{\Delta I_{FS}}{\Delta T_{OPERATING}}\right)\left(T_{AMBIENT} - T_{MIN}\right) + 4\text{ mA}$$

Table 7 shows the values of R6 required for various temperature ranges.

Table 7. R6 Values vs. Temperature

Temp Range	R6
0°C to 70°C	10 kΩ
−40°C to +85°C	6.2 kΩ
−55°C to +150°C	3 kΩ

A MICROPOWER VOLTAGE CONTROLLED OSCILLATOR

The OP293 CMOS analog switch forms the precision VCO of Figure 36. This circuit provides triangle and square wave outputs and draws only 50 µA from a single 5 V supply. A1 acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by A2, which acts as a Schmitt trigger with a precise hysteresis of 1.67 V, set by Resistor R5, Resistor R6, and Resistor R7, and associated CMOS switches. The resulting output of A1 is a triangle wave with upper and lower levels of 3.33 V and 1.67 V. The output of A2 is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}\text{ V} \times 10\text{ Hz/V}$$

However, the frequency can easily be changed by varying C1. The circuit operates well up to 500 Hz.

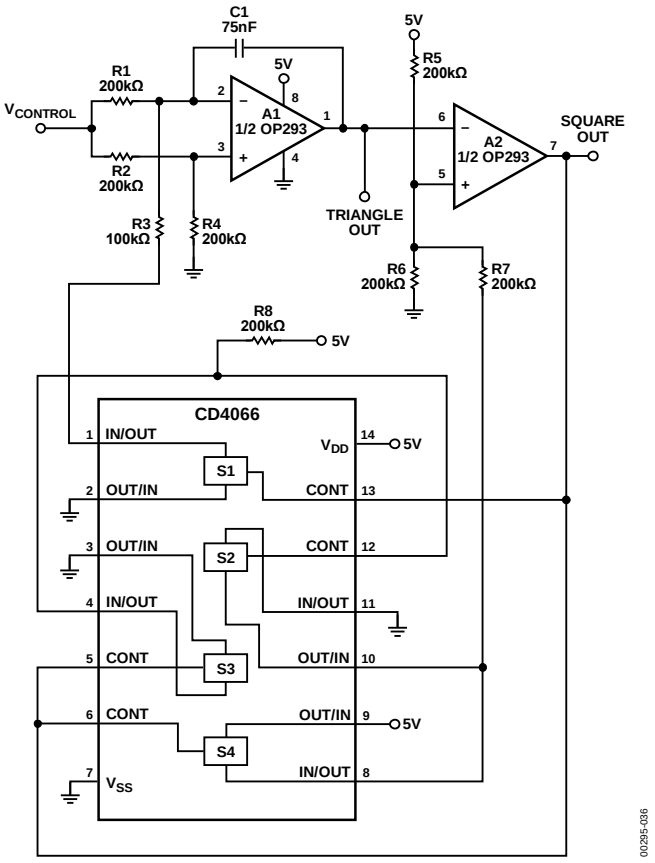

Figure 36. Micropower Voltage Controlled Oscillator

OUTLINE DIMENSIONS

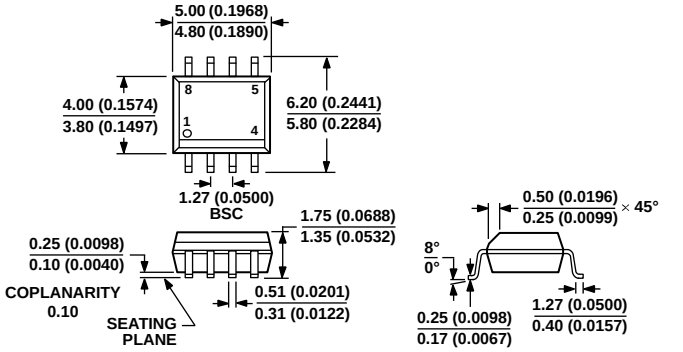

Figure 37. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP193FS-REEL	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP193FSZ	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP193FSZ-REEL	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP193FSZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293ESZ	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293ESZ-REEL	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293ESZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293FSZ	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293FSZ-REEL	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)
OP293FSZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	S-Suffix (R-8)

[1] Z = RoHS Compliant Part.

NOTES

NOTES