Description

The 1giga bit (1Gb) Double-Data-Rate-2 (DDR2) DRAMs is a high-speed CMOS Double Data Rate 2 SDRAM containing 1,073,741,824 bits. It is internally configured as an octal-bank DRAM.

The 1Gb chip is organized as 32Mbit x 4 I/O x 8 bank, 16Mbit x 8 I/O x 8 bank or 8Mbit x 16 I/O x 8 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1066 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR2 DRAM key features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) normal and weak strength data-output driver, (4) variable data-output impedance adjustment and (5) an ODT (On-Die Termination) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion. A 13 bit address bus for x4/x8 organized components and A 12 bit address bus for x16 component is used to convey row, column, and bank address devices.

These devices operate with a single 1.8V ± 0.1V power supply and are available in BGA packages.

Pin Configuration – 60 balls BGA Package (x4)

< TOP View>

See the balls through the package

X 4

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{DQS}$	VDDQ
NC6	VSSQ	DM	B	DQS	VSSQ	NC
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
NC	VSSQ	DQ3	D	DQ2	VSSQ	NC
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	$\overline{WE}$	F	$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA 1	G	$\overline{CAS}$	$\overline{CS}$	
	A10/ AP	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Pin Configuration – 60 balls BGA Package (x8)

< TOP View>

See the balls through the package

X 8

1	2	3		7	8	9
VDD	NU,/RDQS	VSS	A	VSSQ	DQS	VDDQ
DQ6	VSSQ	DM/RDQS	B	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	C	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	D	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	E	VSSDL	CK	VDD
	CKE	WE	F	RAS	CK	ODT
BA2	BA0	BA 1	G	CAS	CS	
	A10/ AP	A1	H	A2	A0	VDD
VSS	A3	A5	J	A6	A4	
	A7	A9	K	A11	A8	VSS
VDD	A12	NC	L	NC	A13	

Pin Configuration – 84 balls BGA Package (x16)

< TOP View>

See the balls through the package

x 16

1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA 1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/ AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

Input / Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must maintain to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, LDM, UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS / $\overline{RQDS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0, BA1, and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 – A13	Input	**Address Inputs:** Provides the row address for Activate commands and the column address and Auto Precharge or Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA0-BA2. The address inputs also provide the op-code during Mode Register Set commands.A13 Row address use on x8 components only.
DQ	Input/output	**Data Inputs/Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) LDQS, ($\overline{LDQS}$), UDQS,($\overline{UDQS}$)	Input/output	**Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on DQ0 - DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with the optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals.

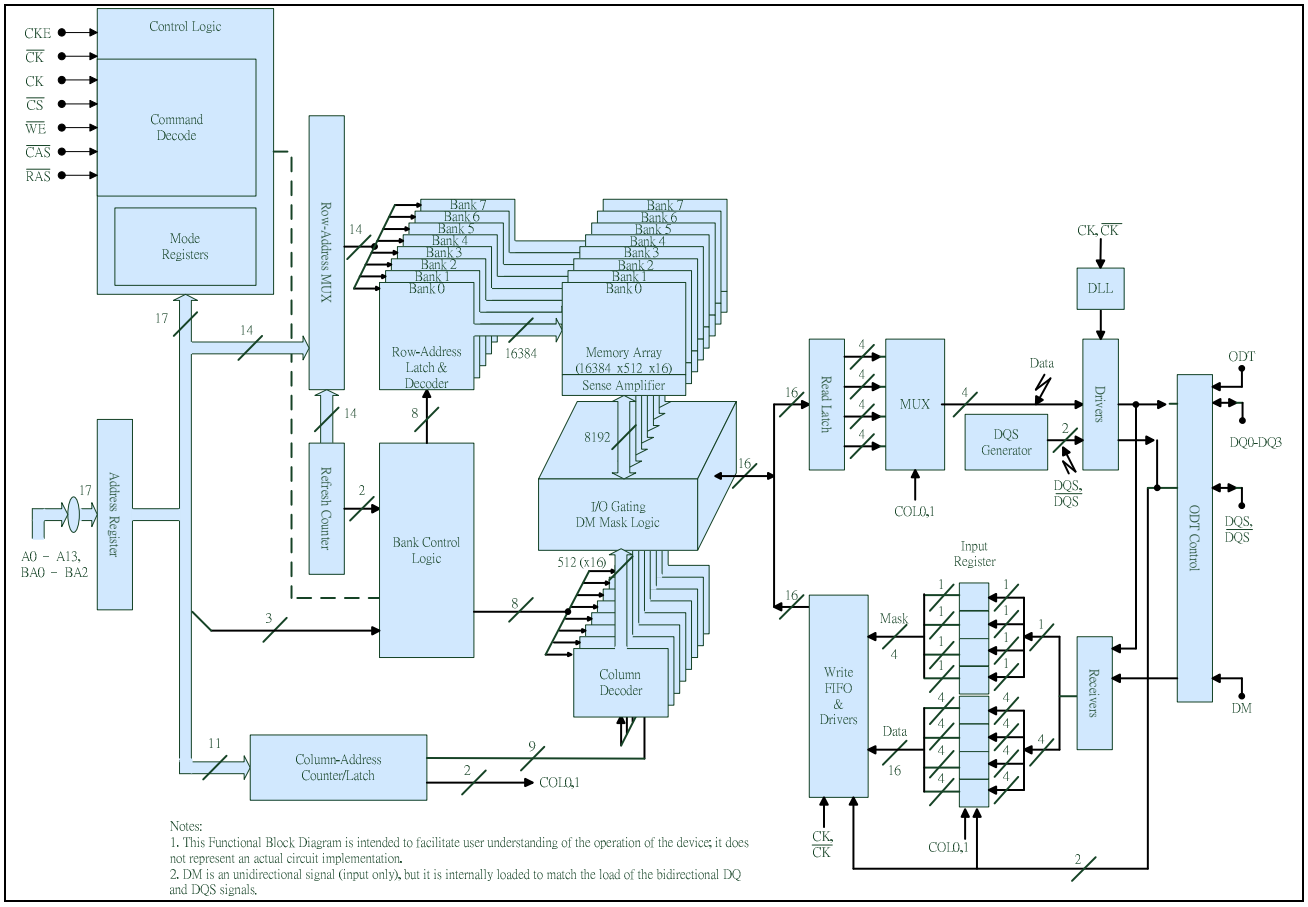
Symbol	Type	Function
RDQS, ($\overline{\text{RDQS}}$)	Input/output	**Read Data Strobe:** For x8 components a RDQS and $\overline{\text{RDQS}}$ pair can be enabled via EMRS(1) for real timing. RDQS and $\overline{\text{RDQS}}$ is not support x16 components. RDQS and $\overline{\text{RDQS}}$ are edge-aligned with real data. If enable RDQS and $\overline{\text{RDQS}}$ then DM function will be disabled.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$, and DM signal for x8 configuration. For x16 configuration ODT is applied to each DQ, UDQS, $\overline{\text{UDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDM and LDM signal. The ODT pin will be ignored if the EMRS (1) is programmed to disable ODT.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V ± 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V ± 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V ± 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_1.8 reference voltage**

Ordering Information

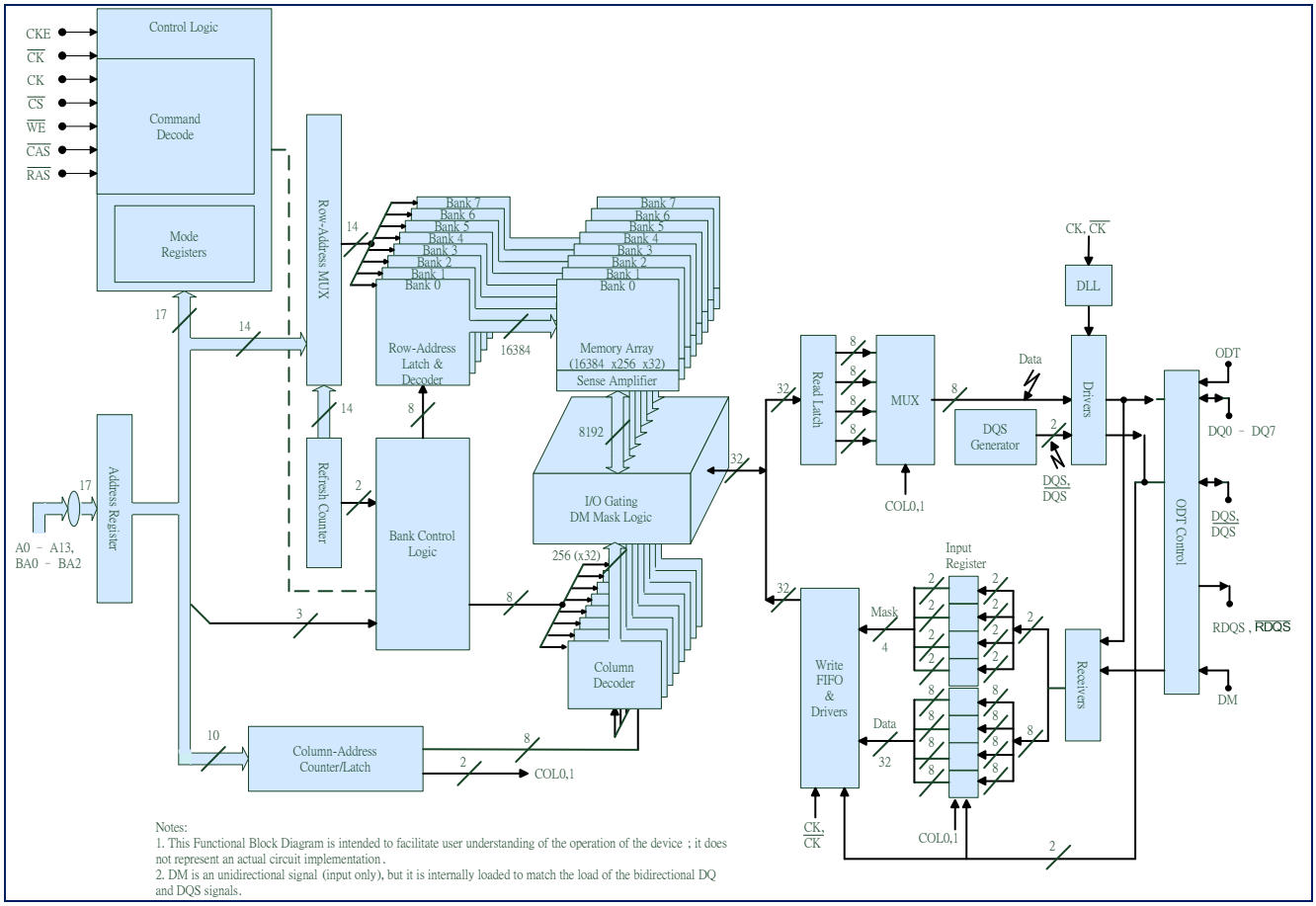
Green

Standard Grade				
Organization	Part Number	Package	Speed	
			Clock (MHz)	CL-T_{RCD}-T_{RP}
	NT5TU256M4GE – 3C	60-Ball BGA	333	5-5-5
	NT5TU256M4GE – AC		400	5-5-5
	NT5TU128M8GE – 3C		333	5-5-5
	NT5TU128M8GE – AC		400	5-5-5
	NT5TU128M8GE – BD		533	6-6-6
	NT5TU64M16GG – 3C	84-Ball BGA	333	5-5-5
	NT5TU64M16GG – AC		400	5-5-5
	NT5TU64M16GG – BD		533	6-6-6
Industrial Grade				
Organization	Part Number	Package	Speed	
			Clock (MHz)	CL-T_{RCD}-T_{RP}
	NT5TU128M8GE – 3CI	60-Ball BGA	333	5-5-5
	NT5TU128M8GE – ACI		400	5-5-5
	NT5TU64M16GG – 3CI	84-Ball BGA	333	5-5-5
	NT5TU64M16GG – ACI		400	5-5-5

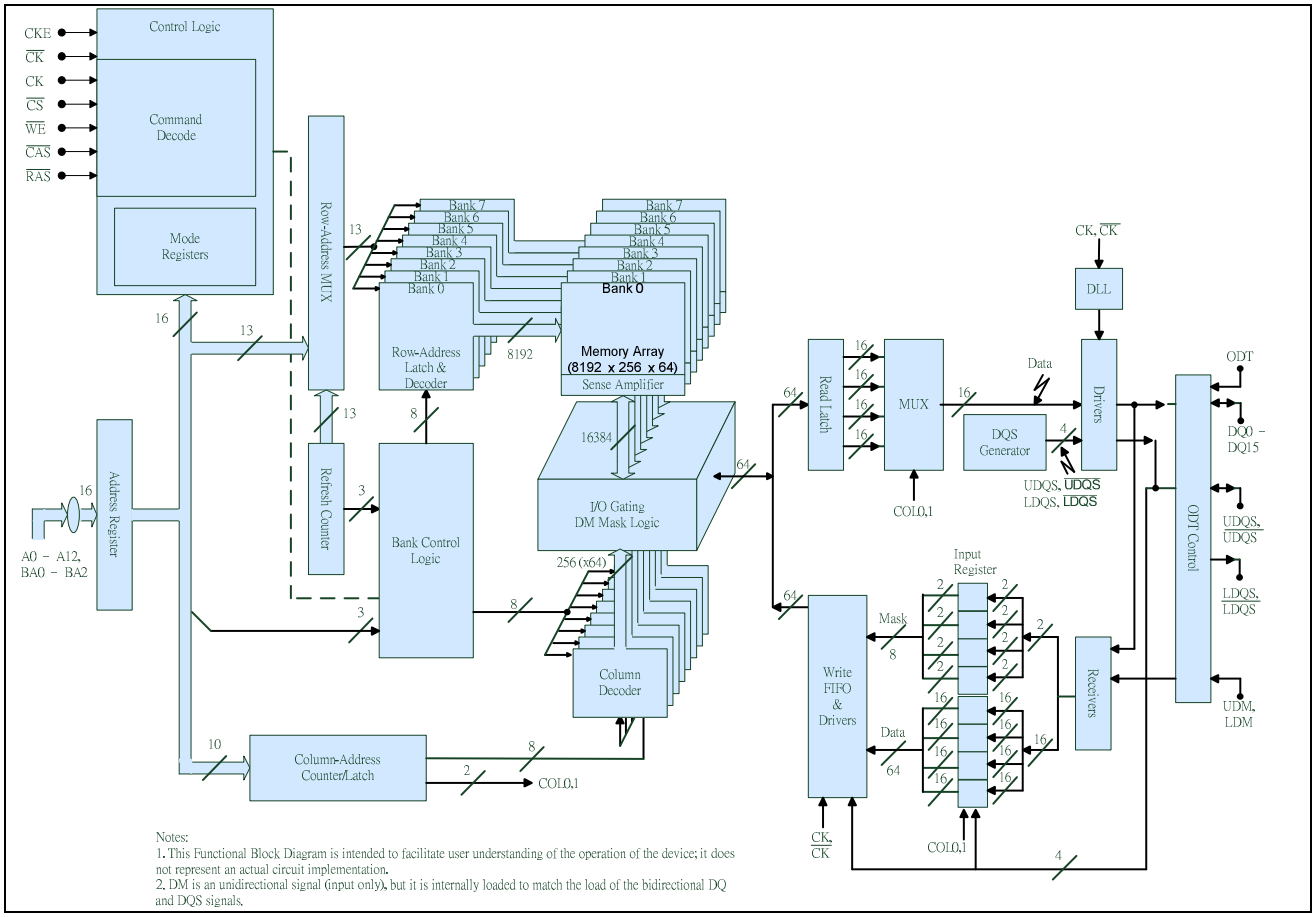
Block Diagram (256Mb x 4)



Block Diagram (128Mb x 8)



Block Diagram (64Mb x 16)



Functional Description

The 1Gb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The 1Gb DDR SDRAM is internally configured as a octal-bank DRAM.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accesses (BA0, BA1, & BA2 select the banks, A0-A13 select the row for x4 and x8 components, A0-A12 select the row for x16 components). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for POWER UP and Initialization.

1. Either one of the following sequence is required for Power-up.

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state (all other inputs may be undefined) The VDD voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDD min; and during the VDD voltage ramp up, IVDD-VDDQI≦0.3 volts. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ min), the supply voltage specifications in Re-commanded DC operating conditions table.

- VDD, VDDL, and VDDQ are driven from a signal power converter output, AND
- VTT is limited to 0.95V max, AND
- Vref tracks VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.
- VDDQ>=VREF must be met at all times.

While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT at a Low state, all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD≧VDDL≧VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in Re-commanded DC operating conditions table.

- Apply VDD/VDDL before or at the same time as VDDQ.
- VDD/VDDL voltage ramp time must be no greater than 200ms from when VDD ramps from 300mV to VDDmin.
- Apply VDDQ before or at the same time as VTT.

- The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500ms. (Note: While VDD is ramping, current may be supplied from VDD through the DRAM to VDDQ.)
- Vref must track VDDQ/2; Vref must be within ±300mV with respect to VDDQ/2 during supply ramp time.
- VDDQ ≧ VREF must be met at all time.
- Apply VTT.

2. Start clock (CK, $\overline{CK}$) and maintain stable condition.

3. For the minimum of 200us after stable power (VDD, VDDL, VDDQ, VREF, and VTT are between their minimum and maximum values as stated in Re-commanded DC operating conditions table, and stable clock, then apply NOP or Deselect & take CKE HIGH.

4. Waiting minimum of 400ns then issue pre-charge all command. NOP or Deselect applied during 400ns period.

5. Issue an EMRS command to EMR (2). (Provide LOW to BA0 and BA2, and HIGH to BA1).

6. Issue an EMRS command to EMR (3). (Provide LOW to BA2 and HIGH to BA0 and BA1).

7. Issue EMRS to enable DLL. (Provide Low to A0, HIGH to BA0 and LOW to BA1-BA2 and A13-A15. And A9=A8=A7=LOW must be used when issuing this command.)

8. Issue a Mode Register Set command for DLL reset. (Provide HIGH to A8 and LOW to BA0-BA2, and A13-A15.)

9. Issue a precharge all command.

10. Issue 2 more auto-refresh commands.

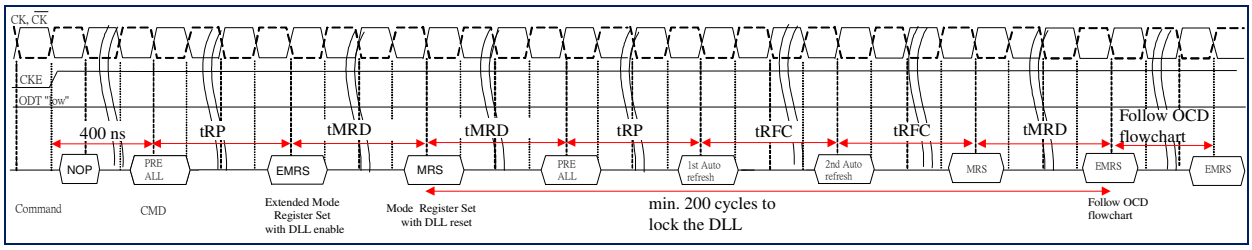
11. Issue a MRS command with LOW to A8 to initialize device operation (i.e. to program operating parameters without resetting the DLL.)

12. At least 200 clocks after step 7, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRs to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).

13. The DDR2 DRAM is now ready for normal operation.

* To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin.

Example



Register Definition

Programming the Mode Registration and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive $\overline{CAS}$ latency, driver impedance, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) and Extended Mode Registers (EMR (#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued. MRS, EMRS and DLL Reset do not affect array contents, which mean re-initialization including those can be executed any time after power-up without affecting array contents.

Mode Registration Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, tWR and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 ~ A13. The DDR2 SDRAM should be in all banks precharged (idle) mode with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and $\overline{CAS}$ latency is defined by A4 ~ A6. A7 is used for test mode and must be set to low for normal MRS operation. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (WR) definition for Auto-Precharge mode.

MRS Mode Register Operation Table (Address Input for Mode Set)

Address Field

BA2*	BA1	BA0	A13*	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

MRS mode

BA 1	BA0	MRS mode
0	0	**MR**
0	1	EMR(1)
1	0	EMR(2)
1	1	EMR(3)

Active power down exit time

A12	Active power down exit time
0	Fast exit (use tXARD)
1	Slow exit (use tXARDS)

Write recovery for autoprecharge

A11	A10	A9	WR (cycles)
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DDR2-667 DDR2-800 DDR2-1066

DLL Reset

A8	DLL Reset
0	NO
1	YES

Burst Length

A2	A1	A0	BL
0	1	0	4
0	1	1	8

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

/CAS Latency

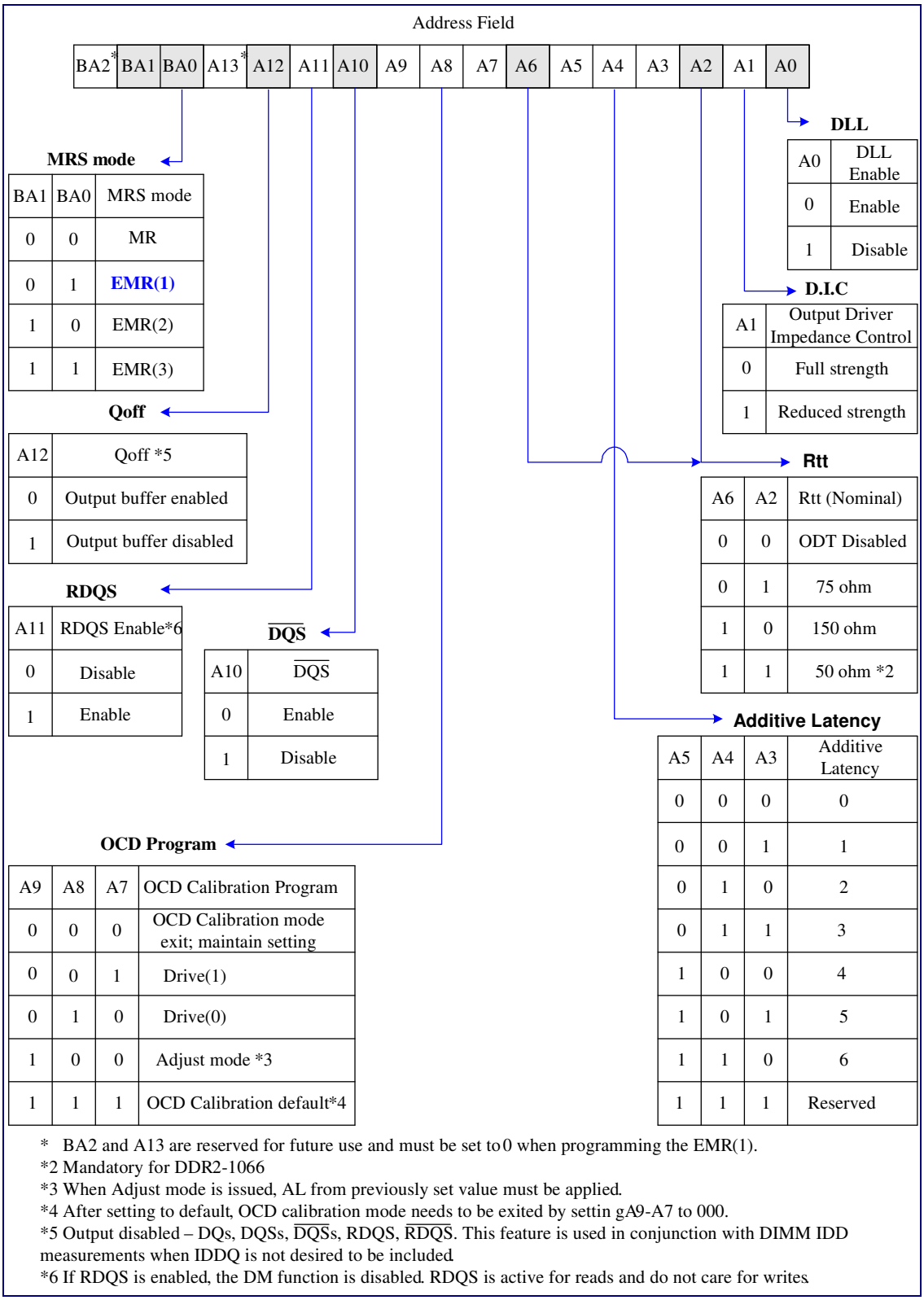
A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Mode

A7	Mode
0	Normal
1	TEST

* BA2 and A13 are reserved for future use and must be set to "0" when programming MR.

Extended Mode Register Set -EMRS (1) Programming



BA1	BA0	MRS mode
0	0	MR
0	1	**EMR(1)**
1	0	EMR(2)
1	1	EMR(3)

A0	DLL Enable
0	Enable
1	Disable

A1	Output Driver Impedance Control
0	Full strength
1	Reduced strength

A12	Qoff *5
0	Output buffer enabled
1	Output buffer disabled

A6	A2	Rtt (Nominal)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm *2

A11	RDQS Enable*6
0	Disable
1	Enable

A10	$\overline{DQS}$
0	Enable
1	Disable

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode *3
1	1	1	OCD Calibration default*4

* BA2 and A13 are reserved for future use and must be set to 0 when programming the EMR(1).
*2 Mandatory for DDR2-1066
*3 When Adjust mode is issued, AL from previously set value must be applied.
*4 After setting to default, OCD calibration mode needs to be exited by settin gA9-A7 to 000.
*5 Output disabled – DQs, DQSs, $\overline{DQS}$s, RDQS, $\overline{RDQS}$. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.
*6 If RDQS is enabled, the DM function is disabled. RDQS is active for reads and do not care for writes.

Extended Mode Register Set –EMRS (1)

The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program, RQDS enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and high on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the EMRS (1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength output driver. A3-A5 determines the additive latency, A7-A9 are used for OCD control, A10 is used for $\overline{DQS}$ disable and A11 is used for RDQS enable. A2 and A6 are used for ODT setting.

Single-ended and Differential Data Strobe Signals

The following table lists all possible combinations for DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ which can be programmed by A10 & A11 address bits in EMRS(1). RDQS and $\overline{RDQS}$ are available in x8 components only. If RDQS is enabled in x8 components, the DM function is disabled. RDQS is active for reads and don't care for writes.

EMRS (1)		Strobe Function Matrix				
A11 (RDQS Enable)	**A10 ($\overline{DQS}$ Enable)**	**RDQS/DM**	**$\overline{RDQS}$**	**DQS**	**$\overline{DQS}$**	**Signaling**
0 (Disable)	0 (Enable)	DM	Hi-Z	DQS	$\overline{DQS}$	differential DQS signals
0 (Disable)	1 (Disable)	DM	Hi-Z	DQS	Hi-Z	single-ended DQS signals
1 (Enable)	0 (Enable)	RDQS	$\overline{RDQS}$	DQS	$\overline{DQS}$	differential DQS signals
1 (Enable)	1 (Disable)	RDQS	Hi-Z	DQS	Hi-Z	single-ended DQS signals

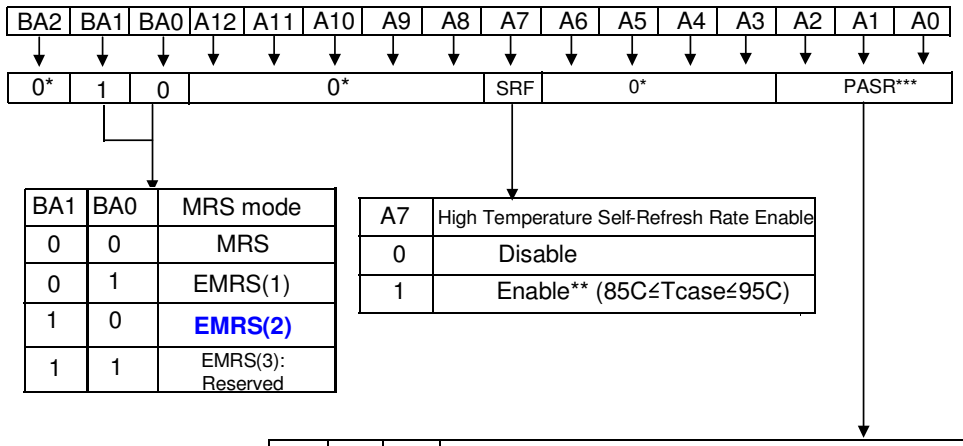
DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Less clock cycles may result in a violation of the t_{AC} or t_{DQSCK} parameters.

Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Q_{off} bit in the EMRS (1) is set to 0). When the Q_{off} bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure I_{DD} currents during Read operations, without including the output buffer current and external load currents.

EMRS (2) Extended Mode Register Set Programming



BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	**EMRS(2)**
1	1	EMRS(3): Reserved

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable** (85C≤Tcase≤95C)

A2	A1	A0	Partial Array Self Refresh
0	0	0	Full array
0	0	1	Half Array (BA[2:0]=000, 001, 010, &011)
0	1	0	Quarter Array (BA[2:0]=000&001)
0	1	1	1/8th array (BA[2:0] = 000)
1	0	0	3 / 4 array (BA[2:0]=010,011,100,101,110, &111)
1	0	1	Half array (BA[2:0]=100, 101, 110, & 111)
1	1	0	Quarter array (BA[2:0]=110&111)
1	1	1	1/8th array (BA[2:0]=111)

* The rest bits in EMRS(2) is reserved for future use and all bits in EMRS(2) except A0-A2,A7,BA0, and BA1 must be programmed to 0 when setting EMRS(2) during initialization.
** DDR2 SDRAM Module user can look at module SPD field Byte 49 bit [0].
*** Optional. If PASR(Partial Array Self Refresh) is enabled, data located in areas of the array beyond the spec. location will be lost if self refresh is entered.

Extended Mode Register Set EMRS (2)

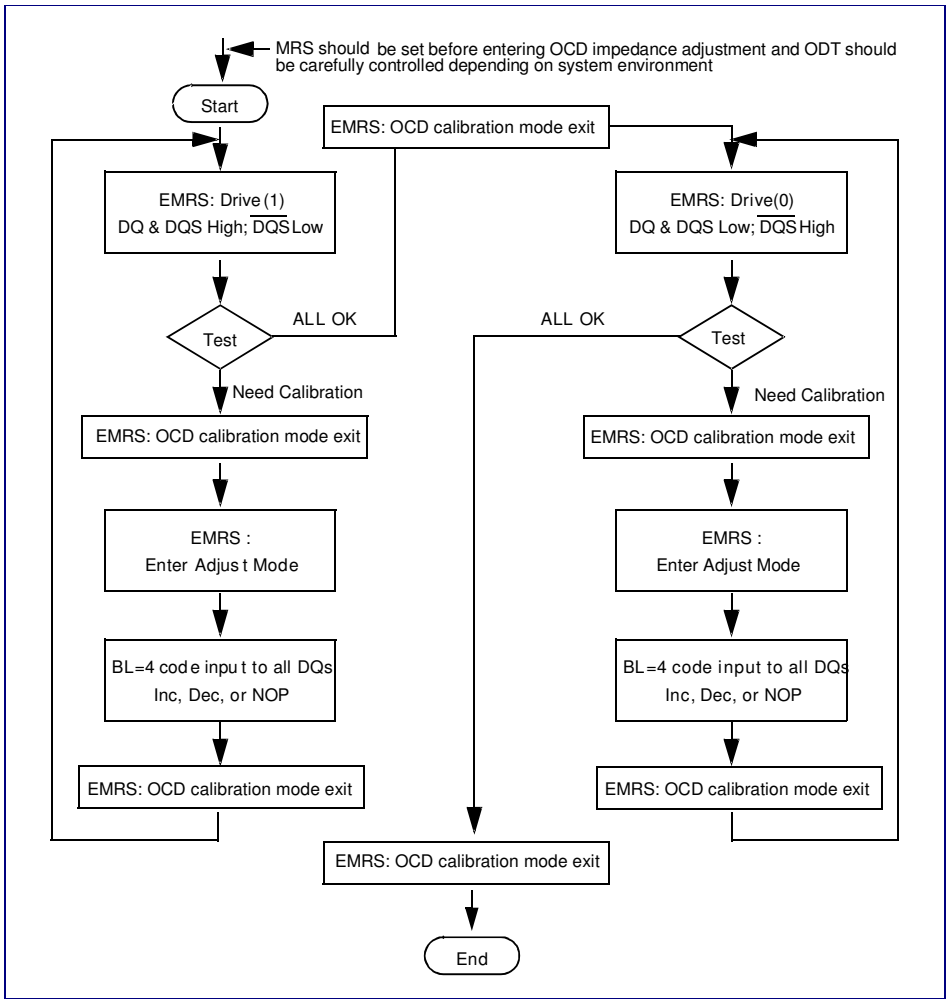
The Extended Mode Registers (2) controls refresh related features. The default value of the extended mode register(2) is not defined, therefore the extended mode register(2) is written by asserting low on CS, RAS, CAS, WE, BA0, high on BA1, while controlling the states of address pin A0-A13. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

EMRS(3) Extended Mode Register Set Programming

All bits in EMRS(3) expect BA0 and BA1 are reserved for future use and must be programmed to 0 when setting the mode register during initialization.

Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS (1) mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS (1) bit enabling RDQS operation. In Drive (1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven low. In Drive (0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMRS (1) and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A7~A9 as '000' in order to maintain the default or calibrated value.

Off- Chip-Driver program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$ low
0	1	0	Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$ high
1	0	0	Adjust mode
1	1	1	OCD calibration default

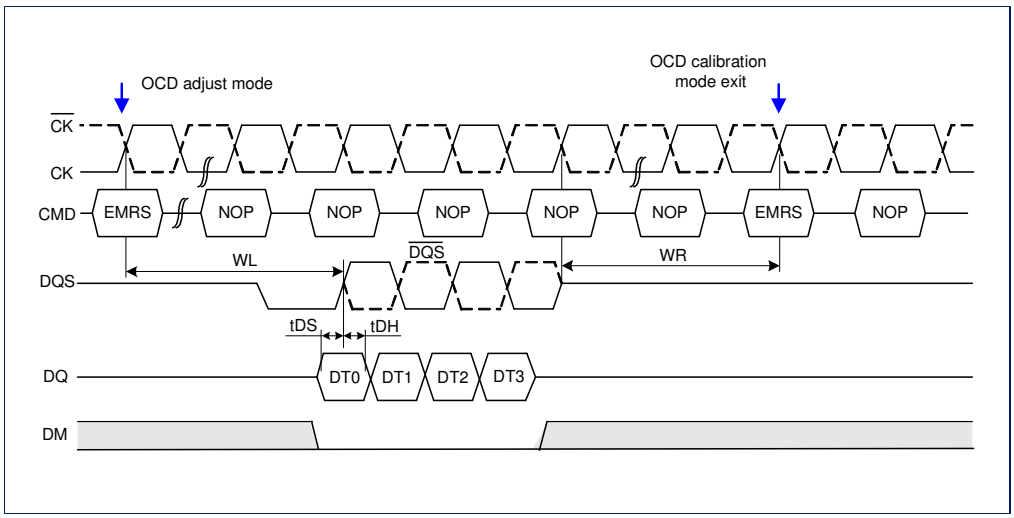
OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS (1) command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 is the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment can be up to 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the maximum step count range. When Adjust mode command is issued, AL from previously set value must be applied.

4 bit burst code inputs to all DQs				Operation	
DT0	**DT1**	**DT2**	**DT3**	**Pull-up driver strength**	**Pull-down driver strength**
0	0	0	0	NOP (no operation)	NOP (no operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

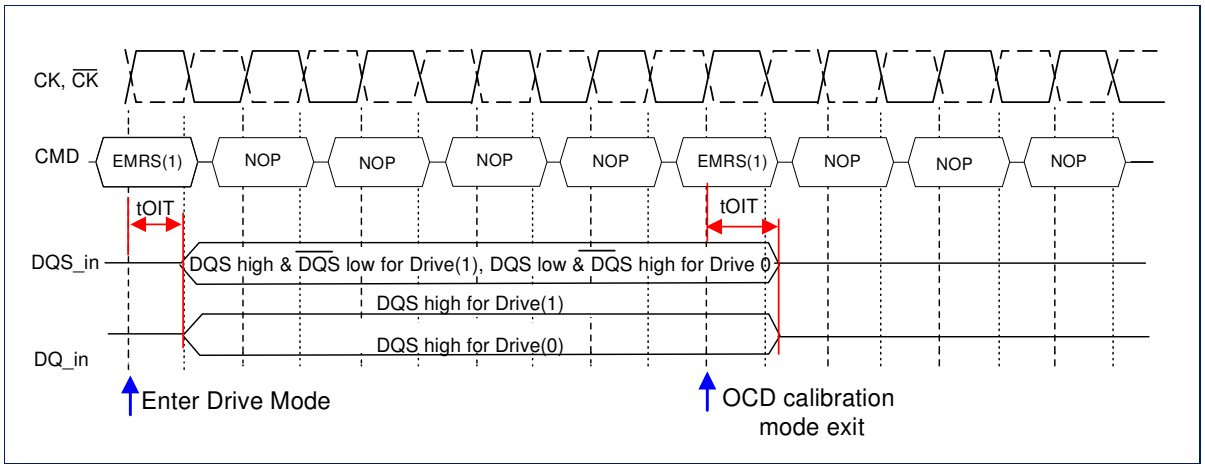
For proper operation of adjust mode, WL = RL - 1 = AL + CL -1 clocks and t_{DS} / t_{DH} should be met as the following timing diagram. Input data pattern for adjustment, DT0 ~ DT3 is fixed and not affected by MRS addressing mode (i.e. sequential or interleave).

OCD Adjust Mode



Drive Mode

Drive mode, both Drive (1) and Drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command as the following timing diagram.

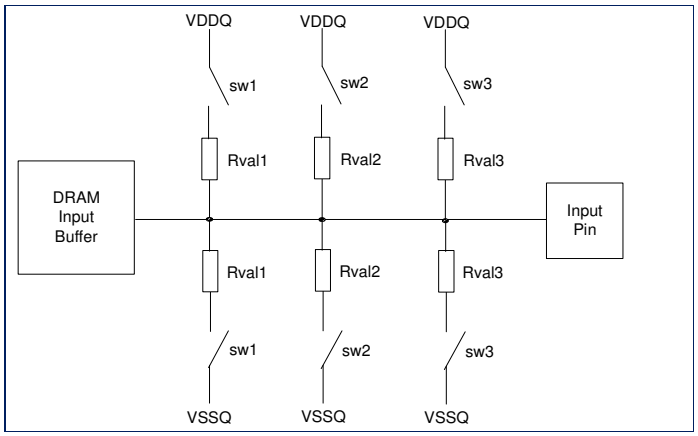


On-Die Termination (ODT)

ODT (On-Die Termination) is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQ, DQS, DQS, RDQS, RDQS, and DM signal for x8 configurations via the ODT control pin. For x16 configuration ODT is applied to each DQ, UDQS, UDQS, LDQS, LDQS, UDM and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

Functional Representation of ODT



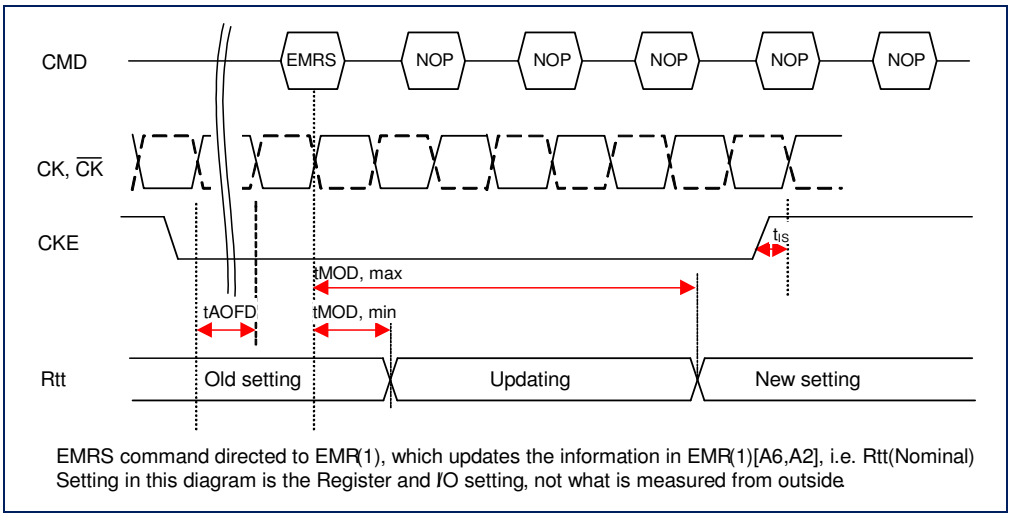
Switch sw1, sw2, or sw3 is enabled by the ODT pin. Selection between sw1, sw2, or sw3 is determined by "Rtt (nominal)" in EMRS.

Termination included on all DQs, DM, DQS, DQS, RDQS, and RDQS pins.

ODT related timings

MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between tMOD, min and tMOD, max, and CKE must remain HIGH for the entire duration of tMOD window for proper operation. The timings are shown in the following timing diagram.



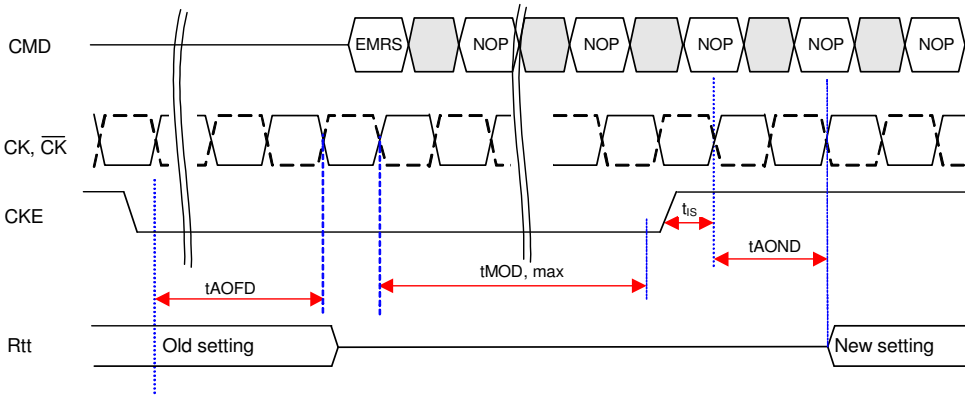
EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt(Nominal) Setting in this diagram is the Register and I/O setting, not what is measured from outside.

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of tMOD window, until tMOD, max is met.

Now the ODT is ready for normal operation with the new setting, and the ODT may be raised again to turn on the ODT.

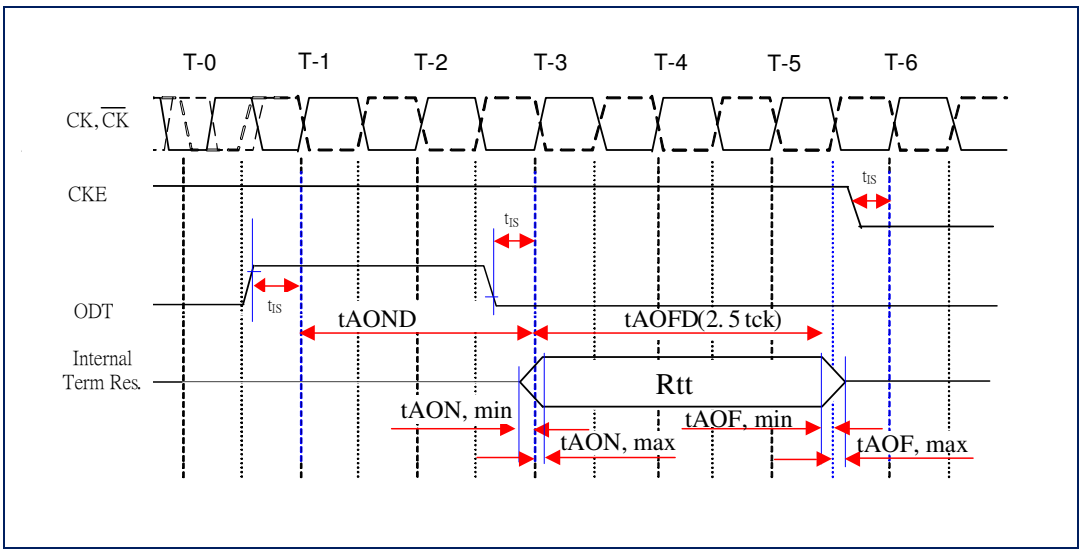
Following timing diagram shows the proper Rtt update procedure.



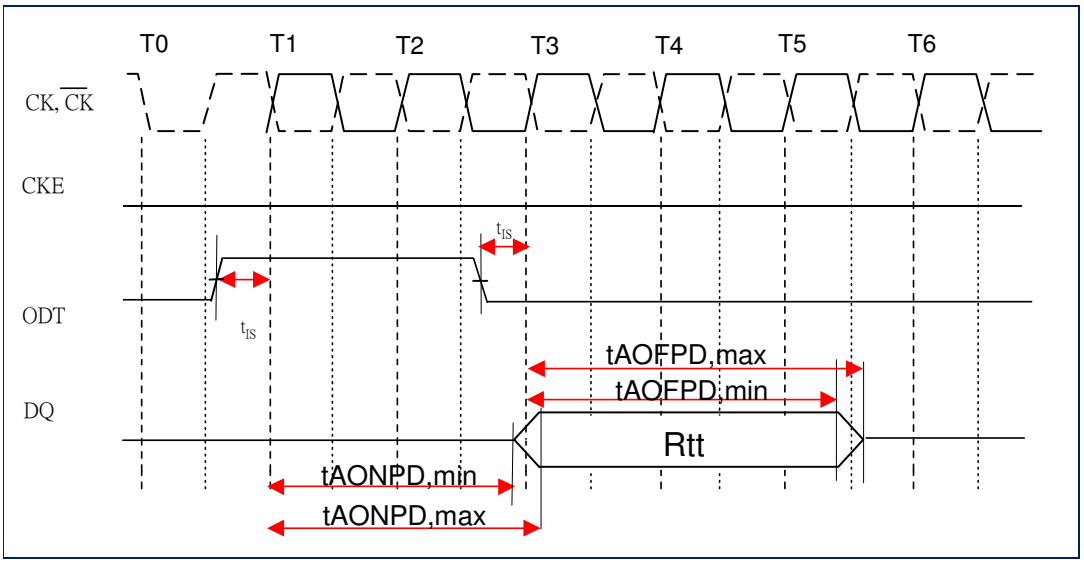
EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt(Nominal) Setting in this diagram is the Register and I/O setting, not what is measured from outside.

ODT On/Off timings

ODT timing for active/standby mode



ODT Timing for Power-down mode



Bank Activate Command

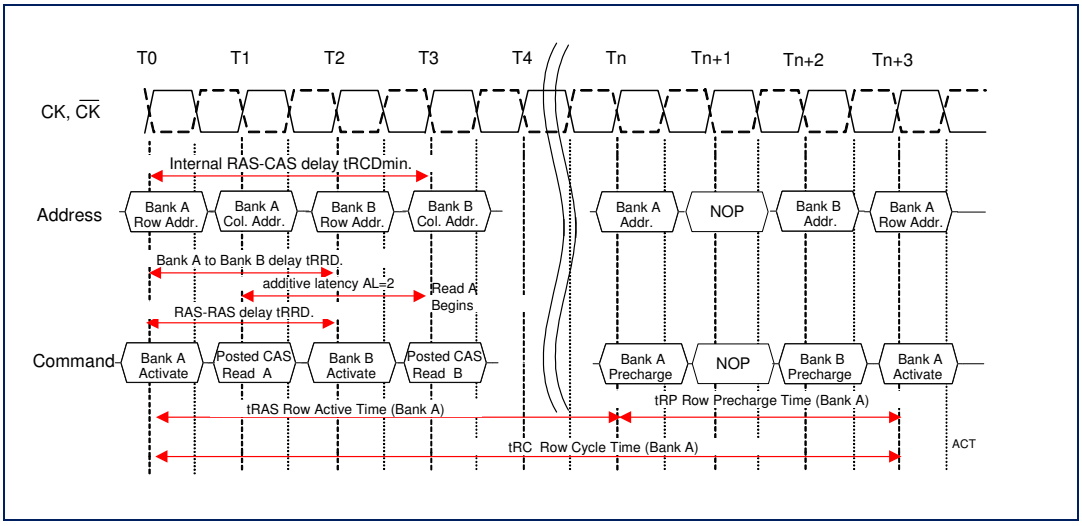
The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high plus $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for and x8 organized components. For x16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If an R/W command is issued to a bank that has not satisfied the t_{RCDmin} specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure t_{RCDmin} is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5, and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (t_{RC}). The minimum time interval between Bank Active commands, to other bank, is the Bank A to Bank B delay time (t_{RRD}).

In order to ensure that 8 bank devices do not exceed the instantaneous current supplying capability of 4 bank devices, certain restrictions on operation of the 8 bank devices must be observed. There are two rules. One for restricting the number of sequential ACTcommands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are list as follow:

* 8 bank device sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Conveting to clocks is done by dividing tFAW by tCK and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clock N+1 through N+9.

*8 bank device Precharge All Allowance: tRP for a Precharge All command for an 8 Bank device will equal to tRP+tCK, where tRP is the value for a single bank pre-charge.

Bank Activate Command Cycle: t_{RCD} = 3, AL = 2, t_{RP} = 3, t_{RRD} = 2, t_{CCD} = 2



Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is restricted to specific segments of the page length.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL=8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively, and the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (t_{CCD}) is minimum 2 clocks for read or write cycles.

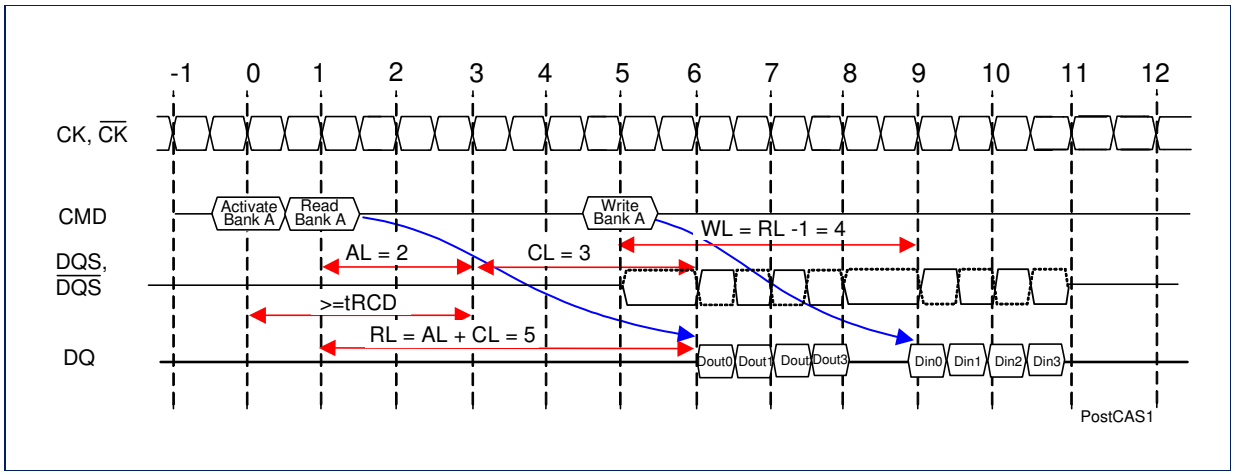
Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS (1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{CAS}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the t_{RCDmin} period, the Read Latency is also defined as RL = AL + CL.

Example of posted $\overline{CAS}$ operation:

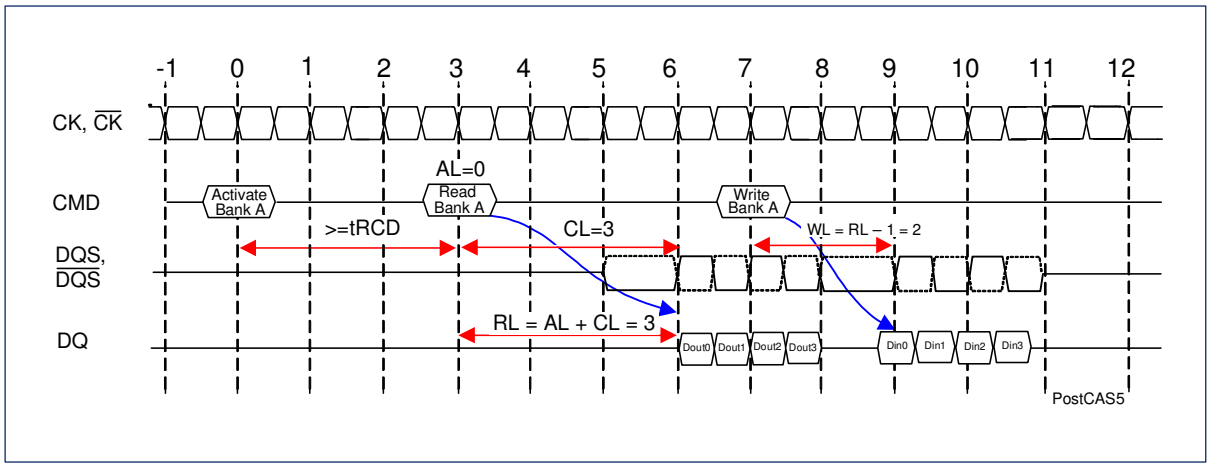
Read followed by a write to the same bank:

AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4



Read followed by a write to the same bank:

AL = 0, CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4



Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the "Burst Interruption "section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

Bust Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: 1) Page length is a function of I/O organization

64Mb X 16 organization (CA0-CA9); Page Size = 2K Byte; Page Length = 1024

128Mb X 8 organization (CA0-CA9); Page Size = 1K Byte; Page Length = 1024

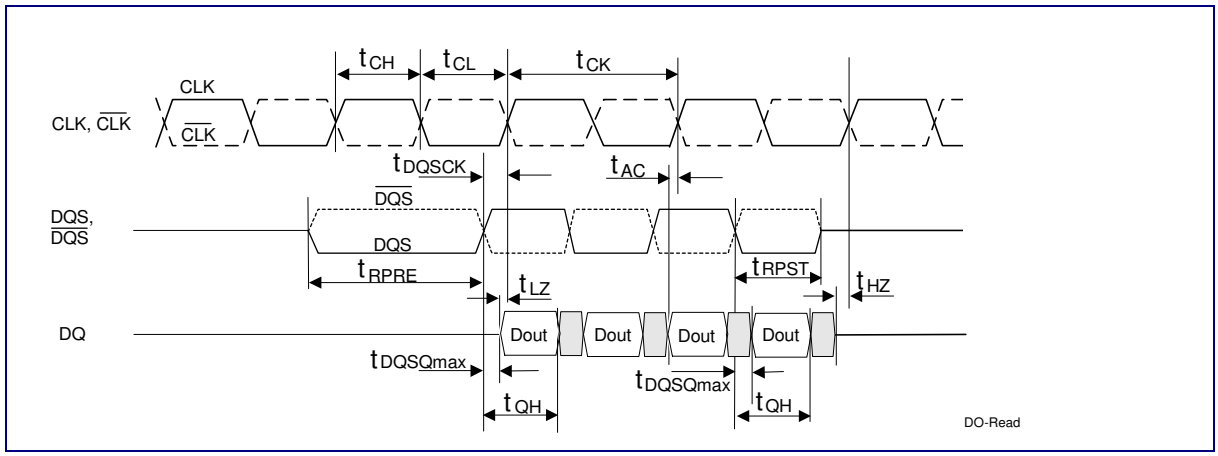
256Mb x 4 organization (CA0-CA9, CA11); Page Size = 1K Byte; Page Length = 2048

2) Order of burst access for sequential addressing is "nibble-based" and therefore different from SDR or DDR components

Burst Read Command

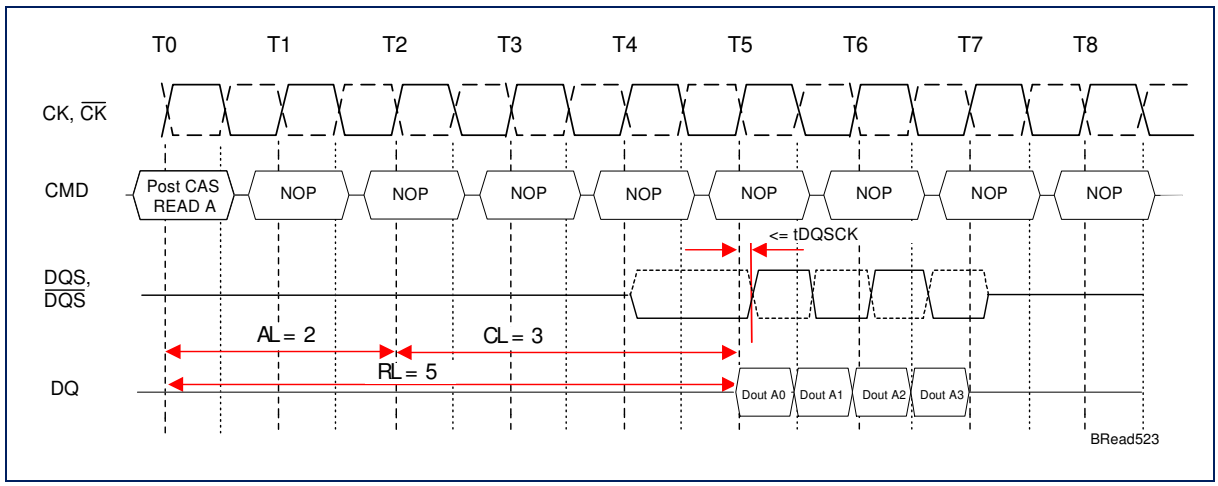
The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS (1))

Basic Burst Read Timing

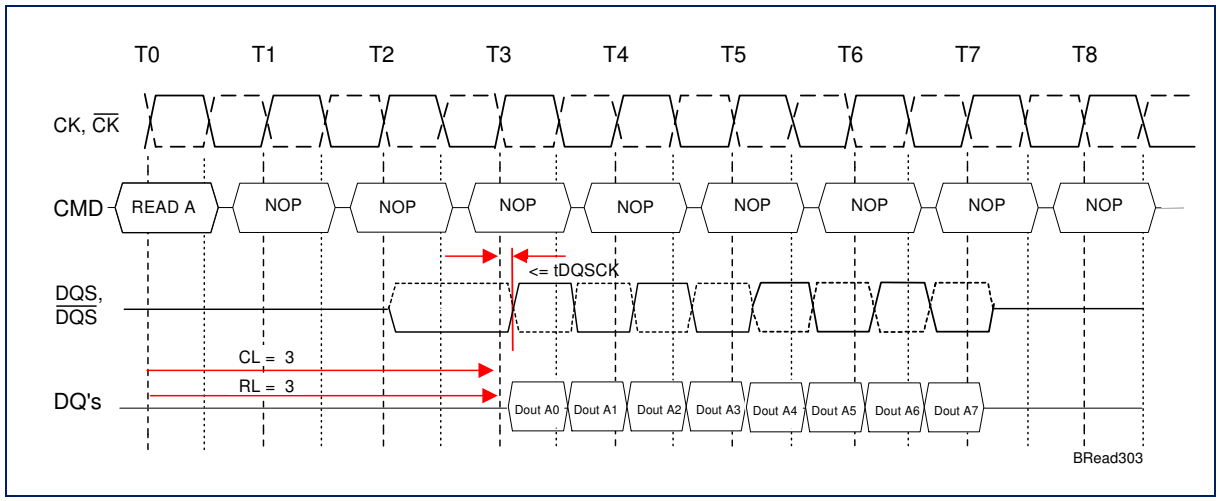


Examples:

Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)

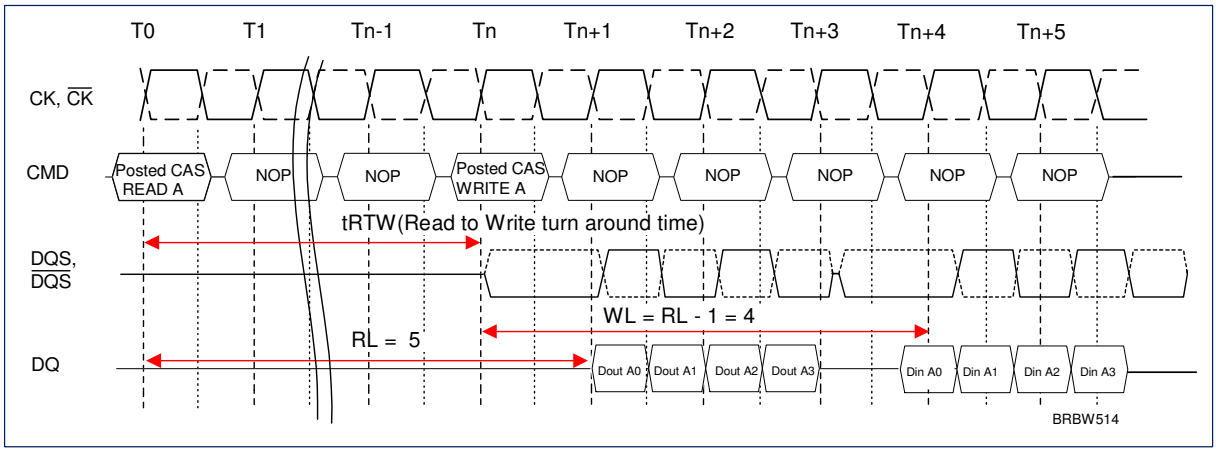


Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)

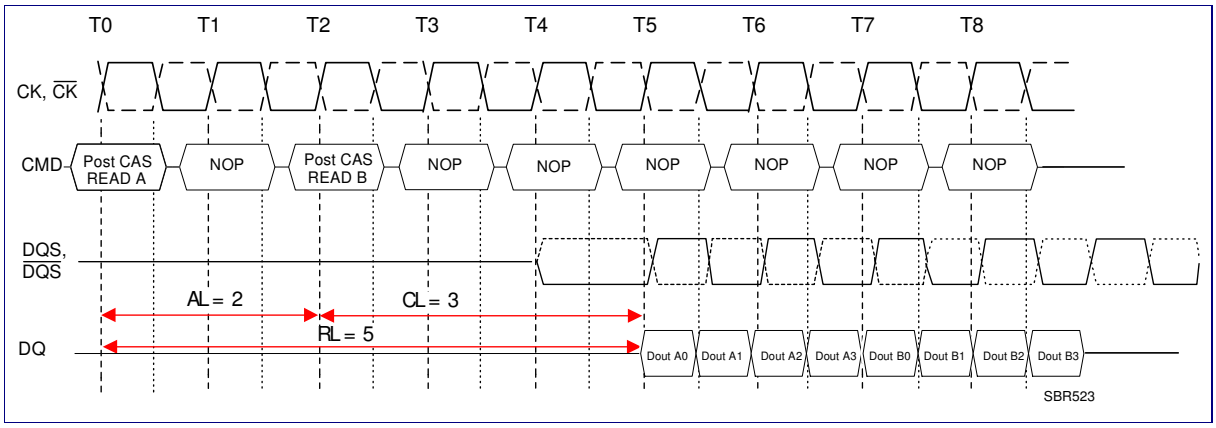


Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around time(tRTW), which is 4 clocks in case of BL=4 operation, 6 clocks in case of BL=8 operation.



Seamless Burst Read Operation: RL = 5, AL = 2, CL = 3, BL = 4



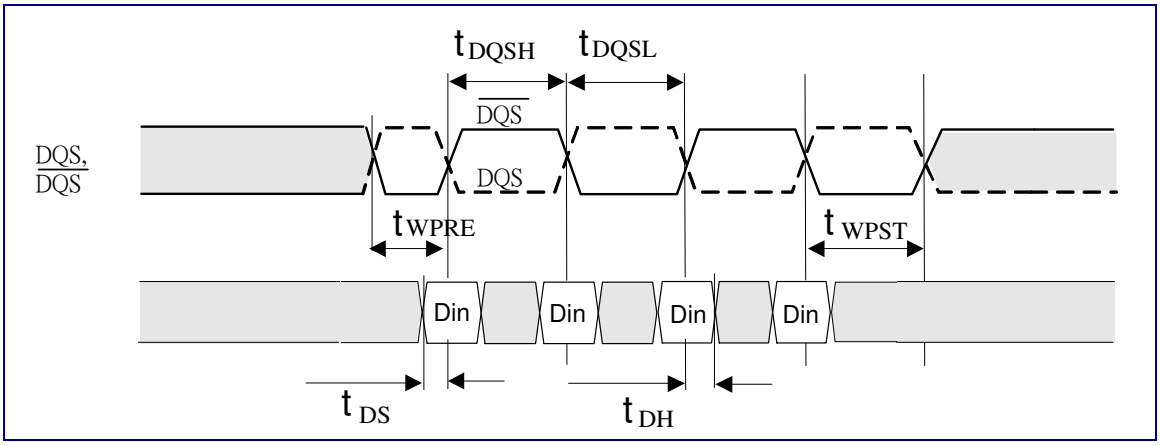
The seamless burst read operation's supported by enabling a read command at every clock for BL=4 operation, and every 4 clock for BL=8 operation. This operation allows regardless of same or different banks as long as the banks activated.

Burst Write Command

The Burst Write command is initiated by having CS, CAS and WE low while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) has to be driven low (preamble) a time tWPRE prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named "write recovery time" (WR) .

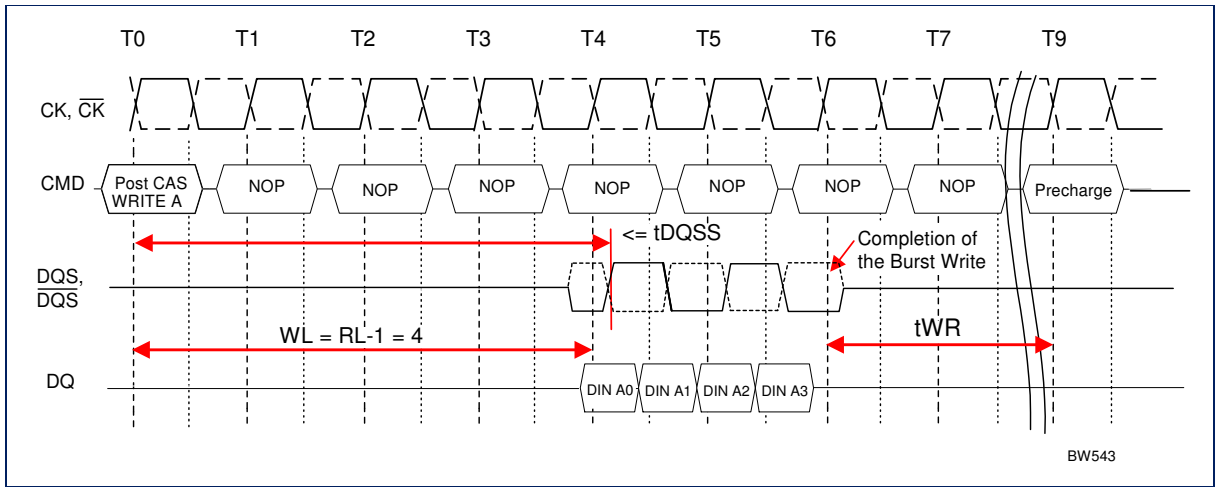
DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing measured is mode dependent.

Basic Burst Write Timing



Example:

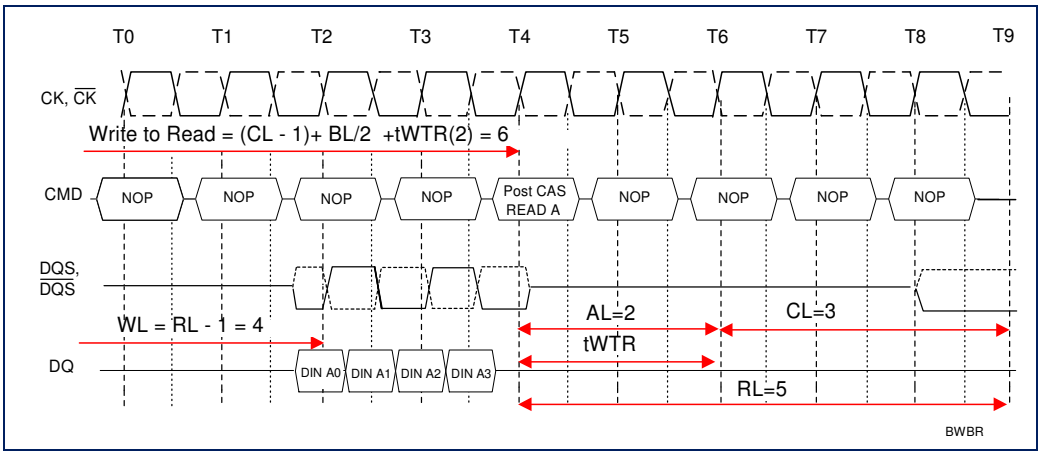
Burst Write Operation: RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4



Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4

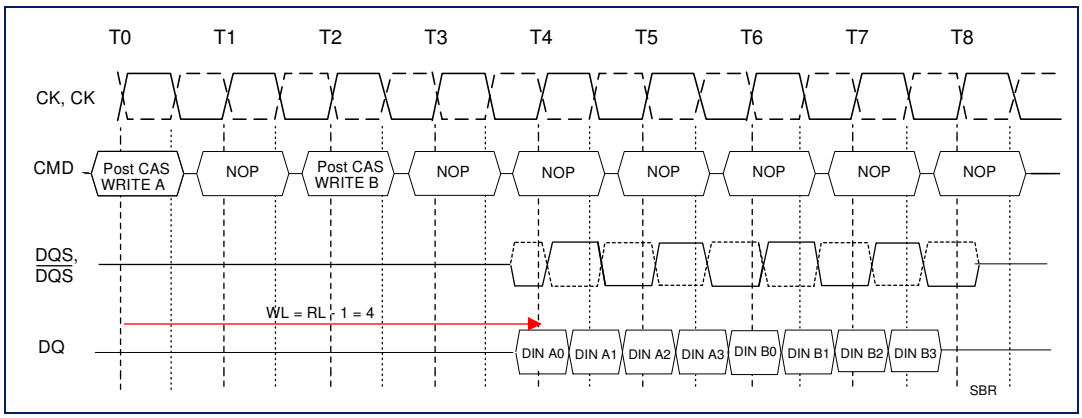
The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around time(tRTW), which is 4 clocks in case of BL=4 operation, 6 clocks in case of BL=8 operation.

Burst Write followed by Burst Read: RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4



The minimum number of clocks from the burst write command to the burst read command is (CL - 1) +BL/2 + t_{WTR} where t_{WTR} is the write-to-read turn-around time t_{WTR} expressed in clock cycles. The t_{WTR} is not a write recovery time (t_{WR}) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write Operation: RL = 5, WL = 4, BL = 4

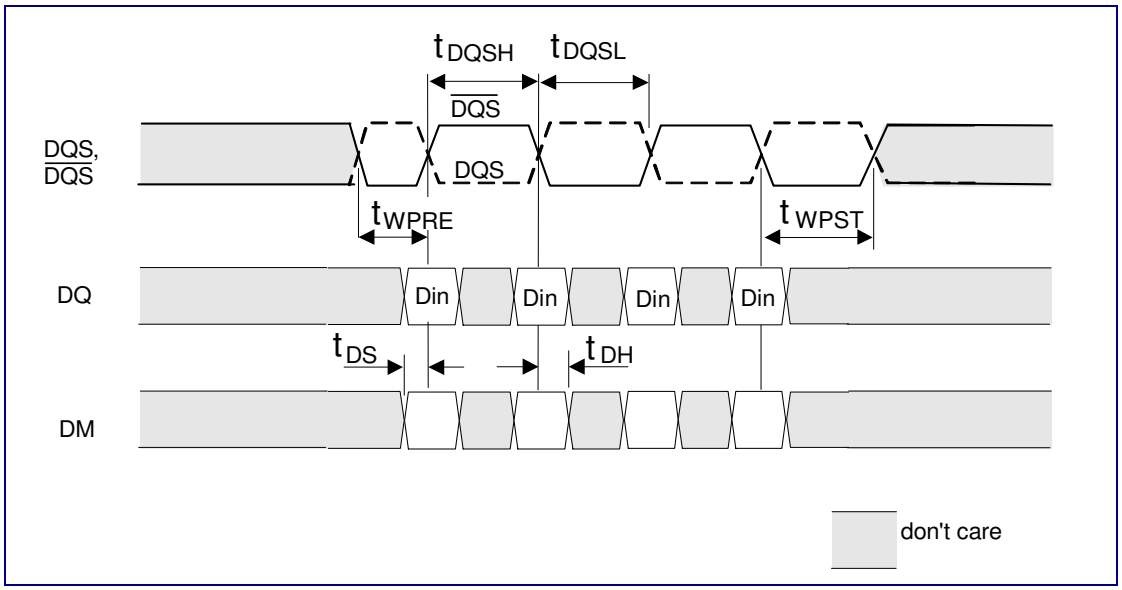


The seamless burst write operation is supported by enabling a write command every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

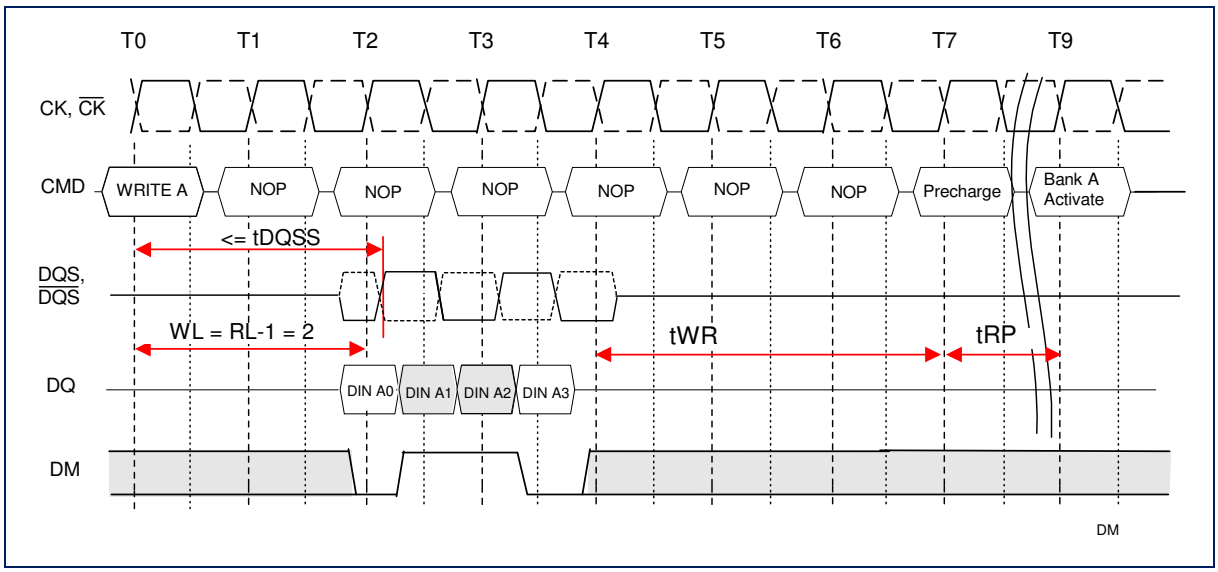
Write Data Mask

One write data mask input (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM of x4 and x16 bit organization is not used during read cycles. However, DM of x8 bit organization can be used as RDQS during read cycles by EMRS (1) setting.

Write Data Mask Timing



Burst Write Operation with Data Mask: RL = 3 (AL = 0, CL = 3), WL = 2, t_{WR} = 3, BL = 4



Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.

2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.

3. Read burst interrupt occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.

4. Write burst interrupt occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.

5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.

6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.

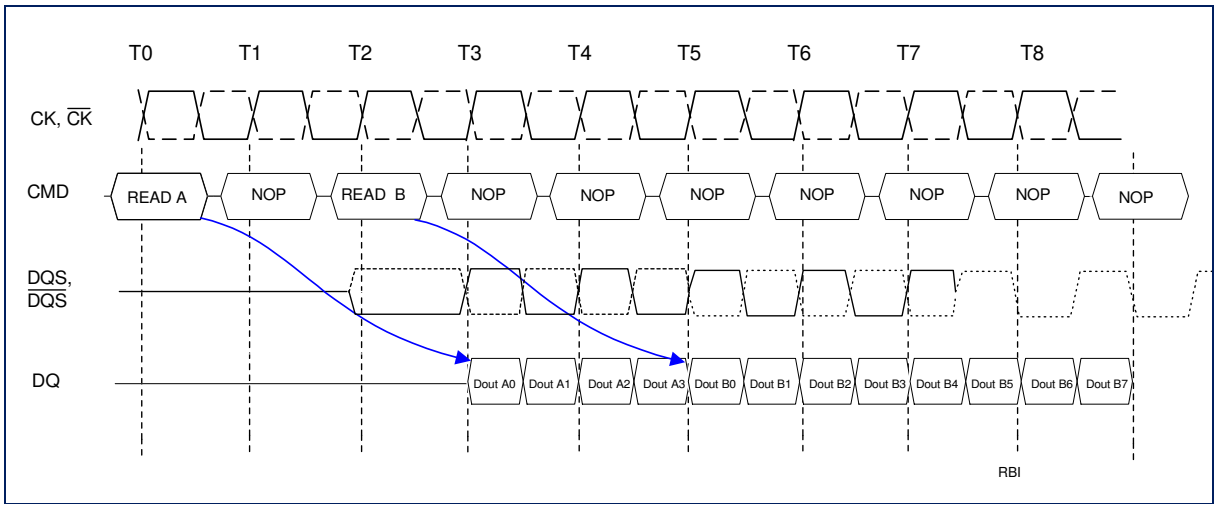
7. Read burst interruption is allowed by a Read with Auto-Precharge command.

8. Write burst interruption is allowed by a Write with Auto-Precharge command.

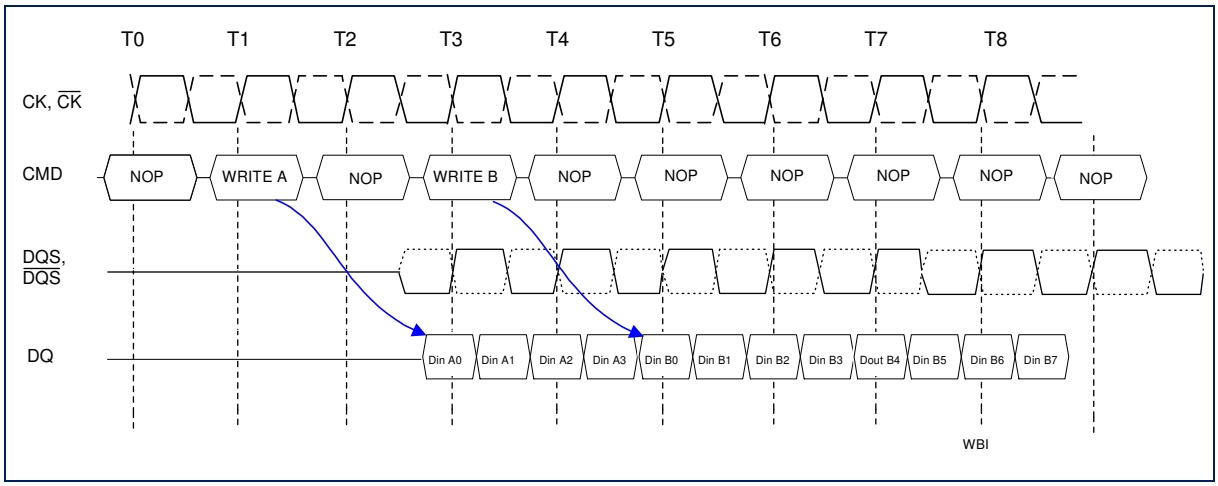
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + t_{WR}, where t_{WR} starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

Examples:

Read Burst Interrupt Timing Example: (CL = 3, AL = 0, RL = 3, BL = 8)



Write Burst Interrupt Timing Example: (CL = 3, AL = 0, WL = 2, BL = 8)



Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0, BA1, and BA2 are used to define which bank to precharge when the command is issued.

Bank Selection for Precharge by Address Bit

A10	BA2	BA1	BA0	Precharge Bank(s)
LOW	LOW	LOW	LOW	Bank 0 only
LOW	LOW	LOW	HIGH	Bank 1 only
LOW	LOW	HIGH	LOW	Bank 2 only
LOW	LOW	HIGH	HIGH	Bank 3 only
LOW	HIGH	LOW	LOW	Bank 4 only
LOW	HIGH	LOW	HIGH	Bank 5 only
LOW	HIGH	HIGH	LOW	Bank 6 only
LOW	HIGH	HIGH	HIGH	Bank 7 only
HIGH	Don't Care	Don't Care	Don't Care	all banks

Burst Read Operation Followed by a Precharge

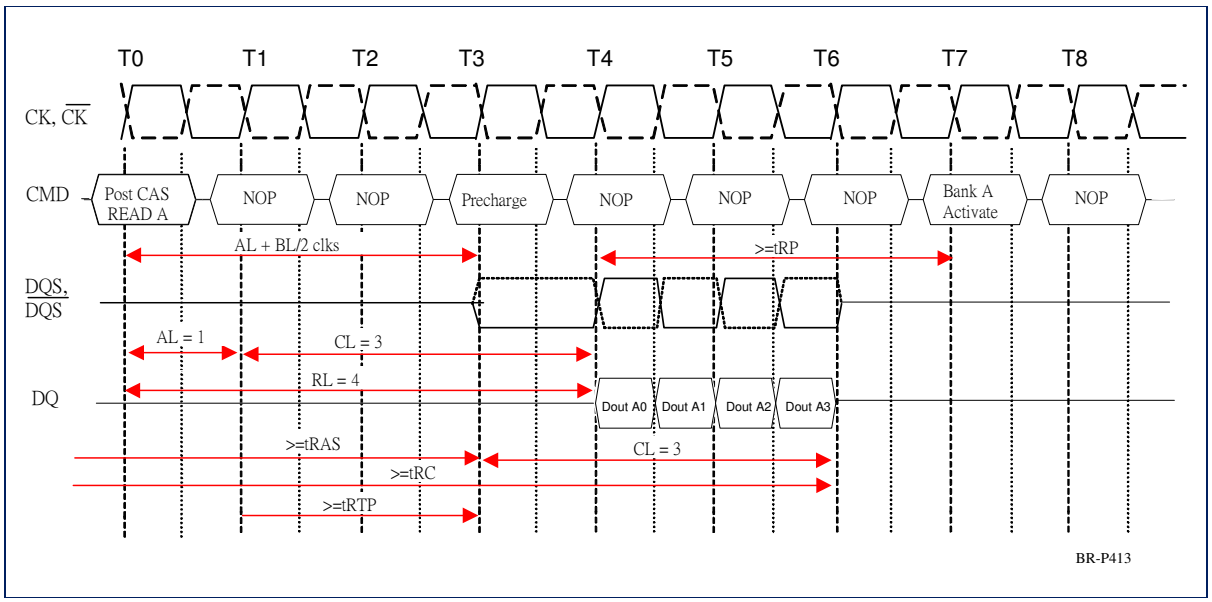
Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max (RTP, 2) - 2 clocks.

For the earliest possible precharge, the Precharge command may be issued on the rising edge which is “Additive Latency (AL) + BL/2 clocks” after a Read Command, as long as the minimum t_{RAS} timing is satisfied.

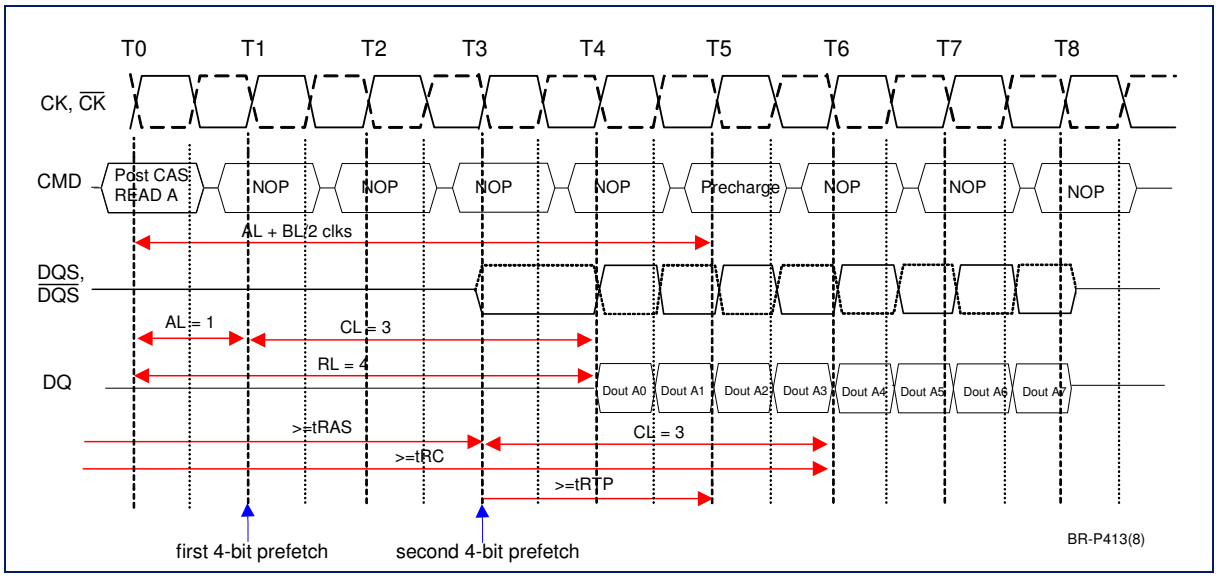
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is call tRTP (Read to Precharge). For BL=4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL=8 this is the time from AL + 2 clocks after the Read to the Precharge command.

Examples:

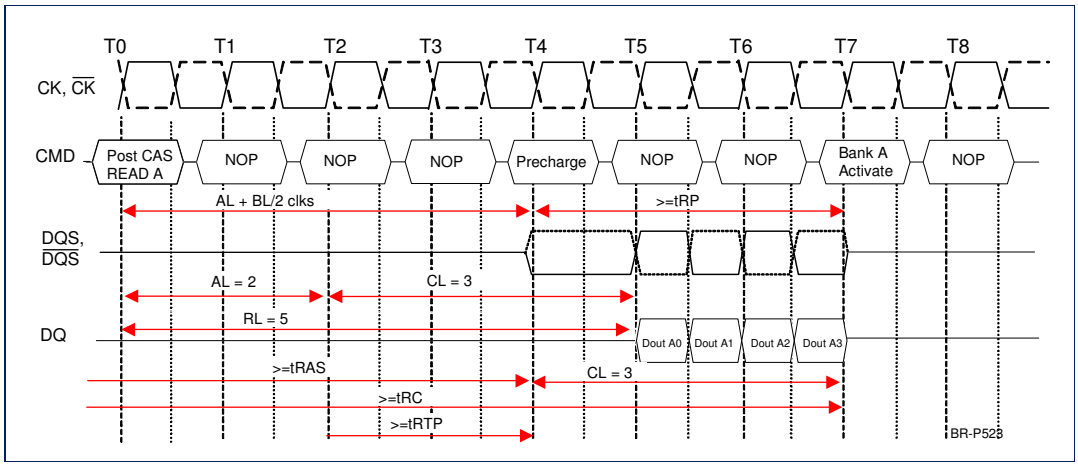
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



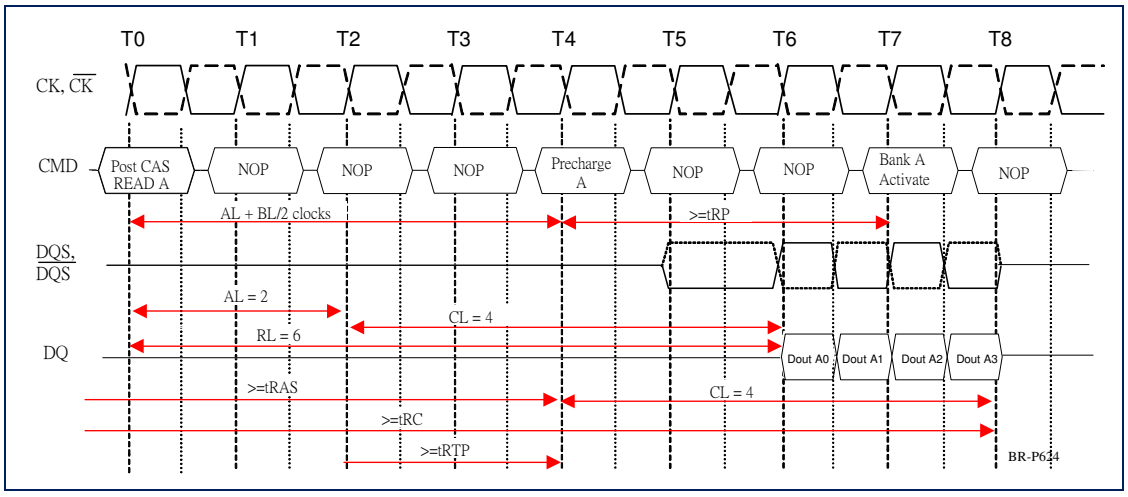
Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 8, t_{RTP} ≦ 2 clocks



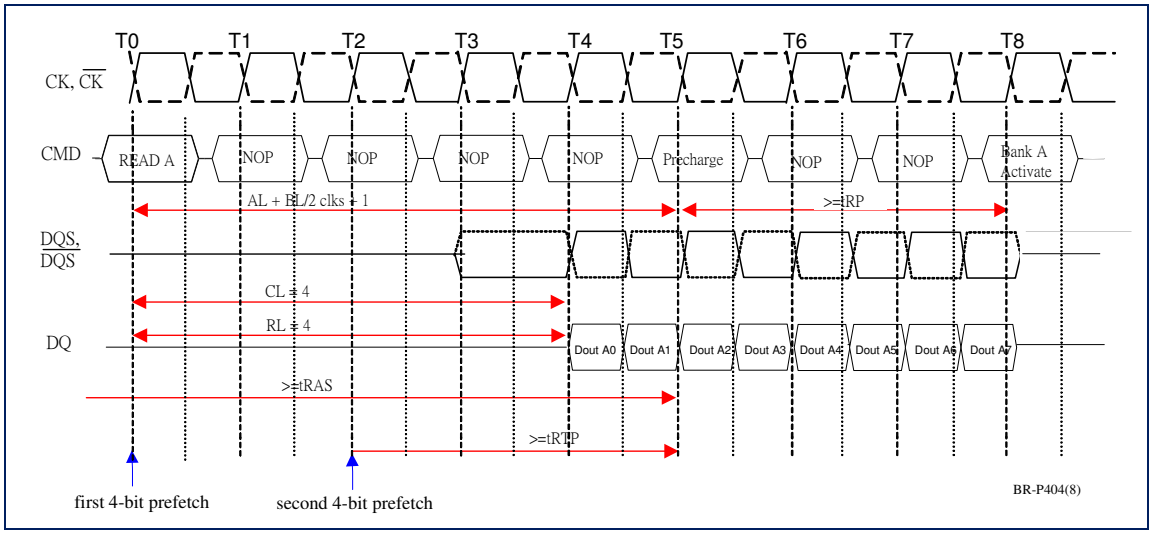
Burst Read Operation Followed by Precharge: RL = 5 (AL = 2, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



Burst Read Operation Followed by Precharge: RL = 6, (AL = 2, CL = 4), BL = 4, t_{RTP} ≦ 2 clocks



Burst Read Operation Followed by Precharge: RL = 4, (AL = 0, CL = 4), BL = 8, t_{RTP} > 2 clocks

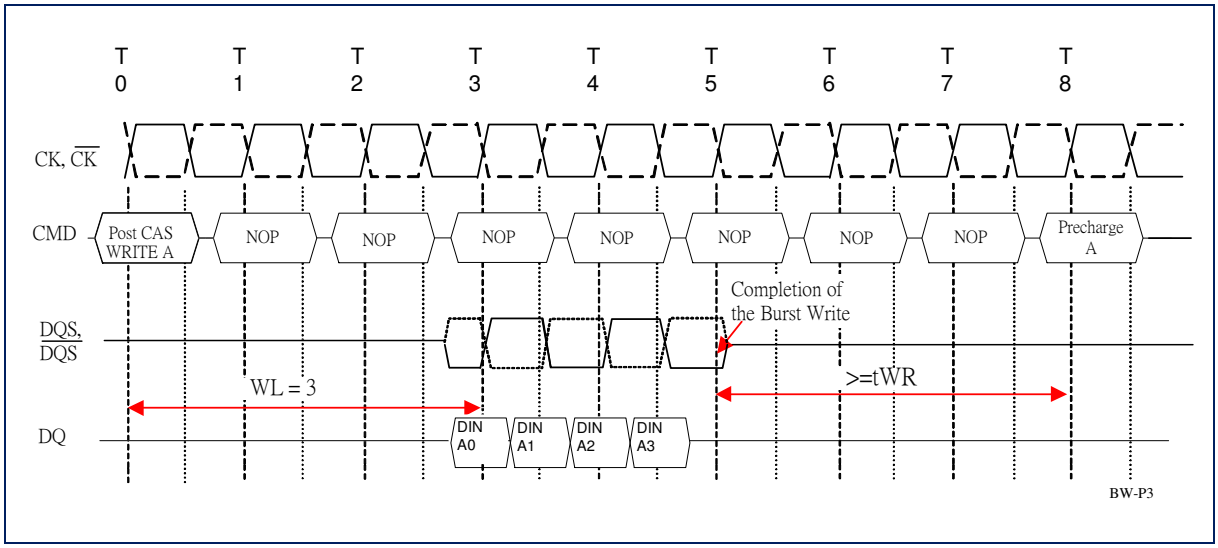


Burst Write followed by Precharge

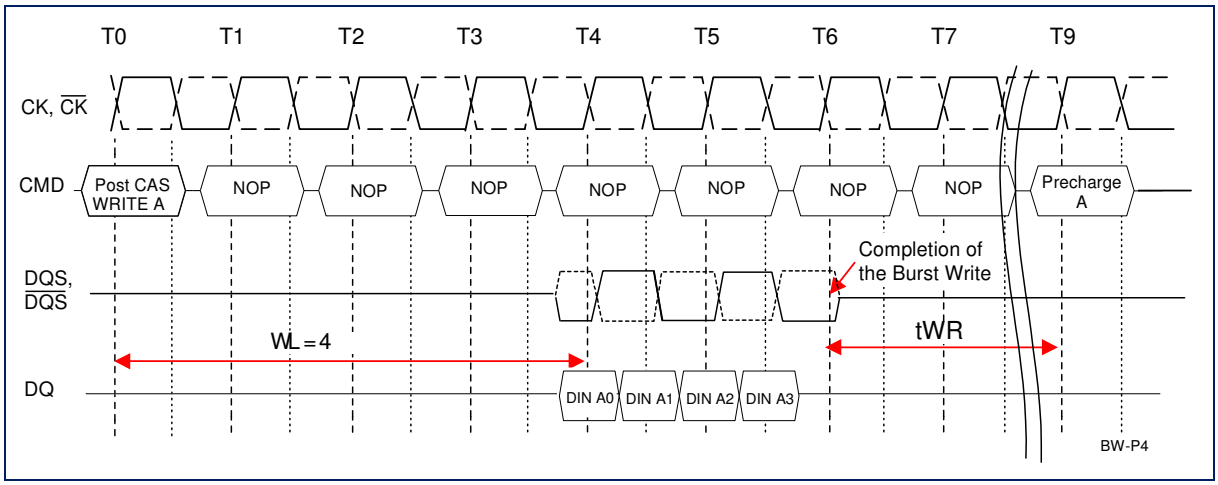
Minimum Write to Precharge command spacing to the same bank = **WL + BL/2 + t_{WR}**. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. t_{WR} is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for t_{WR} in the MRS.

Examples:

Burst Write followed by Precharge : WL = (RL - 1) = 3, BL = 4, t_{WR} = 3



Burst Write followed by Precharge : WL = (RL - 1) = 4, BL = 4, t_{WR} = 3



Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Pre-charge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is $\overline{CAS}$ Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands. The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon $\overline{CAS}$ Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if t_{RAS}(min) and t_{RTP} are satisfied. If t_{RAS}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RAS}(min) is satisfied. If t_{RTP}(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until t_{RTP}(min) is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + t_{RTP} + t_{RP}. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + t_{RTP} + t_{RP}. Note that both parameters t_{RTP} and t_{RP} have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

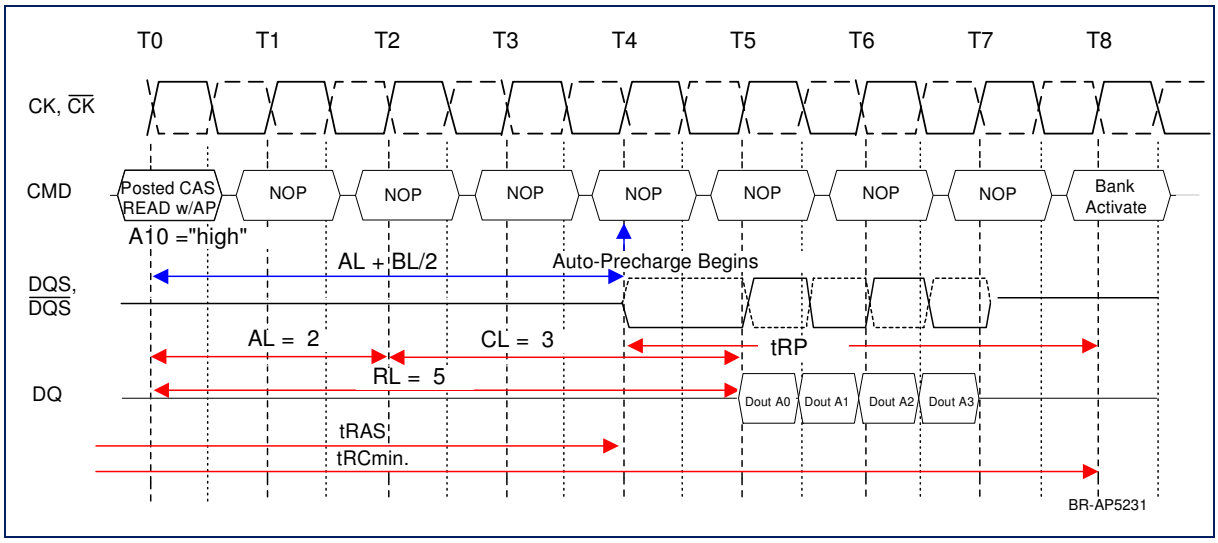
(1) The $\overline{RAS}$ precharge time (t_{RP}) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The $\overline{RAS}$ cycle time (t_{RC}) from the previous bank activation has been satisfied.

Examples:

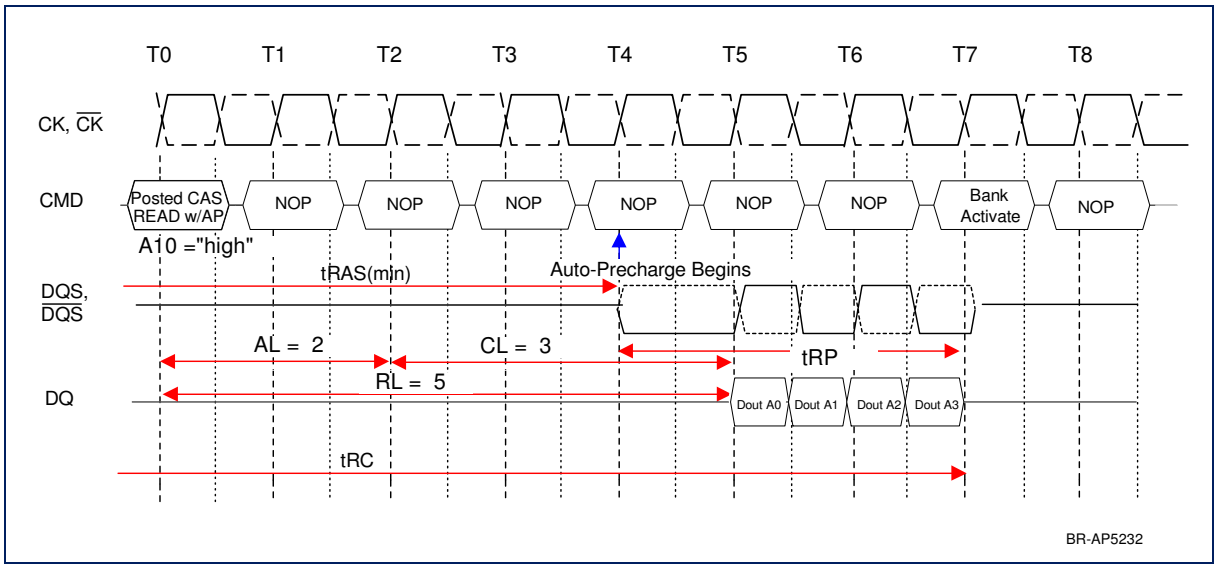
Burst Read with Auto-Precharge followed by an activation to the Same Bank (t_{RC} Limit)

RL = 5 (AL = 2, CL = 3), BL = 4, t_{RTP} ≦ 2 clocks



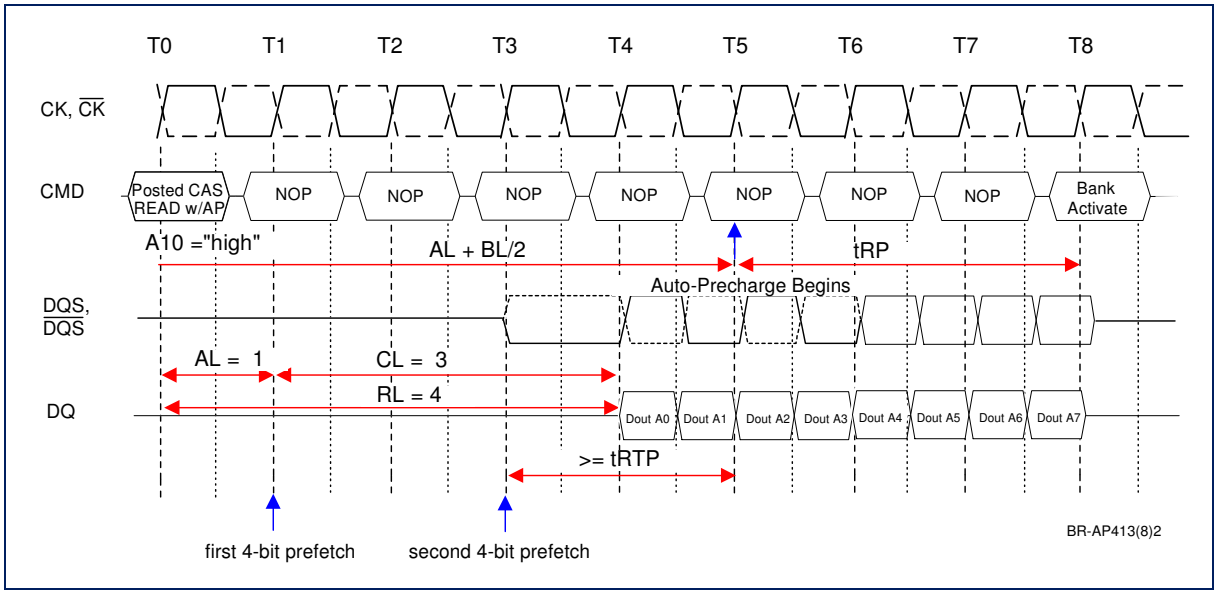
Burst Read with Auto-Precharge followed by an Activation to the Same Bank (tRAS Limit):

RL = 5 (AL = 2, CL = 3), BL = 4, tRTP ≦ 2 clocks



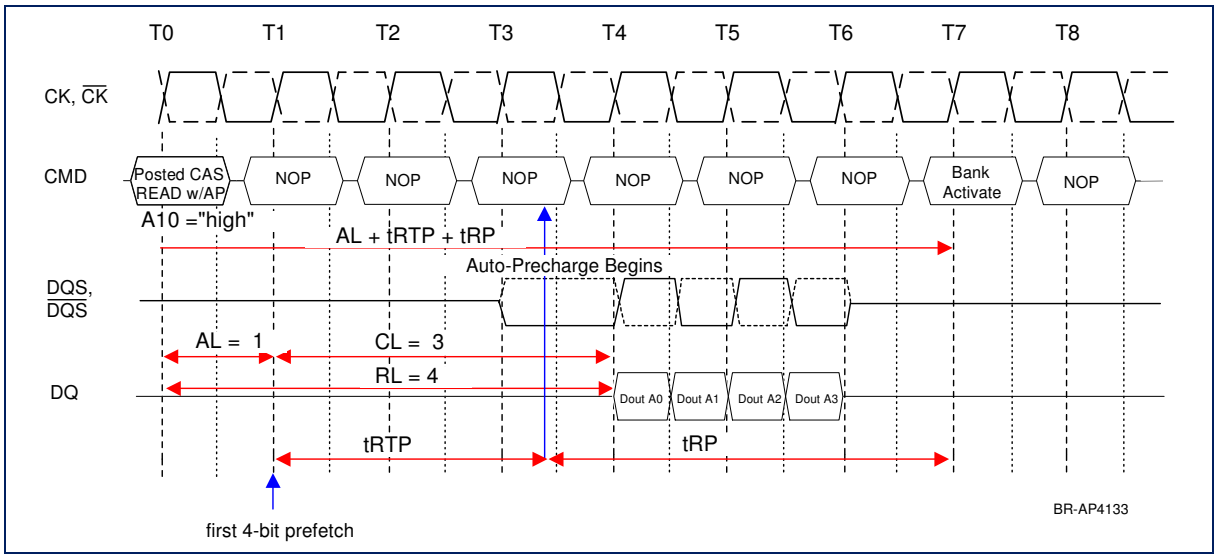
Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 8, t_{RTP} ≦ 2 clocks



Burst Read with Auto-Precharge followed by an Activation to the Same Bank:

RL = 4 (AL = 1, CL = 3), BL = 4, t_{RTP} > 2 clocks



Burst Write with Auto-Precharge

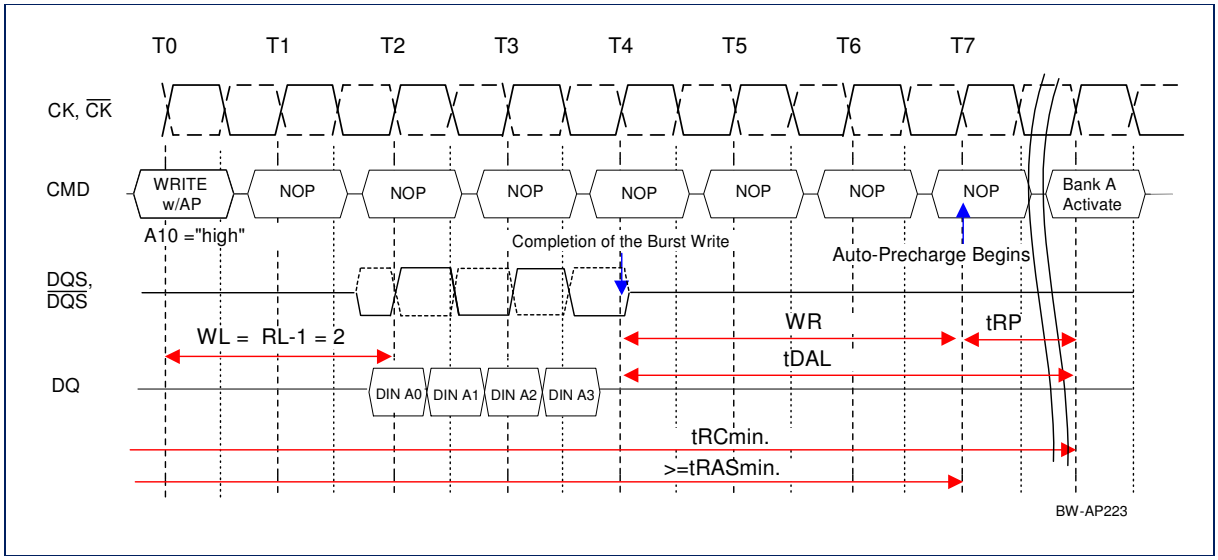
If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as t_{RAS} is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The last data-in to bank activate delay time (t_{DAL} = WR + t_{RP}) has been satisfied.

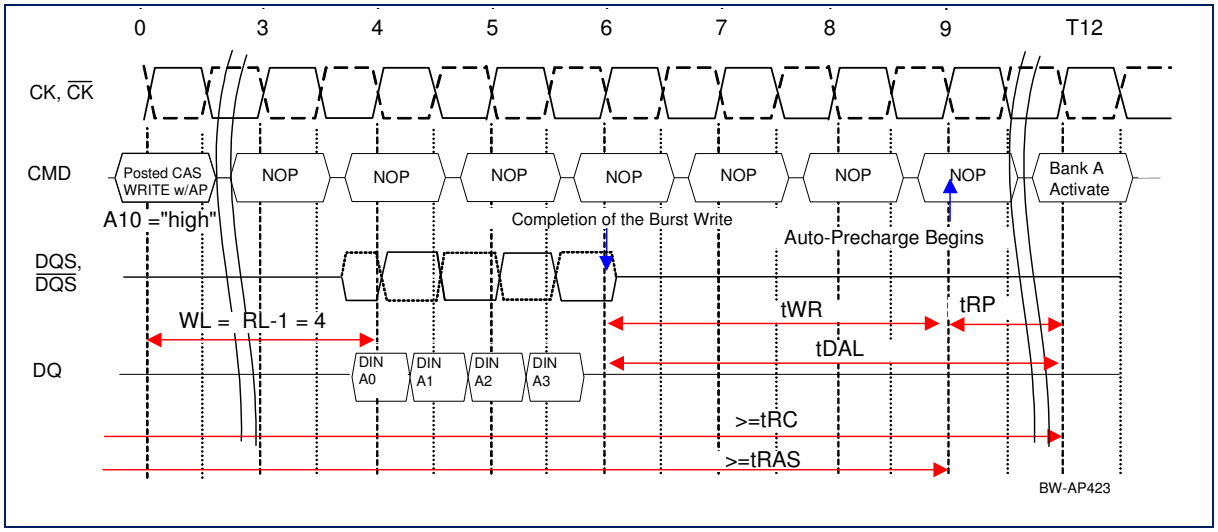
(2) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Examples:

Burst Write with Auto-Precharge (t_{RC} Limit): WL = 2, t_{DAL} = 6 (WR = 3, t_{RP} = 3), BL = 4



Burst Write with Auto-Precharge (t_{WR} + t_{RP} Limit) : WL = 4, t_{DAL} = 6 (t_{WR} = 3, t_{RP} = 3), BL = 4



Precharge & auto precharge clarification

From Command	To Command	Minimum Delay between "From command" to "to command"	Units	Note
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge All	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Read w/AP	Precharge (to same Bank as Read wAP)	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
	Precharge Al	AL + BL/2 + max(RTP,2) - 2	tCK	1,2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR	tCK	2
	Precharge Al	WL + BL/2 + tWR	tCK	2
Write w/AP	Precharge (to same bank as Write w/AP)	WL + BL/2 + WR	tCK	2
	Precharge Al	WL + BL/2 + WR	tCK	2
Precharge	Precharge (to same bank as Precharge)	1	tCK	2
	Precharge Al	1	tCK	2
Precharge All	Precharge	1	tCK	2
	Precharge Al	1	tCK	2

Note:

1) RTP [cycles] = RU {tRTP(ns)/tCK(ns)}, where RI stands for round up.

2) For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP or tRPa depending on the latest precharge command issued to that bank.

Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval t_{REFI}, which is a guideline to controlles for distributed refresh timing. For example, a 1Gbit DDR2 SDRAM has 8392 rows resulting in a t_{REFI} of 7.8 µs.

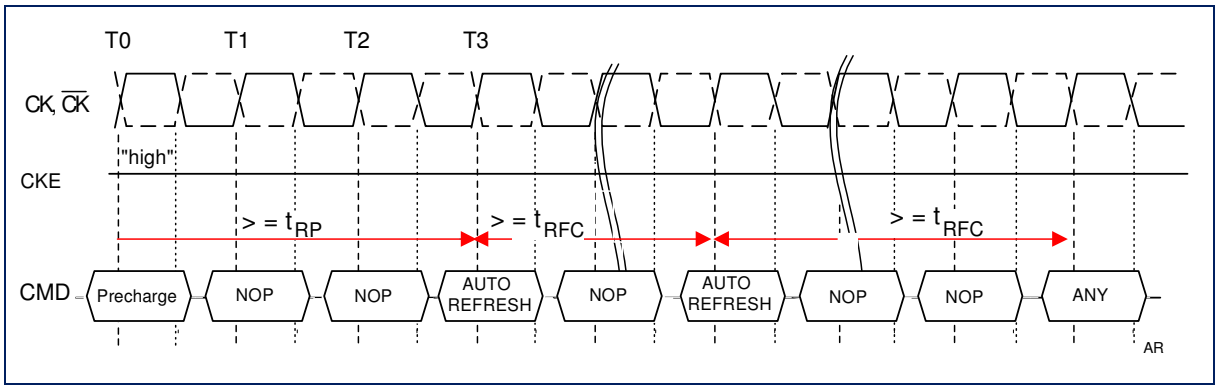
Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits ”Don’t Care” during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of t_{REFI} (maximum).

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time (t_{RP}) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time (t_{RFC}).

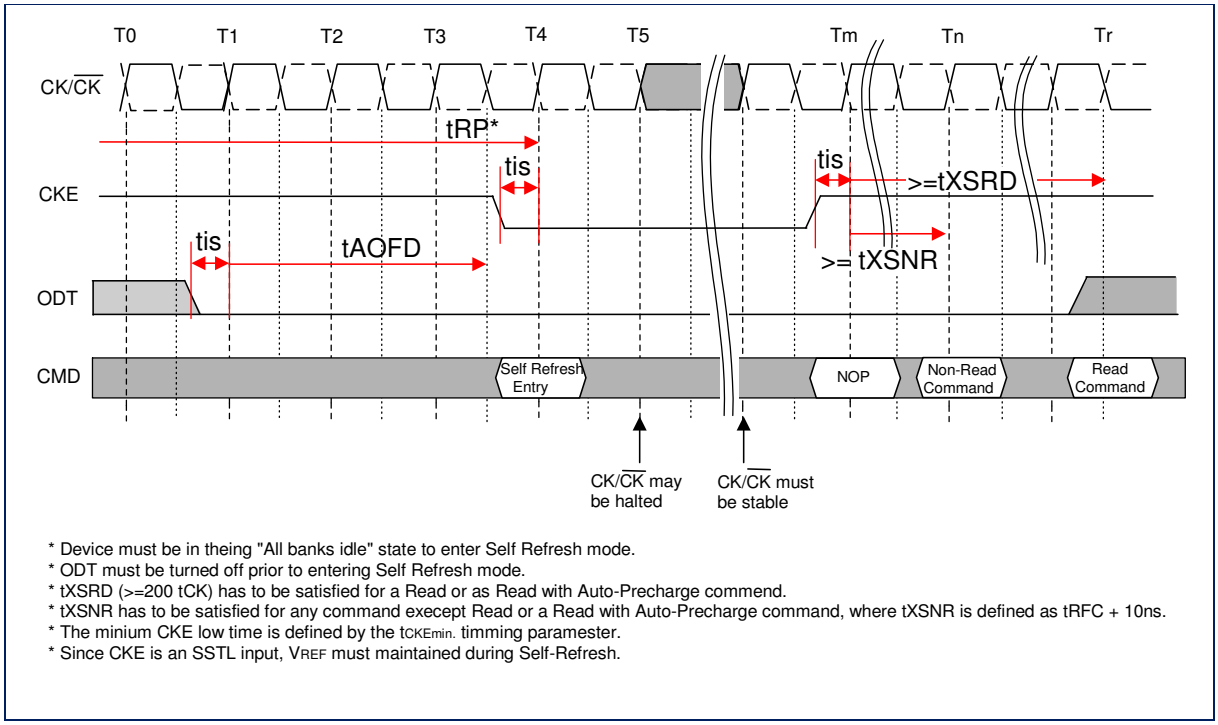
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * t_{REFI}.



Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{CKE}$ held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS (1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the t_{XSNR} or t_{XSRD} must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (t_{XSNR} or t_{XSRD}) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not supported during Self-Refresh operation, ODT has to be turned off t_{AOFD} before entering Self-Refresh Mode and can be turned on again when the t_{XSRD} timing is satisfied.



* Device must be in theing "All banks idle" state to enter Self Refresh mode.
* ODT must be turned off prior to entering Self Refresh mode.
* tXSRD (>=200 tCK) has to be satisfied for a Read or as Read with Auto-Precharge commend.
* tXSNR has to be satisfied for any command execept Read or a Read with Auto-Precharge command, where tXSNR is defined as tRFC + 10ns.
* The minium CKE low time is defined by the $t_{CKEmin.}$ timming paramester.
* Since CKE is an SSTL input, V_{REF} must maintained during Self-Refresh.

Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For Active *Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the t_{XARD} timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the t_{XARDS} timing parameter has to be satisfied.

Entering power-down deactivates the input and output buffers, excluding CK, CK, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, t_{XP}, t_{XARD} or t_{XARDS}, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

Power-Down Entry

Active Power-down mode can be entered after an activate command. *Precharge Power-down* mode can be entered after a precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when t_{MRD} is satisfied.

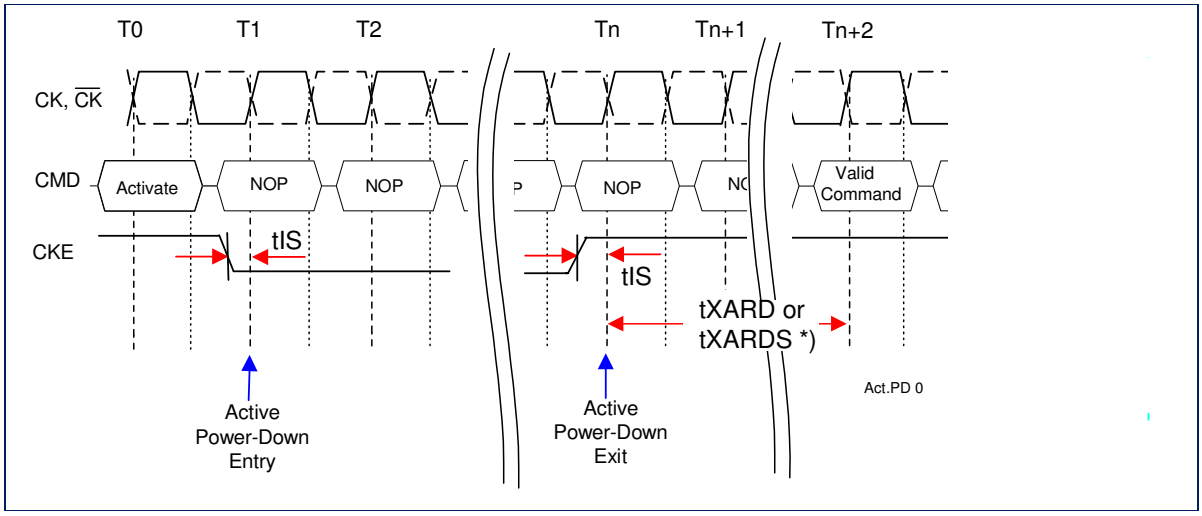
Active Power-down mode entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

Active Power-down mode entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed then WL + BL/2 + tWTR is satisfied.

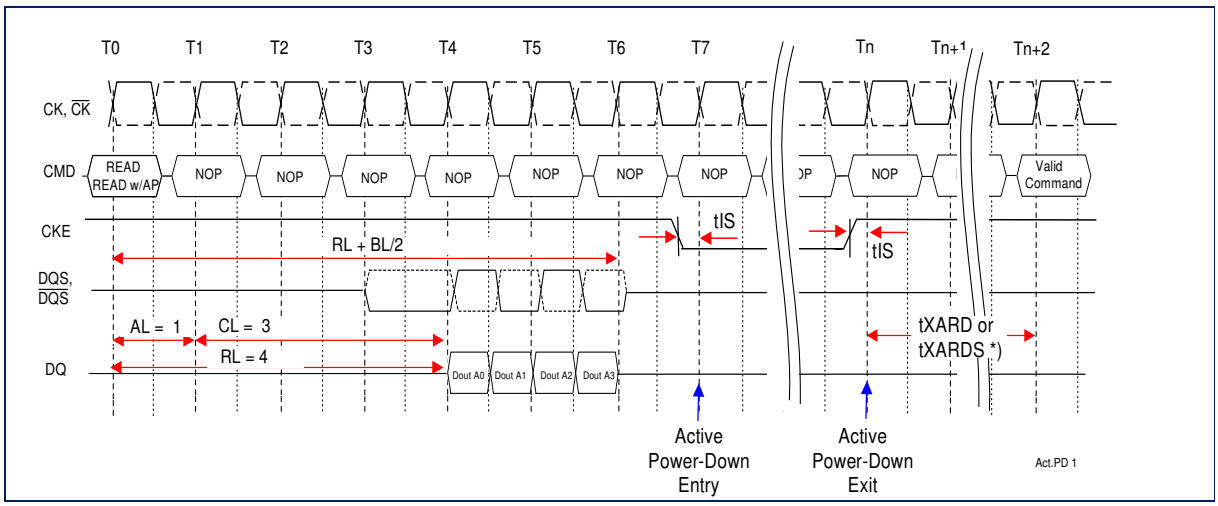
In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which WL + BL/2 + WR is starting from the write with Auto-Precharge command. In case the DDR2 SDRAM enters the *Precharge Power-down* mode.

Examples:

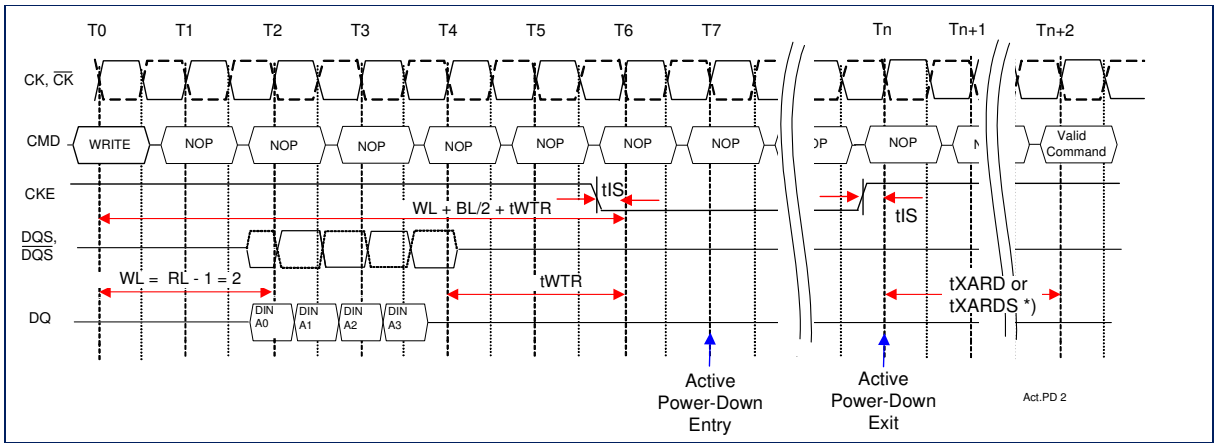
Active Power-Down Mode Entry and Exit after an Activate Command



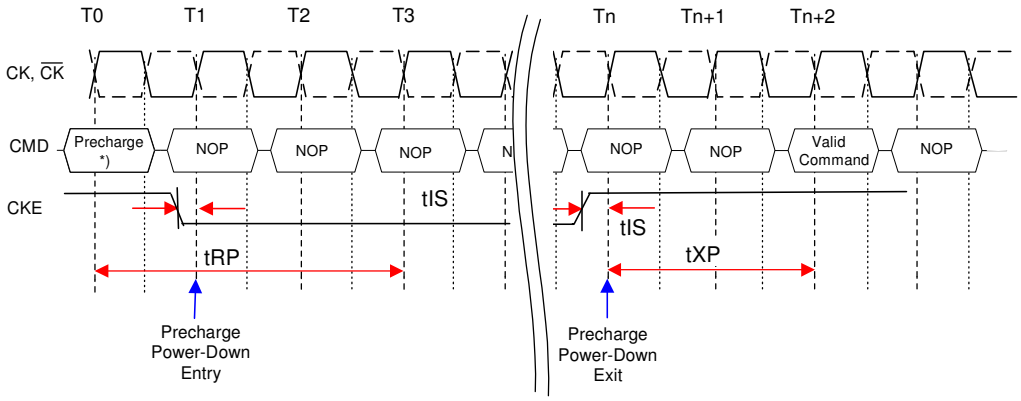
Active Power-Down Mode Entry and Exit after a Read Burst: RL = 4 (AL = 1, CL =3), BL = 4



Active Power-Down Mode Entry and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4



Precharge Power Down Mode Entry and Exit



*) "Precharge" may be an external command or an internal precharge following Write with AP.

PrePD

No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

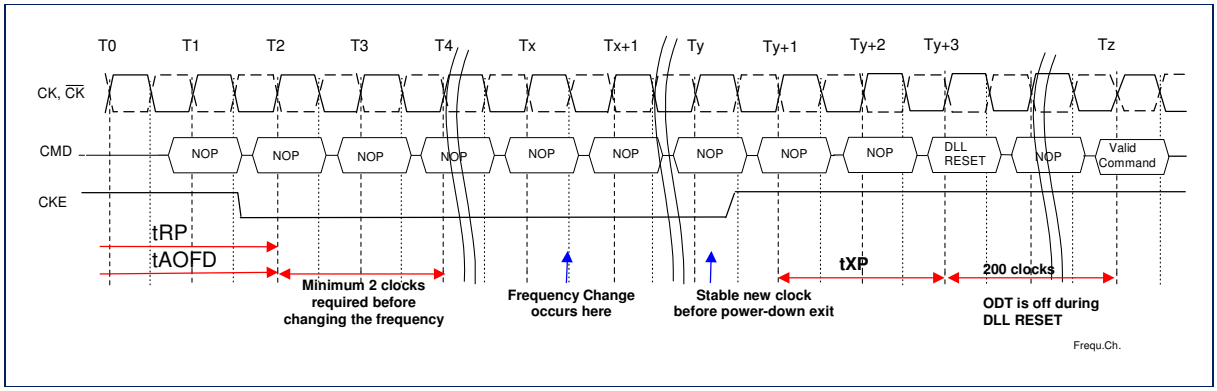
a) During Self-Refresh operation

b) DRAM is in Precharge Power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be allready turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After t_{XP} has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

Example:

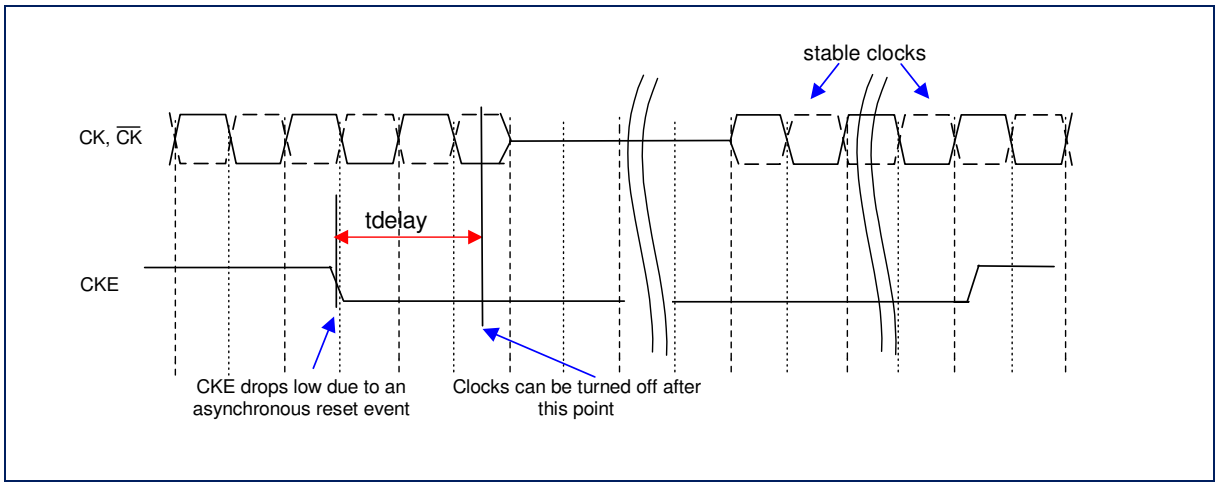
Input frequency change during Precharge Power-Down mode



Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay (t_{delay}) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the the initialization sequence (section 2.2.1, step 4 thru 13). DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for t_{delay} specification.

Asynchronous CKE Low Event



Truth Table

Command Truth Table

Function	CKE		CS	RAS	CAS	WE	BA0-BA2	A13-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	1
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	1,8
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7,8
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.

2. Bank addresses (BAx) determine which bank is to be operated upon. For (E) MRS BAx selects an (Extended) Mode Register.

3. Burst reads or writes at BL = 4 cannot be terminated. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" inspection for details.

4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined.

5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

6. X means "H or L (but a defined logic level)".

7. Self refresh exit is asynchronous.

8. Vref must be maintained during Self Refresh operation.

Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [2]	CKE		Command (N) [3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)			
Power-Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	DESELECT or NOP	Power-Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Self Refresh	11, 15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	4,8,10,11,13
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	4,8,10,11,13
	H	L	AUTOREFRESH	Self Refresh Entry	6, 9, 11,13
Any State other than listed above	H	H	Refer to the Command Truth Table		7

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.

3. Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).

4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.

6. Self Refresh mode can only be entered from the All Banks Idle state.

7. Must be a legal command as defined in the Command Truth Table.

8. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

9. Valid commands for Self Refresh Exit are NOP and DESELCT only.

10. Power-Down and Self Refresh cannot be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See section 2.8 "Power Down" and section 2.7.2 "Self Refresh Command" for a detailed list of restrictions.

11. Minimum CKE high time is 3 clocks, minimum CKE low time is 3 clocks.

12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

13. The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefore limited by the refresh requirements.

14. CKE must be maintained high while the device is in OCD calibration mode.

15. "X" means "don't care (including floating around VREF)" in Self Refresh and Power Down. However DT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in MRS(1)).

16. Vref must be maintained during Self Refresh operation

Operating Conditions

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on VDD pin relative to VSS	-1.0 to + 2.3	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to VSS	-0.5 to + 2.3	V	1,3
V_{DDL}	Voltage on VDDL pin relative to VSS	-0.5 to + 2.3	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to VSS	-0.5 to + 2.3	V	1
T_{STG}	Storage Temperature	-55 to + 100	℃	1, 2

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. When VDD, VDDQ, and VDDL are less than 500mV, Vref may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 85 (Standard Grade)	℃	1, 2
		- 40 to 95 (Industrial Grade)		1, 3

Note:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The operation temperature range is the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operation specification may be required. During operation, the DRAM case temperature must be maintained between 0℃-85℃ under all other specification parameter. However, in some applications, it is desirable to operate the DRAM up to 95 ℃ case temperature. Therefore, two spec. may exist. Supporting 0℃-85℃ with full JEDEC AC & DC spec. This is the minimum requirements for all operating temperature options.
This is an optional feature and not required. Supporting 0℃-85℃ and being able to extend to 95℃ with doubling auto-refresh command in frequency to a 32ms period (tRFI=3.9μs)
Currently the period Self-Refresh interval is hard coded within the DRAM to a vendor specific value. There is a migration plan to support higher temperature Self-Refresh entry via the control of EMRS (2) bit A7.
3. The operation temperature range is the temperature where all DRAM specification will be supported. Outside of this temperature range, even if it is still within the limit of stress condition, some deviation on portion of operation specification may be required. During operation, the DRAM case temperature must be maintained between -40-95 ℃ under all other specification parameter. However, in some applications, it is desirable to operate the DRAM up to 105 degree C case temperature. Therefore, two spec. may exist. Supporting -40℃-95℃ and being able to extend to 105℃

AC & DC Operating Conditions

DC Operating Conditions

Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	5
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1,5
V_{REF}	Input Reference Voltage	0.49 * V_{DDQ}	0.5 * V_{DDQ}	0.51 * V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

1. V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.

2. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

3. Peak to peak ac noise on V_{REF} may not exceed +/- 2% V_{REF} (dc).

4. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors is expected to be set equal to V_{REF} and must track variations in die dc level of VREF.

5. V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ}, and V_{DDL} tied together.

ODT DC Electrical Characteristic

Parameter / Condition	Symbol	min.	nom.	max.	Units	Notes
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohms	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 150 ohm	Rtt2(eff)	120	150	180	ohms	1
Rtt eff. impedance value for EMRS(1)(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohms	1
Deviation of VM with respect to VDDQ / 2	delta VM	-6		6	%	2

1) Measurement Definition for Rtt(eff):

Apply VIHac and VILac to test pin separately, then measure current I(VIHac) and I(VILac) respectively.

$$Rtt(eff) = \frac{(VIHac - VILac)}{(I(VIHac) - I(VILac))}$$

2) Measurement Definition for VM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\text{delta VM} = \left(\frac{2 * VM}{VDDQ} - 1\right) \times 100\%$$

DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the cross point of DQS and its complement, DQS. This distinction in timing methods is guaranteed by design and characterization. In single ended mode, the DQS (and RDQS) signals are internally disabled and don't care.

Single-ended DC & AC Logic Input Levels

Symbol	Parameter	DDR2-667/800/1066		Units
		Min.	Max.	
$V_{IH\ (dc)}$	DC input logic high	VREF + 0.125	VDDQ + 0.3	V
$V_{IL\ (dc)}$	DC input low	-0.3	VREF - 0.125	V
$V_{IH\ (ac)}$	AC input logic high	VREF + 0.200	VDDQ+Vpeak	V
$V_{IL\ (ac)}$	AC input low	VSSQ-Vpeak	VREF - 0.200	V

Single-ended AC Input Test Conditions

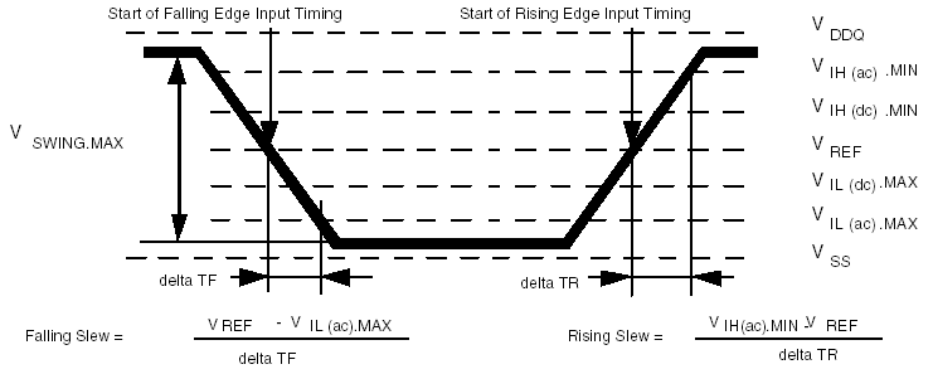
Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1, 2
$V_{SWING(max)}$	Input signal maximum peak to peak swing	1	V	1, 2
SLEW	Input signal minimum slew rate	1	V / ns	3, 4

1. This timing and slew rate definition is valid for all single-ended signals except tis, tih, tds, tdh.

2. Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.

3. The input signal minimum slew rate is to be maintained over the range from $V_{IL(dc)max}$ to $V_{IH(ac)min}$ for rising edges and the range from $V_{IH(dc)min}$ to $V_{IL(ac)max}$ for falling edges as shown in the below figure.

4. AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.



Differential DC and AC Input and Output Logic Levels

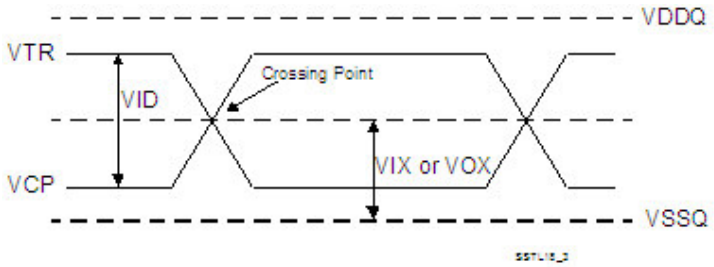
Symbol	Parameter	min.	max.	Units	Notes
$V_{ID(ac)}$	AC differential input voltage	0.5	VDDQ	V	1
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 * VDDQ - 0.125	0.5 * VDDQ + 0.125	V	3

Notes:

1) $V_{ID(ac)}$ specifices the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$.

2) $V_{IX(ac)}$ specifices the input differential voltage IVTR-VCPI required for switching, where VTR is the true input (such as CK, DQS, LDQS, or UDQS) level and VCP is the complementary input (such $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$, or $\overline{UDQS}$) level. The minimum value is equal to $V_{IH(DC)}$ - $V_{IL(DC)}$.

3) The typical value of $V_{OX(AC)}$ is expected to be about 0.5V_{DDQ} of the transmitting device and $V_{OX(AC)}$ is expected to track variations in V_{DDQ}. $V_{OX(AC)}$ indicates the voltage at which differential signals must cross.



Output Buffer Levels

Output AC Test Conditions

Symbol	Parameter	SSTL-18 Class II	Units	Notes
V_{OTR}	Output Timing Measurement Reference Level	0.5 * VDDQ	V	1

1. The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	SSTL-18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current, nominal	-13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current, nominal	13.4	mA	2, 3, 4

1. V_{DDQ} = 1.7 V; V_{OUT} = 1.42 V. (V_{OUT}-V_{DDQ}) / I_{OH} must be less than 21 ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280 mV.

2. V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT} / I_{OL} must be less than 21 ohm for values of V_{OUT} between 0V and 280 mV.

3. The dc value of V_{REF} applied to the receiving device is set to V_{TT}

4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in note 1 and 2. They are used to test drive current capability to ensure $V_{IHmin.}$ plus a noise margin and $V_{ILmax.}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 ohm load line to define a convenient current for measurement.

OCD Default Setting Table

Symbol	Description	Min.	Nominal	Max.	Unit	Notes
-	Pull-up / Pull down mismatch	0	-	4	Ohms	6
-	Output Impedance step size for OCD calibration	0	-	1.5	Ohms	1,2,3
S_{OUT}	Output Slew Rate	1.5	-	5	V / ns	1,4,5,7,8

1) Absolute Specification: T_{OPEN}; V_{DDQ} = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V.

2) Impedance measurement condition for output source dc current: V_{DDQ} = 1.7V, V_{OUT} = 1420 mV; (V_{OUT}-V_{DDQ})/I_{OH} must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ}-280mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7 V; V_{OUT} = -280mV; V_{OUT} / I_{OL} must be less than 23.4 ohms for values of V_{OUT} between 0V and 280 mV.

3) Mismatch is absolute value between pull-up and pull-down; both are measured at same temperature and voltage.

4) Slew rates measured from $V_{IL(AC)}$ to $V_{IH(AC)}$ with the load specified in Section 8.2.

5) The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

6) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 ohms under nominal conditions.

7) DRAM output slew rate specification applies to 533MT/s, 667MT/s, and 800MT/s speed pin.

8) Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQ's is included in tDQSQ and tQHS specification.

Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS (1) bits A7~A9 = ’111’. The driver characteristics evaluation conditions area) Nominal Default 25℃ (Tcase), VDDQ=1.8V, typical process. b) Minimum $T_{OPER(max)}$, VDDQ=1.7V, slow-slow process. c) Maximum 0℃ (Tcase), VDDQ=1.9V, fast-fast process

Full Strength Default Pullup Driver Characteristics

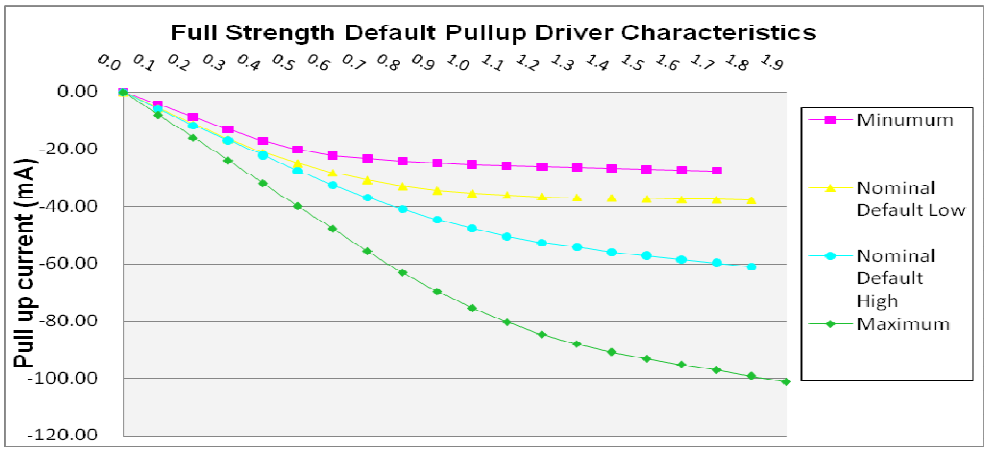
Voltage (V)	Minimum (23.4 Ohms)	Nomal Default low (18 Ohms)	Nomal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.0	0.00	0.00	0.00	0.00
0.1	-4.30	-5.65	-5.90	-7.95
0.2	-8.60	-11.30	-11.80	-15.90
0.3	-12.90	-16.50	-16.80	-23.85
0.4	-16.90	-21.20	-22.10	-31.80
0.5	-20.05	-25.00	-27.60	-39.75
0.6	-22.10	-28.30	-32.40	-47.70
0.7	-23.27	-30.90	-36.90	-55.55
0.8	-24.10	-33.00	-40.90	-62.95
0.9	-24.73	-34.50	-44.60	-69.55
1.0	-25.23	-35.50	-47.70	-75.35
1.1	-25.65	-36.10	-50.40	-80.35
1.2	-26.02	-36.60	-52.60	-84.55
1.3	-26.35	-36.90	-54.20	-87.95
1.4	-26.65	-37.10	-55.90	-90.70
1.5	-26.93	-37.40	-57.10	-93.00
1.6	-27.20	-37.60	-58.40	-95.05
1.7	-27.46	-37.70	-59.60	-97.05
1.8	-	-37.90	-60.90	-99.05
1.9	-	-	-	-101.05

The driver characteristics evaluetion conditions are:

Nominal Default 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Minimum Toper(max.), VDDQ = 1.7V, slow-slow process

Maximum 0 ℃ (Tcase). VDDQ = 1.9 V, fast-fast process



Full Strength Default Pulldown Driver Characteristics

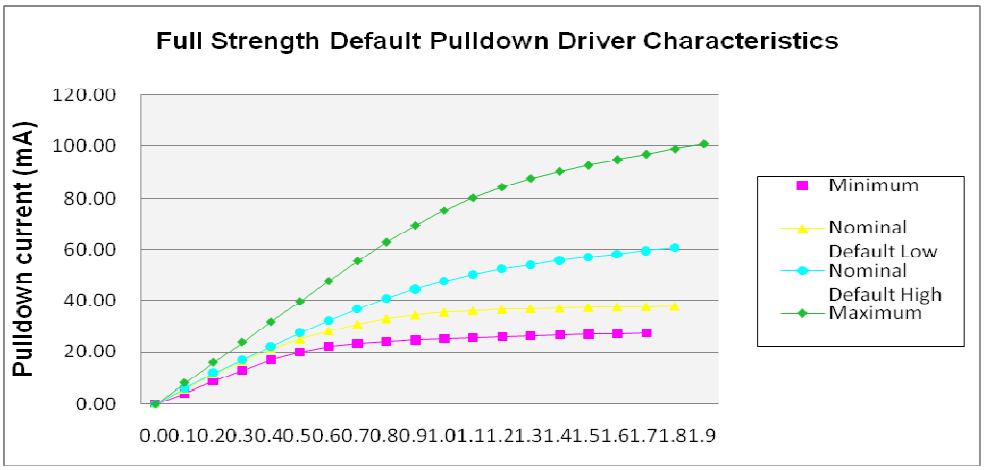
Voltage (V)	Minimum (23.4 Ohms)	Nomal Default low (18 Ohms)	Nomal Default high (18 Ohms)	Maximum (12.6 Ohms)
0.0	0.00	0.00	0.00	0.00
0.1	4.30	5.65	5.90	7.95
0.2	8.60	11.30	11.80	15.90
0.3	12.90	16.50	16.80	23.85
0.4	16.90	21.20	22.10	31.80
0.5	20.05	25.00	27.60	39.75
0.6	22.10	28.30	32.40	47.70
0.7	23.27	30.90	36.90	55.55
0.8	24.10	33.00	40.90	62.95
0.9	24.73	34.50	44.60	69.55
1.0	25.23	35.50	47.70	75.35
1.1	25.65	36.10	50.40	80.35
1.2	26.02	36.60	52.60	84.55
1.3	26.35	36.90	54.20	87.95
1.4	26.65	37.10	55.90	90.70
1.5	26.93	37.40	57.10	93.00
1.6	27.20	37.60	58.40	95.05
1.7	27.46	37.70	59.60	97.05
1.8	-	37.90	60.90	99.05
1.9	-	-	-	101.05

The driver characteristics evaluetion conditions are:

Nominal Default 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Minimum Toper(max.), VDDQ = 1.7V, slow-slow process

Maximum 0 ℃ (Tcase). VDDQ = 1.9 V, fast-fast process



Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The following tables show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedure, 1.5 ohm maximum step size guaranteed by specification). Real system calibration error needs to be added to these values. It must be understood that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this a system specific phenomena, it cannot be quantified here. the values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characteristics tables and figure. in such a situation, the timing parameters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, re-calibration policy and uncertainty with DQ to DQ variation, it is recommend that only the default values to be used. The nominal maximum ad minimum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

Full Strength Calibrated Pulldown Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Normal Low (18.75 Ohms)	Nominal (18 ohms)	Normal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

The driver characteristics evaluation conditions are:

Nominal 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Nominal Low and Nominal High 25℃ (Tcase), VDDQ = 1.8V, any process

Nominal Minimum Toper(max), VDDQ = 1.7 V, any process

Nominal Maximum 0℃(Tcase), VDDQ = 1.9 V, any process

Full Strength Calibrated Pullup Driver Characteristics

Voltage (V)	Nominal Minimum (21 Ohms)	Normal Low (18.75 Ohms)	Nominal (18 ohms)	Normal High (17.25 Ohms)	Nominal Maximum (15 Ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.6	-17.4	-20.0
0.4	-18.7	-21.0	-21.6	-23.0	-27.0

The driver characteristics evaluation conditions are:

Nominal 25℃ (Tcase) , VDDQ = 1.8 V, typical process

Nominal Low and Nominal High 25℃(Tcase), VDDQ = 1.8V, any process

Nominal Minimum Toper(max), VDDQ = 1.7 V, any process

Nominal Maximum 0℃ (Tcase), VDDQ = 1.9 V, any process

Symbol	Parameter	-3C/3CI		-AC/ACI		-BE		-BD		Units
		min.	max.	min.	max.	min.	max.	min.	max.	
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	-	0.25	-	0.25	-	0.25	-	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	2.0	1.0	1.75	1.0	1.75	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	-	0.25	-	0.25	-	0.25	-	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	2.5	3.5	2.5	3.5	2.5	3.5	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	-	0.5	-	0.5	-	0.5	-	0.5	pF

Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A0~A13, BA0, BA1, BA2), $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, WE, CKE, and ODT pins. The V-I characteristics for pins with clamps is shown in the following table

Voltage across clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

IDD Specifications and Measurement Conditions

IDD Specifications

(VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

Symbol	Parameter/Condition		I/O	-3C/-3CI	-AC/-ACI	-BE	-BD	Unit	Notes
IDD0	Operating Current		X4/x8 x16	65 100	70 115	TBD	TBD	mA	1,2
IDD1	Operating Current		X4/x8 x16	75 120	85 130	TBD	TBD	mA	1,2
IDD2P	Precharge Power-Down Current		All	7	7	TBD	TBD	mA	1,2
IDD2N	Precharge Standby Current		All	30	40	TBD	TBD	mA	1,2
IDD2Q	Precharge Quiet Standby Current		All	30	35	TBD	TBD	mA	1,2
IDD3P	Active Power-Down Standby Current	MRS(12)=0	All	25	30	TBD	TBD	mA	1,2
		MRS(12)=1	All	8	8	TBD	TBD	mA	1,2
IDD3N	Active Standby Current		X4/x8 x16	45 65	50 75	TBD	TBD	mA	1,2
IDD4R	Operating Current Burst Read		X4/x8 x16	100 150	120 235	TBD	TBD	mA	1,2
IDD4W	Operating Current Burst Write		X4/x8 x16	100 150	120 235	TBD	TBD	mA	1,2
IDD5B	Burst Auto-Refresh Current		X4/x8 x16	160 200	175 210	TBD	TBD	mA	1,2
IDD5D	Distributed Auto-Refresh Current		All	15	15	TBD	TBD	mA	1,2
IDD6	Self-Refresh Current for standard products		All	7	7	TBD	TBD	mA	1,2
IDD7	Operating Current		X4/x8 x16	210 260	250 330	TBD	TBD	mA	1,2

IDD Measurement Conditions

(VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

IDD1	Operating Current - One bank Active - Read - Precharge IOUT = 0 mA; BL = 4, tCK = tCKmin, tRC = tRCmin; tRAS = tRASmin; tRCD = tRCDmin, CL = CLmin.;AL = 0; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING,Data bus inputs are SWITCHING;
IDD2P	Precharge Power-Down Current: All banks idle; CKE is LOW; tCK = tCKmin.; Other control and address inputs are STABLE, Data Bus inputs are FLOATING.
IDD2N	Precharge Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address bus inputs are SWICHTING; Data bus inputs are SWITCHING.
IDD2Q	Precharge Quiet Standby Current:All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
IDD3P(0)	Active Power-Down Current: All banks open; tCK = tCKmin.;CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "0"(Fast Power-down Exit);
IDD3P(1)	Active Power-Down Current: All banks open; tCK = tCKmin.;CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "1"(Slow Power-down Exit);
IDD3N	Active Standby Current: All banks open; tCK = tCKmin.; tRAS = tRASmax.; tRP = tRPmin., CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; Other control and address inputs are SWITCHING; Data Bus inputs are SWITCHING.
IDD4R	Operating Current - Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin., CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; IOUT = 0mA.
IDD4W	Operating Current - Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.;CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.
IDD5B	Burst Auto-Refresh Current: tCK = tCKmin.; Refresh command every tRFC = tRFCmin interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and adress inputs are SWITCHING; Data bus
IDD5D	Distributed Auto-Refresh Current: tCK = tCKmin.; Refresh command every tREFI interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and adress inputs are SWITCHING; Data bus inputs
IDD6	Self-Refresh Current: CKE <= 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING.
IDD7	Operating Bank Interleave Read Current: 1. All bank interleaving reads; IOUT = 0 mA, BL =4, CL = CLmin., AL = tRCDmin. - 1*tCK; tCK = tCKmin., tRC = TRCmin.; tRRD = tRRDmin; tRCD = 1*tCK, CKE = HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS. 2. Timing pattern: - DDR2 -667 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D - DDR2 -800 5-5-5: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D - DDR2 -1066 6-6-6: A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D 3. Legend : A=Activate, RA=Read with Auto-Precharge, D=DESELECT

1. IDD specifications are tested after the device is properly initialized.
2. IDD parameter are specified with ODT disabled.
3. Data Bus consists of DQ, DM, DQS, DQS, RDQS, RDQS, LDQS, LDQS, UDQS and UDQS.
4. Definitions for IDD :
   LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.);
   STABLE is defined as inputs are stable at a HIGH or LOW level
   FLOATING is defined as inputs are VREF = VDDQ / 2
   SWITCHING is defined as:
   Inputs are changing between HIGH and LOW every other clock (once per two clocks) for adress and control signals, and
   inputs changing between HIGH and LOW every other clock (once per two clocks) for DQ signals not including mask or strobes
5. Timing parameter minimum and maximum values for IDD current measurements are defined in the following table.

IDD Measurement Conditions (cont'd)

For testing the IDD parameters, the following timing parameters are used:

Parameter		Symble	-3C/-3CI	-AC/-ACI	-BE	-BD	Units
Latency		CL	5	5	7	6	tCK(avg)
Clock Cycle Time		tCK	3	2.5	1.875	1.875	ns
Active to Read or Write delay		tRCD	15	12.5	13.125	11.25	ns
Active to Active / Auto-Refresh command period		tRC	60	57.5	58.125	56.25	ns
Active bank A to Active bank B command delay	**x8**	tRRD	7.5	7.5	7.5	7.5	ns
	x16		10	10	10	10	
Active to Precharge Command		tRASmin	45	45	45	45	ns
		tRASmax	70000	70000	70000	70000	
Precharge Command Period		tRP	15	12.5	13.125	11.25	ns

Refresh parameters

Parameter	Symbol	Component Type		1Gb	Unit
Auto-Refresh to Active / Auto-Refresh command period	tRFC	All		127.5	ns
Average periodic Refresh interval	tREFI	Standard Grade	(0℃ ≦Tcase≦85℃)	7.8	µs
			(85℃ ≦Tcase≦95℃)	3.9	
		Industry Grade	(-40℃ ≦Tcase≦95℃)	7.8	µs

Electrical Characteristics & AC Timing - Absolute Specification

Timing Parameter by Speed Grade

(VDDQ = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

Symbol	Parameter		-3C/-3CI		-AC/-ACI		-BE		-BD		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCK(avg)	Clock cycle time, CL=x, (Average)		3000	8000	2500	8000	1875	8000	1875	8000	ps
tCH(avg)	CK, $\overline{CK}$ high-level width (Average)		0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
tCL(avg)	CK, $\overline{CK}$ low-level width (Average)		0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
WL	Write command to DQS associated clock edge		RL-1								nCK
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)
tDSS	DQS falling edge to CK setup time		0.2	-	0.2	-	0.2	-	0.2	-	tCK(avg)
tDSH	DQS falling edge hold time from CK		0.2	-	0.2	-	0.2	-	0.2	-	tCK(avg)
tDQSL,H	DQS input low (high) pulse width		0.35	-	0.35	-	0.35	-	0.35	-	tCK(avg)
tWPRE	Write preamble		0.35	-	0.35	-	0.35	-	0.35	-	tCK(avg)
tWPST	Write postamble		0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK(avg)
tIS	Address and control input setup time		200	-	175	-	125	-	125	-	ps
tIH	Address and control input hold time		275	-	250	-	200	-	200	-	ps
tIPW	Address and control input pulse width (each input)		0.6	-	0.6	-	0.6	-	0.6	-	tCK(avg)
tDS	DQ and DM input setup time	differential	100	-	50	-	0	-	0	-	ps
tDH	DQ and DM input hold time	differential	175	-	125	-	75	-	75	-	ps

Symbol	Parameter	-3C/-3CI		-AC/-ACI		-BE		-BD		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tDIPW	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	0.35	-	tCK(avg)
tAC	DQ output access time from CK / $\overline{CK}$	-450	450	-400	400	-350	350	-350	350	ps
tDQSCK	DQS output access time from CK / $\overline{CK}$	-400	400	-350	350	-350	350	-350	350	ps
tHZ	Data-out high-impedance time from CK / $\overline{CK}$	-	tAC,max	-	tAC,max	-	tAC,max	-	tAC,max	ps
tLZ(DQS)	DQS($\overline{DQS}$) low-impedance time from CK / $\overline{CK}$	tAC,min	tAC,max	tAC,min	tAC,max	tAC,min	tAC,max	tAC,min	tAC,max	ps
tLZ(DQ)	DQ low-impedance time from CK / $\overline{CK}$	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	ps
tDQSQ	DQS-DQ skew (for DQS & associated DQ signals)	-	240	-	200	-	175	-	175	ps
tHP	Clock half period	Min (tCH(avg) tCL(avg))	-	Min (tCH(avg) tCL(avg))	-	Min (tCH(avg) tCL(avg))	-	Min (tCH(avg) tCL(avg))	-	ps
tQHS	Data hold skew factor	-	340	-	300	-	250	-	250	ps
tQH	Data output hold time from DQS	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	tHP - tQHS	-	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK(avg)
tRPST	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK(avg)
tRRD	Active bank A to Active bank B command period	7.5	-	7.5	-	7.5	-	7.5	-	ns
tFAW	Four Activate Window	37.5	-	35	-	35	-	35	-	ns
tCCD	$\overline{CAS}$ A to $\overline{CAS}$ B command period	2	-	2	-	2	-	2	-	nCK
tWR	Write recovery time	15	-	15	-	15	-	15	-	ns

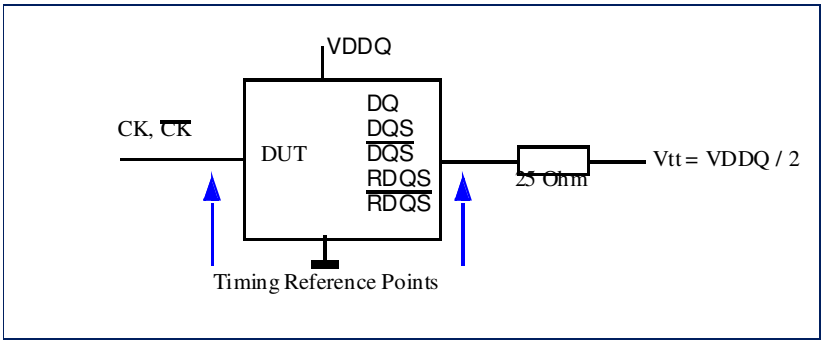
Symbol	Parameter	-3C/-3CI		-AC/-ACI		-BE		-BD		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tDAL	Auto-Precharge write recovery + precharge time	WR + tnRP	-	WR + tnRP	-	WR + tnRP	-	WR + tnRP	-	nCK
tWTR	Internal Write to Read command delay	7.5	-	7.5	-	7.5	-	7.5	-	ns
tRTP	Internal Read to Precharge command delay	7.5	-	7.5	-	7.5	-	7.5	-	ns
tCKE	CKE minimum high and low pulse width	3	-	3	-	3	-	3	-	nCK
tXSNR	Exit Self-Refresh to non-Read command	tRFC + 10	-	tRFC + 10	-	tRFC + 10	-	tRFC + 10	-	ns
tXSRD	Exit Self-Refresh to Read command	200	-	200	-	200	-	200	-	nCK
tXP	Exit precharge power-down to any valid command (other than NOP or Deselect)	2	-	2	-	3	-	3	-	nCK
tXARD	Exit power down to any valid command (other than NOP or Deselect)	2	-	2	-	3	-	3	-	nCK
tXARDS	Exit active power-down mode to Read command (slow exit, lower power)	7-AL	-	8-AL	-	10-AL	-	10-AL	-	nCK
tAOND	ODT turn-on delay	2	2	2	2	2	2	2	2	nCK
tAON	ODT turn-on	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 2.575	tAC,min	tAC,max + 2.575	ns
tAONPD	ODT turn-on (Power-Down mode)	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	tAC,min + 2	2 x tCK(avg) + tAC,max + 1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	nCK
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	ns

Symbol	Parameter	-3C/-3CI		-AC/-ACI		-BE		-BD		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tAOFPD	ODT turn-off (Power-Down mode)	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	tAC,min + 2	2.5 x tCK(avg) + tAC,max + 1	ns
tANPD	ODT to power down entry latency	3	-	3	-	2.5		2.5		nCK
tAXPD	ODT power down exit latency	8	-	8	-	11	-	11	-	nCK
tMRD	Mode register set command cycle time	2	-	2	-	2	-	2	-	nCK
tMOD	MRS command to ODT update delay	0	12	0	12	0	12	0	12	ns
tOIT	OCD drive mode output delay	0	12	0	12	0	12	0	12	ns
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS + tCK(avg) + tIH	-	tIS + tCK(avg) + tIH	-	tIS + tCK(avg) + tIH	-	tIS + tCK(avg) + tIH	-	ns

Reference Loads, Setup & Hold Timing Definition and Slew Rate Derating

Reference Load for Timing Measurements

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial transmission line terminated at the tester electronics. This reference load is also used for output slew rate characterization.



The output timing reference voltage level for single ended signals is the cross point with VTT.

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. $\overline{\text{DQS}}$) signal.

Slew rate Measurements

Output Slew rate

With the reference load for timing measurements output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS / $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = - 500 mV and DQS - $\overline{DQS}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

Input Slew rate - Differential signals

Input slew rate for differential signals (CK / $\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$) for rising edges are measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = + 500 mV and from CK - CK = +250 mV to CK - CK = - 500mV for falling edges.

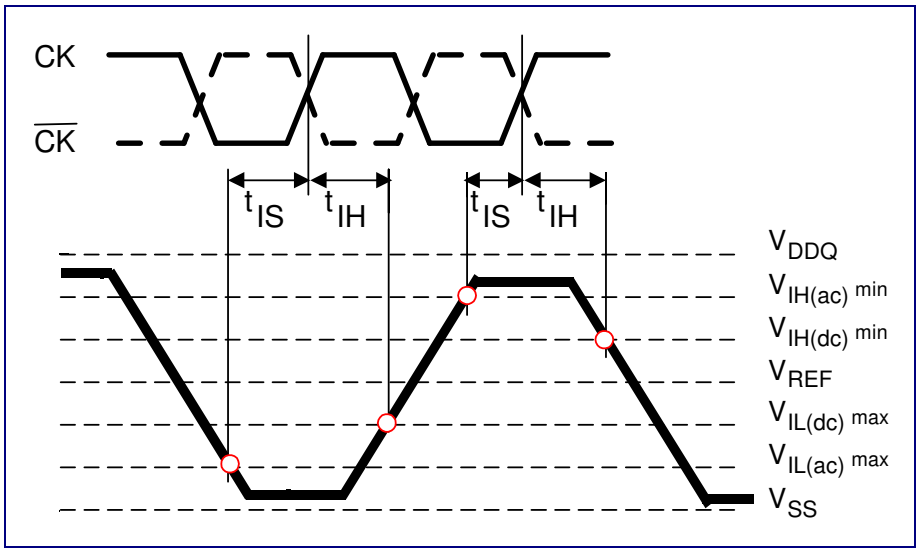
Input Slew rate - Single ended signals

Input slew rate for single ended signals (other than tis, tih, tds and tdh) are measured from dc-level to ac-level: VREF -125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV to VREF - 250 mV for falling edges. For slew rate definition of the input and data setup and hold parameters see section 8.3 of this datasheet.

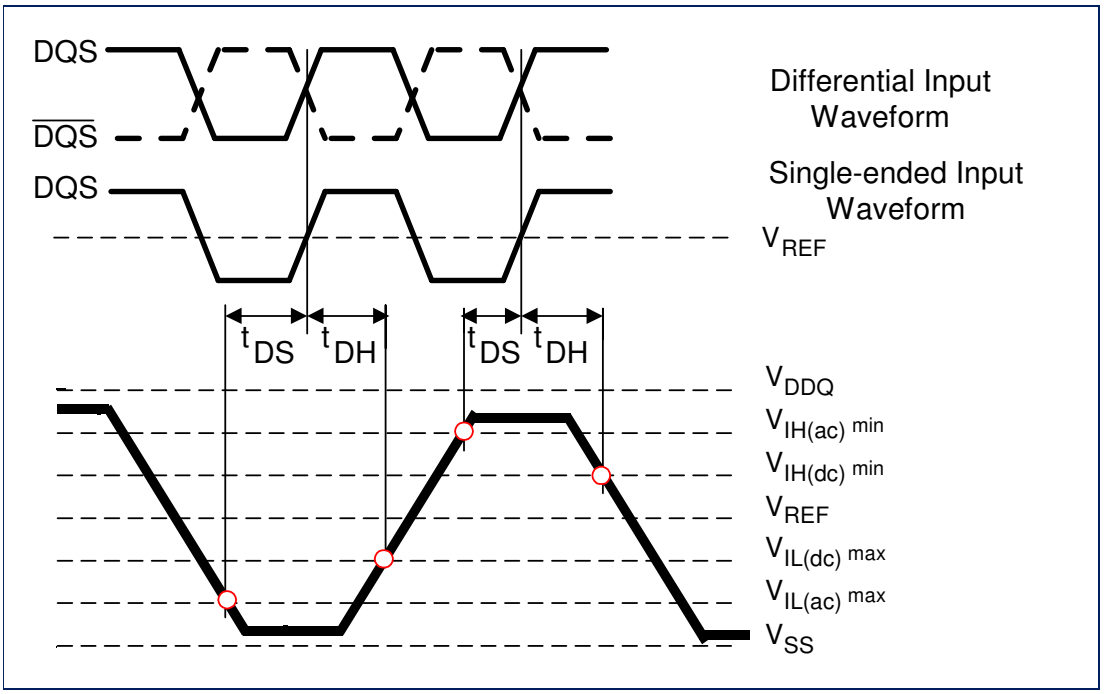
Input and Data Setup and Hold Time

Timing Definition for Input Setup (t_{IS}) and Hold Time (t_{IH})

Address and control input setup time (t_{IS}) is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test. Address and control input hold time (tIH) is referenced from the input signal crossing at the $V_{IL(dc)}$ level for a rising signal and $V_{IH(dc)}$ for a falling signal applied to the device under test



Timing Definition for Data Setup (t_{DS}) and Hold Time (t_{DH})



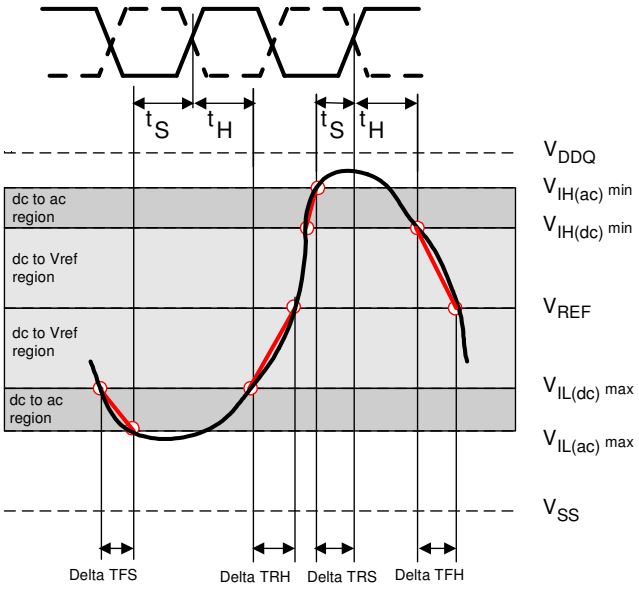
1. Data input setup time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level to differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIH(ac) level to the data strobe crossing Vref for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing Vref for a falling signal applied to the device under test.

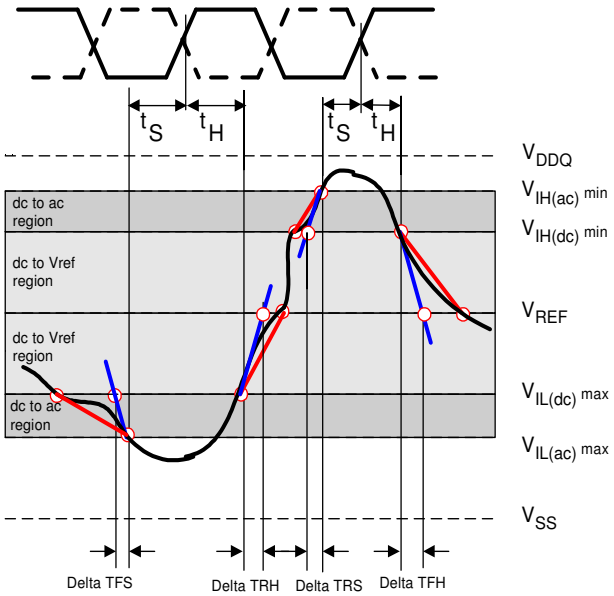
2. Data input hold time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIL(dc) level to the differential data strobe crosspoint for a rising signal and VIH(dc) to the differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing Vref for a rising signal and VIH(dc) to the single-ended data strobe crossing Vref for a falling signal applied to the device under test

Slew Rate Definition for Input and Data Setup and Hold Times

Setup (tIS & tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VIH(ac)min. Setup (tIS & tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VIL(ac)max, (fig. A) If the actual signal is always earlier than the nominal slew rate line between shaded 'dc to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'dc to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.(fig.B)

Hold (tIH & tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref.(fig. A). If the actual signal is always later than the nominal slew rate line between shaded 'dc to Vref region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref region', the slew rate of a tangent line to the actual signal from the dc level to Vref level is used for derating value.(fig.B)





$$\text{Setup Slew Rate} = \frac{\text{VIL(dc)max - VIL(ac)max}}{\text{Delta TFS}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{VIH(dc)min - VIL(ac)min}}{\text{Delta TRS}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VREF - VIL(dc)max}}{\text{Delta TRH}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VIH(dc)min - VREF}}{\text{Delta TFH}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{tangent line [VIL(dc)max - VIL(ac)max]}}{\text{Delta TFS}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{tangent line [VIH(dc)min - VIL(ac)min]}}{\text{Delta TRS}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{tangent line [REF - VIL(dc)max]}}{\text{Delta TRH}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VIH(dc)min - VREF]}}{\text{Delta TFH}} \quad \text{falling signal}$$

Input Setup (t_{IS}) and Hold (t_{IH}) Time DeratingTable

Command/Address Slew rate (V/ns)	CK, $\overline{CK}$ Differential Slew Rate						Units
	(-3C/-3Cl/-AC/-ACl/-BE/-BD)						
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	D tIS	D tIH	D tIS	D tIH	D tIS	D tIH	
4.00	150	94	180	124	210	154	ps
3.50	143	89	173	119	203	149	ps
3.00	133	83	163	113	193	143	ps
2.50	120	75	150	105	180	135	ps
2.00	100	45	130	75	160	105	ps
1.50	67	21	97	51	127	81	ps
1.00	0	0	30	30	60	60	ps
0.90	-5	-14	25	16	55	46	ps
0.80	-13	-31	17	-1	47	29	ps
0.70	-22	-54	8	-24	38	6	ps
0.60	-34	-83	-4	-53	26	-23	ps
0.50	-60	-125	-30	-95	0	-65	ps
0.40	-100	-188	-70	-158	-40	-128	ps
0.30	-168	-292	-138	-262	-108	-232	ps
0.25	-200	-375	-170	-345	-140	-315	ps
0.20	-325	-500	-295	-470	-265	-440	ps
0.15	-517	-708	-487	-678	-457	-648	ps
0.10	-1000	-1125	-970	-1095	-940	-1065	ps

Data Setup (tDS) and Hold Time (tDH) Derating Table

DQ Slewrate (V/ns)	DQS, $\overline{DQS}$ Differential Slew Rate (-3C/-3CI/-AC/-ACI/-BE/-BD)																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH	D tDS	D tDH
2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

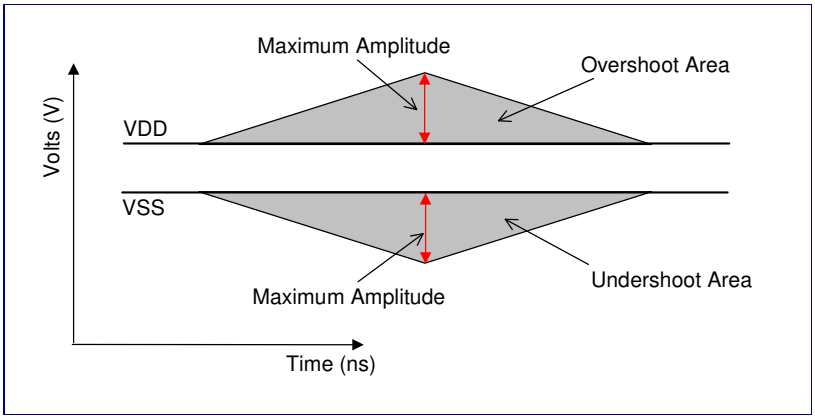
1. All units in ps.

2. For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the individual datasheet value to the derating value listed in the previous table

Overshoot and Undershoot Specification

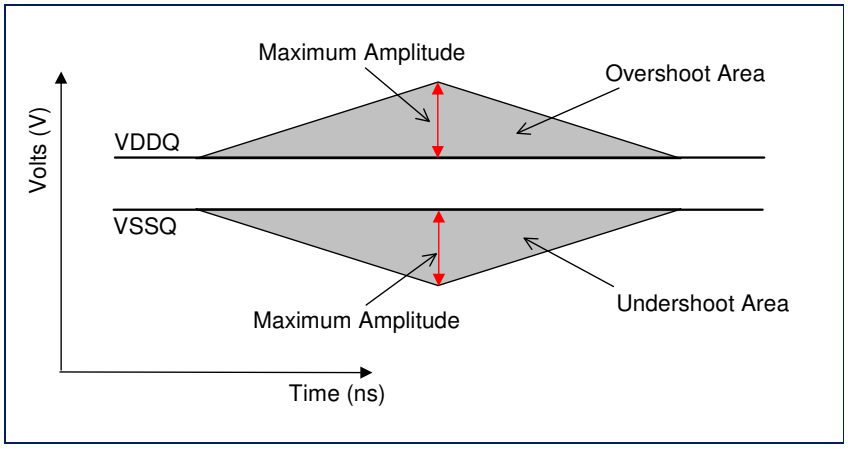
AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	-3C/-3CI	-AC/-ACI	-BE	-BD	Units
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.8	0.66	0.66	0.66	V-ns
Maximum undershoot area below VSS	0.8	0.66	0.66	0.66	V-ns



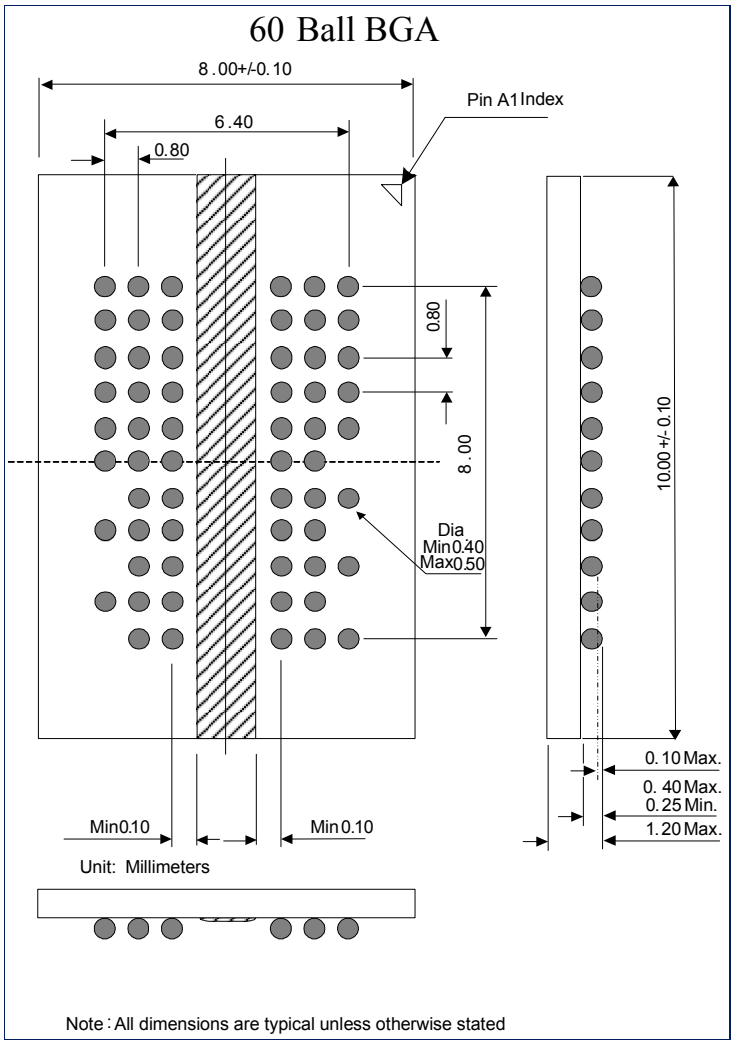
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	-3C/-3CI	-AC/-ACI	-BE	-BD	Units
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	0.5	V
Maximum overshoot area above VDD	0.23	0.23	0.23	0.23	V.ns
Maximum undershoot area below VSS	0.23	0.23	0.23	0.23	V.ns



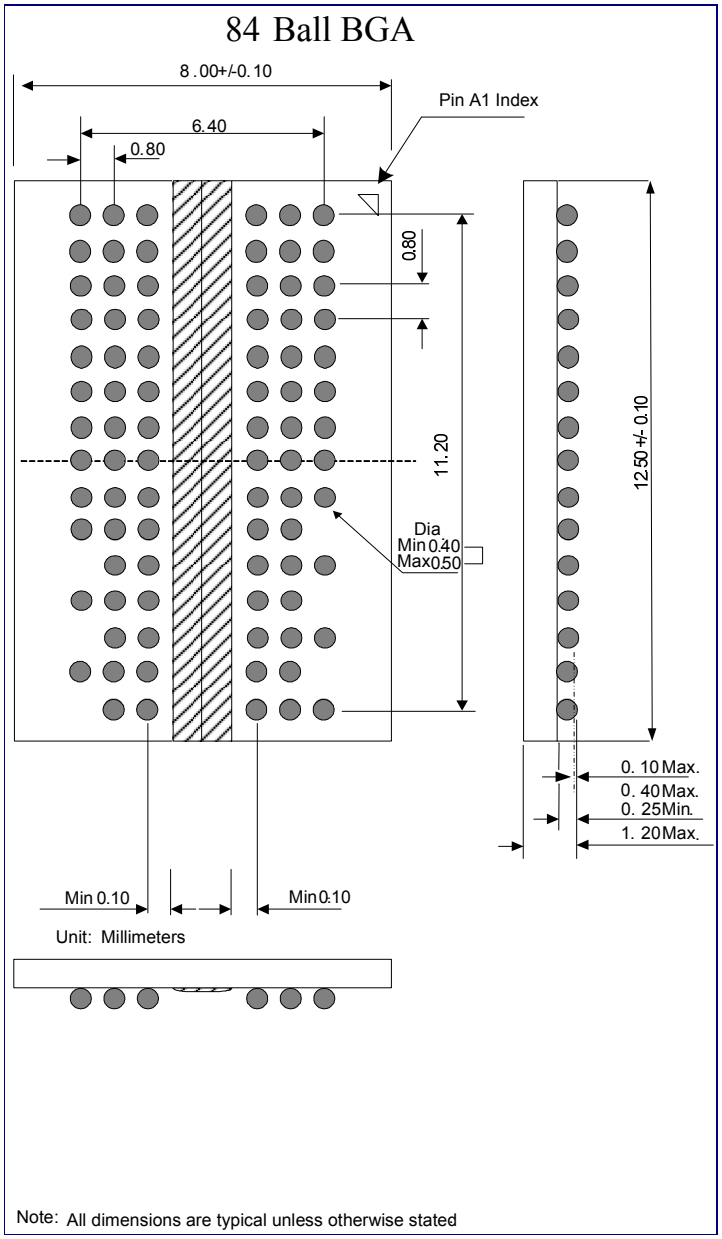
Package Dimensions

(x4/x8; 60 balls; BGA Package)



Package Dimensions

(X16; 84 balls; BGA Package)



Revision Log

Rev	Date	Modification
0.1	11/2009	Preliminary Release
1.0	12/2009	Official Release
1.1	5/2010	Modified the typo on page 8
1.2	5/2010	Add the timing specificity of DDR2-1066 (-BE)
1.3	6/2010	Modified the typos on the page 1 and page 76.

Nanya Technology Corporation.

Printed in Taiwan, R.O.C., 2006

NANYA TECHNOLOGY CORPORATION (NTC) reserves the right to make changes without notice. NTC warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with NTC's standard warranty. Testing and other quality control techniques are utilize to the extent NTC deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

NTC SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTEND, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of NTC products in such applications is understood to be fully at the risk of the customer. Use of NTC products in such applications requires the written approval of an appropriate NTC officer. Question concerning potential risk applications should be directed to NTC through a local sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by customer to minimize the inherent or procedural hazards.NTC assumes no liability of applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does NTC warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of NTC covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

NANYA TECHNOLOGY CORPORATION

HWA YA Technology Park, 669, FU HSING 3rd Rd., Kueishan,

Taoyuan, Taiwan, R.O.C.

The NANYA TECHNOLOGY CORPORATION

Home page can be found at http:\\www.nanya.com