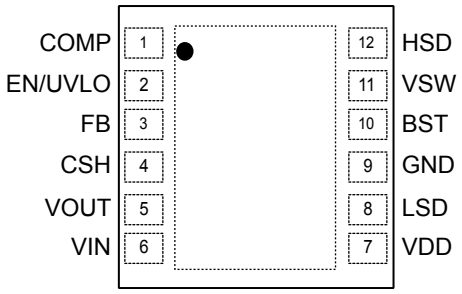
Ordering Information

Part Number		Voltage	Temperature Range	Package
Standard	**Pb-Free**			
MIC2199BML	MIC2199YML	Adj	−40ºC to +125ºC	12-Pin 4x4 MLF®

Pin Configuration



12-Pin 4×4 MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	COMP	Compensation (Output): Internal error amplifier output. Connect to capacitor or series RC network to compensate the regulator control loop.
2	EN/UVLO	Enable/Undervoltage Lockout (Input): Low-level signal powers down the controller. Input below the 2.5V threshold disables switching and functions as an accurate undervoltage lockout (UVLO). Input below the threshold forces complete micropower (<0.1µA) shutdown.
3	FB	Feedback (Input): Regulates FB pin to 0.8V. See *"Applications Information"* for resistor divider calculations.
4	CSH	Current-Sense High (Input): Current limit comparator non-inverting input. A built-in offset of 100mV between CSH and V_{OUT} pins in conjunction with the current-sense resistor set the current limit threshold level. This is also the non-inverting input to the current sense amplifier.
5	VOUT	Current-Sense Low (Input): Output voltage feedback input and inverting input for the current limit comparator and the current sense amplifier.
6	VIN	Unregulated Input (Input): +4.5V to +32V supply input.
7	VDD	5V Internal Linear-Regulator (Output): V_{DD} is the external MOSFET gate drive supply voltage and internal supply bus for the IC. Bypass to GND with 4.7µF.
8	LSD	Low-Side Drive (Output): High-current driver output for low-side N-Channel MOSFET. Voltage swing is between ground and V_{DD}.
9	GND	Ground (Return).
10	BST	Boost (Input): Provides drive voltage for the high-side MOSFET driver. The drive voltage is higher than the input voltage by V_{DD} minus a diode drop.
11	VSW	Switch (Return): High-side MOSFET driver return.
12	HSD	High-Side Drive (Output): High-current driver output for high-side MOSFET. This node voltage swing is between ground and V_{IN} +5V minus a diode drop.

Absolute Maximum Ratings (Note 1)

Analog Supply Voltage (V_{IN}) ..... +34V
Digital Supply Voltage (V_{DD}) ..... +7V
Driver Supply Voltage (B_{ST}) ..... V_{IN} + 7V
Sense Voltage (V_{OUT}, C_{SH}) ..... 7V to –0.3V
Enable Pin Voltage ($V_{EN/UVLO}$) ..... V_{IN}
Power Dissipation (P_D)
4×4 MLF™ ..... 665mW @ T_A = 85°C
Ambient Storage Temperature (T_S) ..... –65°C to +150°C
ESD, **Note 3**

Operating Ratings (Note 2)

Analog Supply Voltage (V_{IN}) ..... +4.5V to +32V
Output Voltage Range (V_{OUT}) ..... +0.8V to +6V
Junction Temperature (T_J) ..... –40°C to +125°C
Package Thermal Resistance
4×4 MLF-12L (θ_{JA}) ..... 60°C/W

Electrical Characteristics (Note 4)

V_{IN} = V_{EN} = 12V; T_J = 25°C, unless noted, **bold** values indicate –40°C ≤ T_J ≤ +125°C

Parameter	Condition	Min	Typ	Max	Units
Feedback Voltage Reference	(±1%)	0.792	0.8	0.808	V
Feedback Voltage Reference	(±2%)	**0.784**		**0.816**	V
Feedback Voltage Reference	4.5V < V_{IN} < 32V, 0 < (V_{CSH} – V_{OUT}) < 60mV (±3%)	**0.776**		**0.824**	V
Feedback Bias Current			10		nA
Output Voltage Range		0.8		6	V
Output Voltage Line Regulation	V_{IN} = 4.5V to 32V, V_{CSH} – V_{OUT} = 60mV		0.03		%/V
Output Voltage Load Regulation	25mV < (V_{CSH} – V_{OUT}) < 60mV		0.5		%
Input and V_{DD} Supply					
Quiescent Current	excluding external MOSFET gate drive current		1.6	**2.5**	mA
Shutdown Quiescent Current	$V_{EN/UVLO}$ = 0V		0.1	**5**	µA
Digital Supply Voltage (V_{DD})	I_L = 0mA to 5mA	4.7	5.0	5.3	V
Undervoltage Lockout	V_{IN} upper threshold (turn-on threshold)		4.25	4.4	V
	V_{IN} lower threshold (turn-off threshold)	3.95	4.1		V
Enable/UVLO					
Enable Input Threshold		**0.6**	1.1	**1.6**	V
UVLO Threshold		**2.2**	2.5	**2.8**	V
Enable Input Current	$V_{EN/UVLO}$ = 5V		0.1	**5**	µA
Current Limit					
Current Limit Threshold Voltage	(V_{CSH} – V_{OUT})	**55**	75	**95**	mV
Error Amplifier					
Transconductance Error Amplifier GM			0.2		mS
Oscillator Section					
Oscillator Frequency		270	300	330	kHz
Maximum Duty Cycle		80	85		%
Minimum On-Time			170	200	ns
Frequency Foldback Threshold	measured at V_{OUT} pin	0.25	0.40	0.55	V
Foldback Frequency			75		kHz
Gate Drivers					
Rise/Fall Time	C_L = 3000pF		60		ns
Output Driver Impedance	source		5	**8.5**	Ω
	sink		3.5	**6**	Ω
Driver Non-Overlap Time			80		ns

Note 1. Exceeding the absolute maximum rating may damage the device.

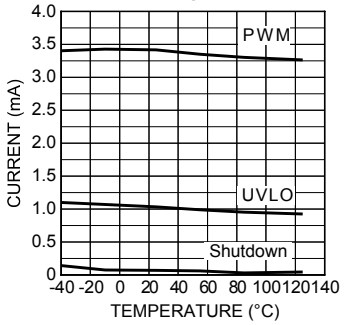
Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD protected; however, handling precautions are recommended. Human body model, 1.5k in series with 100pF.

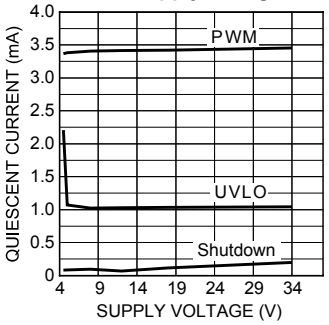
Note 4. Specification for packaged product only.

Typical Characteristics

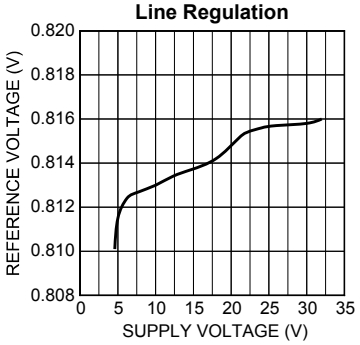
Quiescent Current vs. Temperature



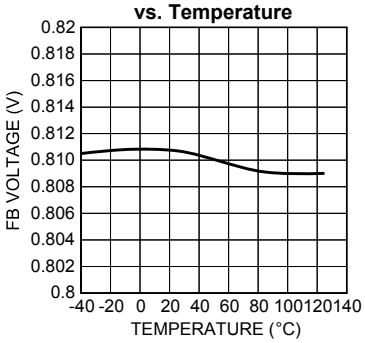
Quiescent Current vs. Supply Voltage



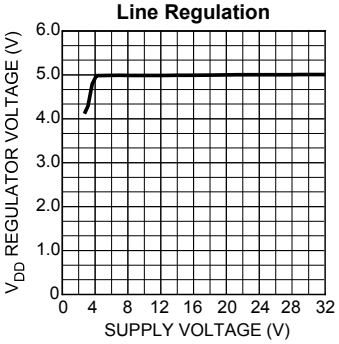
V_{FB} Line Regulation



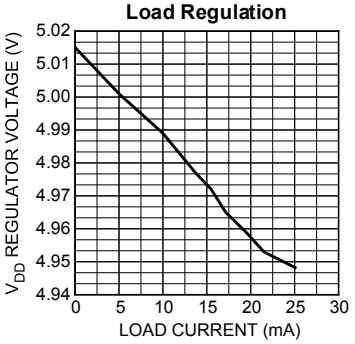
V_{FB} vs. Temperature



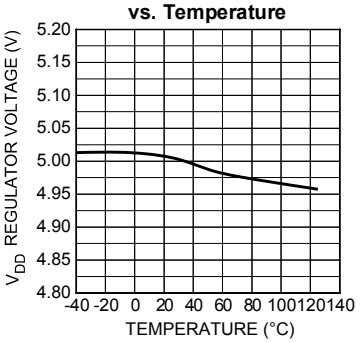
V_{DD} Line Regulation



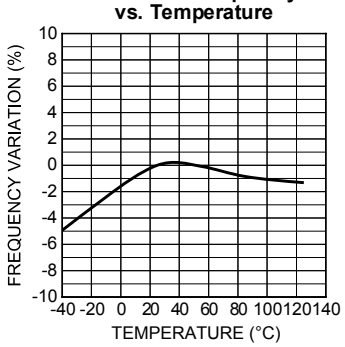
V_{DD} Load Regulation



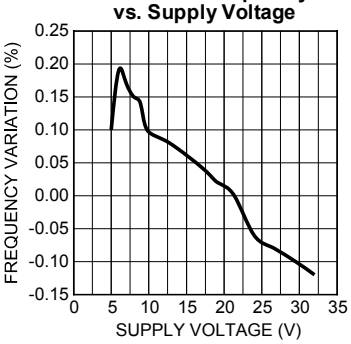
V_{DD} vs. Temperature



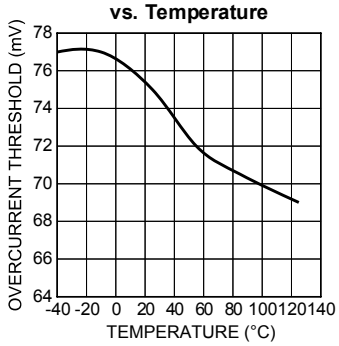
Oscillator Frequency vs. Temperature



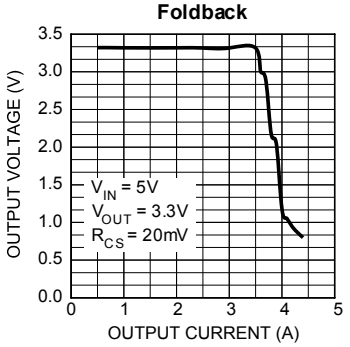
Oscillator Frequency vs. Supply Voltage



Overcurrent Threshold vs. Temperature



Current Limit Foldback



Block Diagram

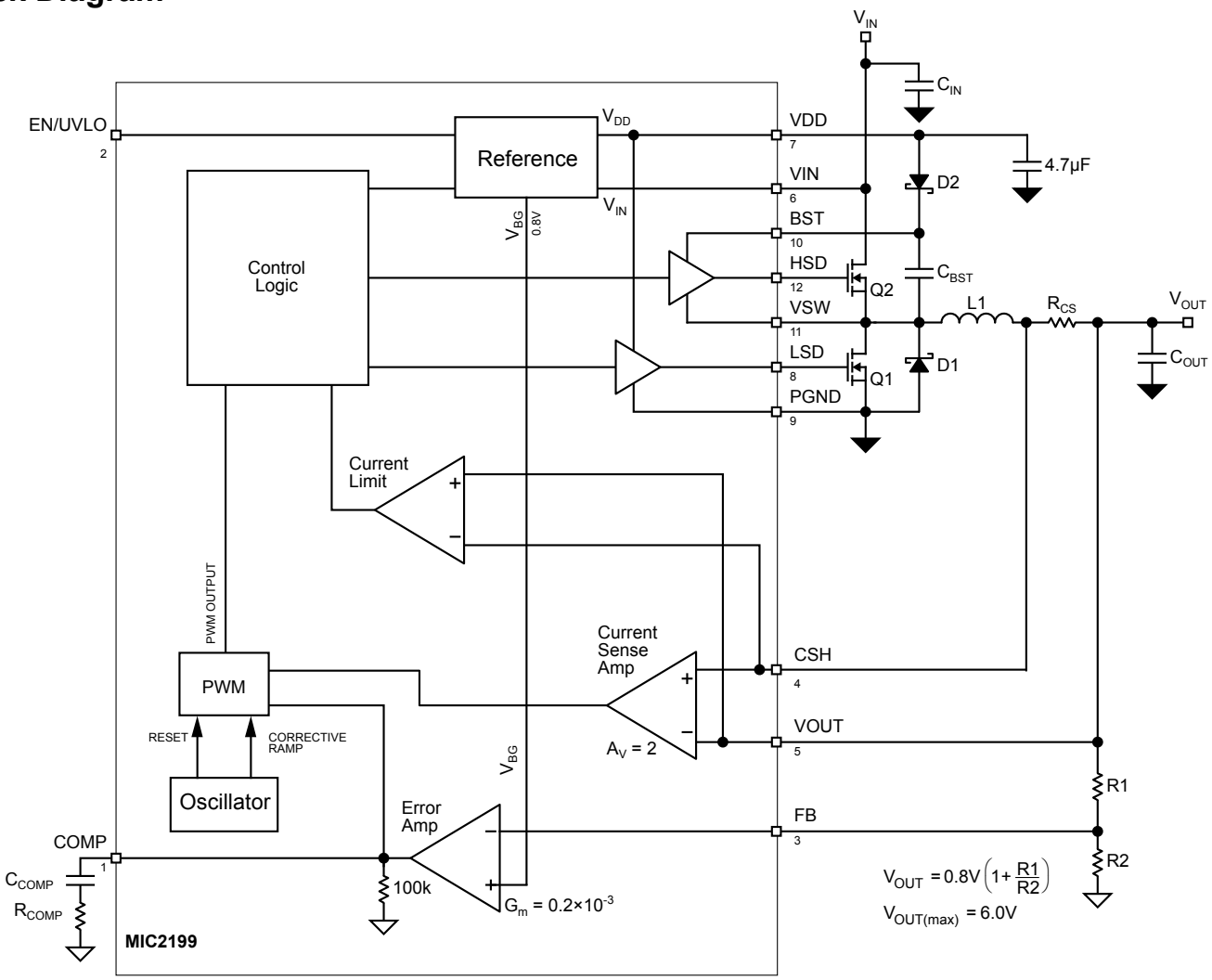


Figure 1. Internal Block Diagram

Functional Description

The MIC2199 is a BiCMOS, switched-mode, synchronous step-down (buck) converter controller. Current-mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above a 50% duty cycle. The controller is optimized for high-efficiency, high-performance DC-DC converter applications.

The MIC2199 block diagram is shown above.

The MIC2199 controller is divided into 5 functions.

- Control loop
- Current limit
- Reference, enable and UVLO
- MOSFET gate drive
- Oscillator

Control Loop

The MIC2199 operates in PWM (pulse-width-modulation) mode. In PWM mode, the synchronous buck converter forces continuous current to flow in the inductor which also improves cross regulation of transformer coupled, multiple output configurations.

PWM Control Loop

The MIC2199 uses current-mode control to regulate the output voltage. This method senses the output voltage (outer loop) and the inductor current (inner loop). It uses inductor current and output voltage to determine the duty cycle of the buck converter. Sampling the inductor current removes the inductor from the control loop, which simplifies compensation.

A block diagram of the MIC2199 PWM current-mode control loop is shown in Figure 2 and the PWM mode voltage and current waveform is shown in Figure 3. The inductor current is sensed by measuring the voltage across the resistor, R_{CS}.

A ramp is added to the amplified current-sense signal to provide slope compensation, which is required to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a reference voltage. The output of the error amplifier is the COMP (compensation) pin, which is compared to the current-sense waveform in the PWM block. When the current signal becomes greater than the error signal, the comparator turns off the high-side drive. The COMP pin (pin 1) provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

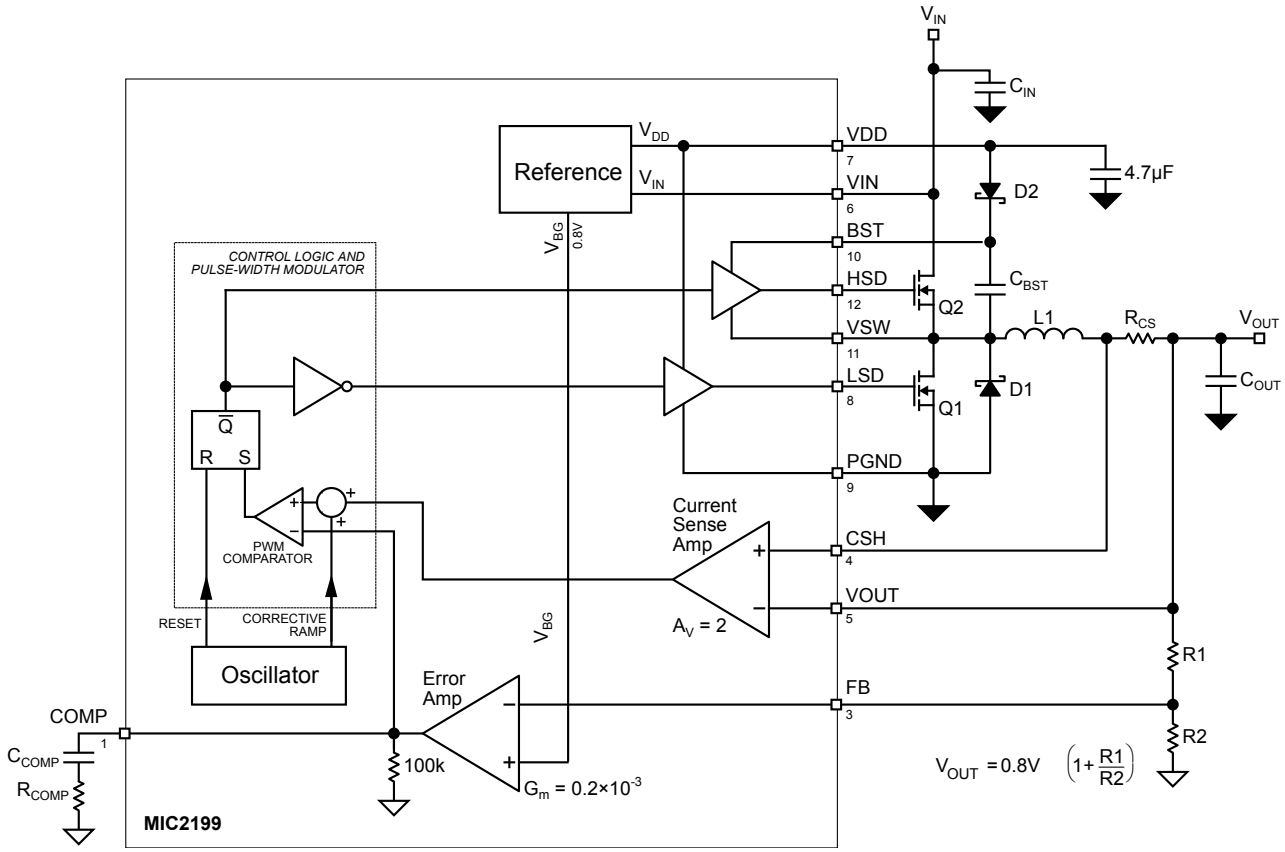


Figure 2. PWM Operation

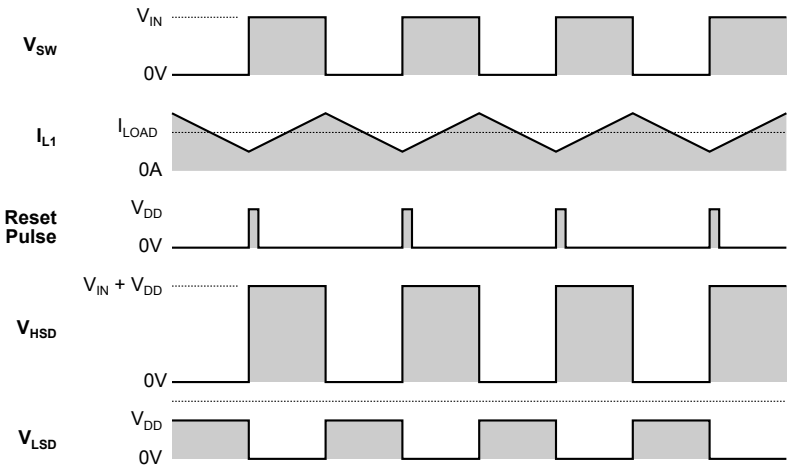


Figure 3. PWM-Mode Timing

Current Limit

The MIC2199 output current is detected by the voltage drop across the external current-sense resistor (R_{CS} in Figure 2.). The current limit threshold is 75mV±20mV. The current-sense resistor must be sized using the minimum current limit threshold. The external components must be designed to withstand the maximum current limit. The current-sense resistor value is calculated by the equation below:

$$R_{CS} = \frac{55mV}{I_{OUT(max)}}$$

The maximum output current is:

$$I_{OUT(max)} = \frac{95mV}{R_{CS}}$$

The current-sense pins CSH (pin 4) and V_{OUT} (pin 5) are noise sensitive due to the low signal level and high input impedance. The PCB traces should be short and routed close to each other. A small (1nF to 0.1µF) capacitor across the pins will attenuate high frequency switching noise.

When the peak inductor current exceeds the current limit threshold, the current limit comparator, in Figure 2, turns off the high-side MOSFET for the remainder of the cycle. The output voltage drops as additional load current is pulled from the converter. When the output voltage reaches approximately 0.4V, the circuit enters frequency-foldback mode and the oscillator frequency will drop to 75kHz while maintaining the peak inductor current equal to the nominal 75mV across the external current-sense resistor. This limits the maximum output power delivered to the load under a short circuit condition.

Reference, Enable and UVLO Circuits

The output drivers are enabled when the following conditions are satisfied:

- The V_{DD} voltage (pin 7) is greater than its under-voltage threshold (typically 4.25V).
- The voltage on the enable pin is greater than the enable UVLO threshold (typically 2.5V).

The internal bias circuit generates a 0.8V bandgap reference voltage for the voltage error amplifier and a 5V V_{DD} voltage for the gate drive circuit. The MIC2199 uses FB (pin 3) for output voltage sensing.

The enable pin (pin 2) has two threshold levels, allowing the MIC2199 to shut down in a low current mode, or turn off output switching in UVLO mode. An enable pin voltage lower than the shutdown threshold turns off all the internal circuitry and reduces the input current to typically 0.1µA.

If the enable pin voltage is between the shutdown and UVLO thresholds, the internal bias, V_{DD}, and reference voltages are turned on. The output drivers are inhibited from switching and remain in a low state. Raising the enable voltage above the UVLO threshold of 2.5V enables the output drivers.

Either of two UVLO conditions will disable the MIC2199 from switching.

- When the V_{DD} drops below 4.1V
- When the enable pin drops below the 2.5V threshold

MOSFET Gate Drive

The MIC2199 high-side drive circuit is designed to switch an N-Channel MOSFET. Referring to the block diagram in Figure 2, a bootstrap circuit, consisting of D2 and C_{BST}, supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the V_{SW} pin (pin 11) is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the MOSFET turns on, the voltage on the V_{SW} pin increases to approximately V_{IN}. Diode D2 is reversed biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. When the low-side switch is turned back on, C_{BST} is recharged through D2.

The drive voltage is derived from the internal 5V V_{DD} bias supply. The nominal low-side gate drive voltage is 5V and the nominal high-side gate drive voltage is approximately 4.5V due the voltage drop across D2. A fixed 80ns delay between the high- and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Oscillator

The internal oscillator is free running and requires no external components. The nominal oscillator frequency is 500kHz. If the output voltage is below approximately 0.4V, the oscillator operates in a frequency-foldback mode and the switching frequency is reduced to 75kHz.

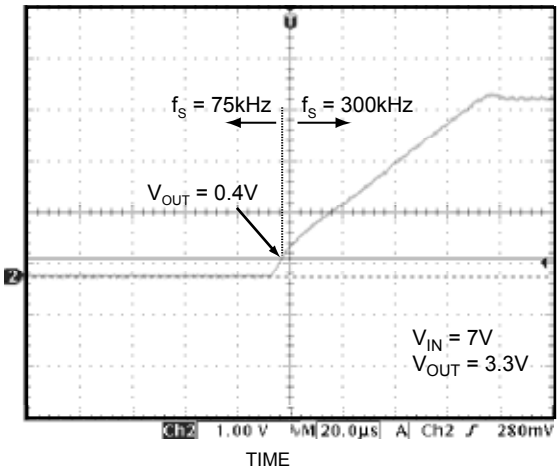


Figure 4. Startup Waveform

Above 0.4V, the switching frequency increases to 500kHz causing the output voltage to rise a greater rate. The rise time of the output is dependent on the output capacitance, output voltage, and load current. The oscilloscope photo in Figure 4 show the output voltage at startup.

Minimum Pulsewidth

The MIC2199 has a specified minimum pulsewidth. This minimum pulsewidth places a lower limit on the minimum duty cycle of the buck converter.

Figure 5 shows the minimum output voltage versus input supply voltage for the MIC2199. For example, for V_{IN} = 15V, V_{OUT} = 1V would be the lowest achievable voltage that conforms to the minimum-on-time.

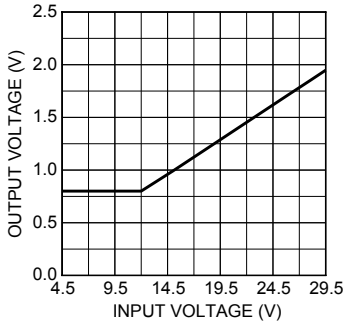


Figure 5. Minimum Output Voltage vs. Input Supply Voltage

Applications Information

Following applications information includes component selection and design guidelines.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.

The inductance value is calculated by the equation below.

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_S \times 0.2 \times I_{OUT(max)}}$$

where:

f_S = switching frequency

0.2 = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum input voltage

The peak-to-peak inductor current (AC ripple current) is:

$$I_{PP} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_S \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor ripple current.

$$I_{PK} = I_{OUT(max)} + 0.5 \times I_{PP}$$

The RMS inductor current is used to calculate the $I^2 \times R$ losses in the inductor.

$$I_{INDUCTOR(rms)} = I_{OUT(max)} \times \sqrt{1 + \frac{1}{3}\left(\frac{I_P}{I_{OUT(max)}}\right)^2}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2199 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor.

The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTORCu} = I_{INDUCTOR(rms)^2} \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING(hot)} = R_{WINDING(20°C)} \times \left(1 + 0.0042 \times (T_{HOT} - T_{20°C})\right)$$

where:

T_{HOT} = temperature of the wire under operating load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ is room temperature winding resistance

(usually specified by the manufacturer)

Current-Sense Resistor Selection

Low inductance power resistors, such as metal film resistors should be used. Most resistor manufacturers make low inductance resistors with low temperature coefficients, designed specifically for current-sense applications. Both resistance and power dissipation must be calculated before the resistor is selected. The value of R_{SENSE} is chosen based on the maximum output current and the maximum threshold level. The power dissipated is based on the maximum peak output current at the minimum overcurrent threshold limit.

$$R_{SENSE} = \frac{55mV}{I_{OUT(max)}}$$

The maximum overcurrent threshold is:

$$I_{OVERCURRENT(max)} = \frac{95mV}{R_{CS}}$$

The maximum power dissipated in the sense resistor is:

$$P_{D(R_{SENSE})} = I_{OVERCURRENT(max)}^2 \times R_{CS}$$

MOSFET Selection

External N-Channel logic-level power MOSFETs must be used for the high- and low-side switches. The MOSFET gate-to-source drive voltage of the MIC2199 is regulated by an internal 5V V_{DD} regulator. Logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

It is important to note the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2199 gate drive circuit. At 500kHz switching frequency, the gate charge can be a significant source of power dissipation in the MIC2199. At low output load this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side](avg)} = Q_G \times f_S$$

where:

$I_{G[high\text{-}side](avg)}$ = average high-side MOSFET gate current

Q_G = total gate charge for the high-side MOSFET taken from manufacturer's data sheet with V_{GS} = 5V.

f_s = 300kHz

The low-side MOSFET is turned on and off at $V_{DS} = 0$ because the freewheeling diode is conducting during this time. The switching losses for the low-side MOSFET is usually negligible. Also, the gate drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low\text{-}side](avg)} = C_{ISS} \times V_{GS} \times f_S$$

Since the current from the gate drive comes from the input voltage, the power dissipated in the MIC2199 due to gate drive is:

$$P_{GATEDRIVE} = V_{IN}\left(I_{G[high\text{-}side](avg)} + I_{G[low\text{-}side](avg)}\right)$$

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge ($R_{DS(on)} \times Q_G$). Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2199. Power dissipation in the MIC2199 package limits the maximum gate drive current.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage rating of the MOSFETs are essentially equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

where:

$$P_{CONDUCTION} = I_{SW(rms)^2} \times R_{SW}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)}$$

R_{SW} = on-resistance of the MOSFET switch.

Making the assumption the turn-on and turnoff transition times are equal, the transition time can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{GS} + C_{OSS} \times V_{IN}}{I_G}$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0.

I_G = gate drive current (1A for the MIC2199)

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{IN} + V_D) \times I_{PK} \times t_T \times f_S$$

where:

t_T = switching transition time (typically 20ns to 50ns)

V_D = freewheeling diode drop, typically 0.5V.

f_S it the switching frequency, nominally 300kHz

The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

RMS Current and MOSFET Power Dissipation Calculation

Under normal operation, the high-side MOSFETs RMS current is greatest when V_{IN} is low (maximum duty cycle). The low-side MOSFETs RMS current is greatest when V_{IN} is high (minimum duty cycle). However, the maximum stress the MOSFETs see occurs during short circuit conditions, where the output current is equal to $I_{OVERCURRENT(max)}$. (See the *"Sense Resistor"* section). The calculations below are for normal operation. To calculate the stress under short circuit conditions, substitute $I_{OVERCURRENT(max)}$ for $I_{OUT(max)}$. Use the formula below to calculate D under short circuit conditions.

$$D_{SHORTCIRCUIT} = 0.063 - 1.8 \times 10^{-3} \times V_{IN}$$

The RMS value of the high-side switch current is:

$$I_{SW(high-side)(rms)} = \sqrt{D \times \left(I_{OUT(max)}^2 + \frac{I_{PP}^2}{12}\right)}$$

$$I_{SW(low-side)(rms)} = \sqrt{(1-D)\left(I_{OUT(max)}^2 + \frac{I_{PP}^2}{12}\right)}$$

where:

D = duty cycle of the converter

$$D = \frac{V_{OUT}}{\eta \times V_{IN}}$$

η = efficiency of the converter.

Converter efficiency depends on component parameters, which have not yet been selected. For design purposes, an efficiency of 90% can be used for V_{IN} less than 10V and 85% can be used for V_{IN} greater than 10V. The efficiency can be more accurately calculated once the design is complete. If the assumed efficiency is grossly inaccurate, a second iteration through the design procedure can be made.

For the high-side switch, the maximum DC power dissipation is:

$$P_{SWITCH1(dc)} = R_{DS(on)1} \times I_{SW1(rms)^2}$$

For the low-side switch (N-Channel MOSFET), the DC power dissipation is:

$$P_{SWITCH2(dc)} = R_{DS(on)2} \times I_{SW\,2(rms)^2}$$

Since the AC switching losses for the low side MOSFET is near zero, the total power dissipation is:

$$P_{low\text{-}side\ MOSFET(max)} = P_{SWITCH2(dc)}$$

The total power dissipation for the high side MOSFET is:

$$P_{high-sideMOSFET(max)} = P_{SWITCH\,1(dc)} + P_{AC}$$

External Schottky Diode

An external freewheeling diode is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically 80ns The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)} = I_{OUT} \times 2 \times 80ns \times f_S$$

The reverse voltage requirement of the diode is:

$$V_{DIODE(rrm)} = V_{IN}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F$$

where:

V_F = forward voltage at the peak diode current

The external Schottky diode, D2, is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a 1/2% to 1% improvement in efficiency.

Output Capacitor Selection

The output capacitor values are usually determined by the capacitors ESR (equivalent series resistance). Voltage rating and RMS current capability are two other important factors in selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytics, and OS-CON.

The output capacitor's ESR is usually the main cause of output ripple. The maximum value of ESR is calculated by:

$$R_{ESR} \le \frac{\Delta V_{OUT}}{I_{PP}}$$

where:

V_{OUT} = peak-to-peak output voltage ripple

I_{PP} = peak-to-peak inductor ripple current

The total output ripple is a combination of the ESR and the output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP} \times (1-D)}{C_{OUT} \times f_S}\right)^2 + \left(I_{PP} \times R_{ESR}\right)^2}$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_S = switching frequency

The voltage rating of capacitor should be twice the output voltage for a tantalum and 20% greater for an aluminum electrolytic or OS-CON.

The output capacitor RMS current is calculated below:

$$I_{C_{OUT(rms)}} = \frac{I_{PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT(rms)^2}} \times R_{ESR(C_{OUT})}$$

Input Capacitor Selection

The input capacitor should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. Tantalum input capacitor voltage rating should be at least 2 times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating.

The input voltage ripple will primarily depend on the input capacitors ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{INDUCTOR(peak)} \times R_{ESR(C_{IN})}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor ripple current is low:

$$I_{C_{IN}(rms)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)}$$

The power dissipated in the input capacitor is:

$$P_{DISS(C_{IN})} = I_{C_{IN}(rms)^2} \times R_{ESR(C_{IN})}$$

Voltage Setting Components

The MIC2199 requires two resistors to set the output voltage as shown in Figure 6.

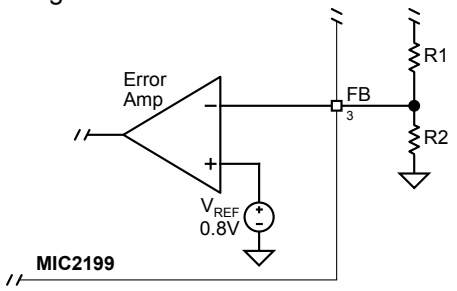


Figure 6. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_O = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where: V_{REF} for the MIC2199 is typically 0.8V.

A typical value of R1 can be between 3k and 10k. If R1 is too large it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value it will decrease the efficiency of the power supply, especially at low output loads.

Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \times R1}{V_O - V_{REF}}$$

Voltage Divider Power Dissipation

The reference voltage and R2 set the current through the voltage divider.

$$I_{DIVIDER} = \frac{V_{REF}}{R2}$$

The power dissipated by the divider resistors is:

$$P_{DIVIDER} = (R1 + R2) \times I_{DIVIDER}^{2}$$

Efficiency Calculation and Considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the buck converter. Under light output load, the significant contributors are:

- Supply current to the MIC2199
- MOSFET gate-charge power (included in the IC supply current)
- Core losses in the output inductor

To maximize efficiency at light loads:

- Use a low gate-charge MOSFET or use the smallest MOSFET, which is still adequate for maximum output current.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

Under heavy output loads the significant contributors to power loss are (in approximate order of magnitude):

- Resistive on-time losses in the MOSFETs
- Switching transition losses in the MOSFETs
- Inductor resistive losses
- Current-sense resistor losses
- Input capacitor resistive losses (due to the capacitors ESR)

To minimize power loss under heavy loads:

- Use logic-level, low on-resistance MOSFETs. Multiplying the gate charge by the on-resistance gives a figure of merit, providing a good balance between low and high load efficiency.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during turn-on and turnoff of the MOSFETs. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate-charge MOSFETs will transition faster than those with higher gate-charge requirements.
- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will require more output capacitors to filter the output ripple, which will force a smaller bandwidth, slower transient response and possible instability under certain conditions.
- Lowering the current-sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and will require larger MOSFETs and inductor components.
- Use low-ESR input capacitors to minimize the power dissipated in the capacitors ESR.

Decoupling Capacitor Selection

The 4.7µF decoupling capacitor is used to minimize noise on the V_{DD} pin. The placement of this capacitor is critical to the proper operation of the IC. It must be placed right next to the pins and routed with a wide trace. The capacitor should be a good quality tantalum. An additional 1µF ceramic capacitor may be necessary when driving large MOSFETs with high gate capacitance. Incorrect placement of the V_{DD} decoupling capacitor will cause jitter or oscillations in the switching waveform and large variations in the overcurrent limit.

A 0.1µF ceramic capacitor is required to decouple the V_{IN}. The capacitor should be placed near the IC and connected directly to between pin 6 (V_{IN}) and pin 9 (GND).

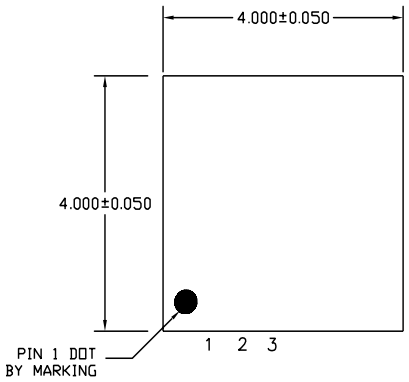
PCB Layout and Checklist

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

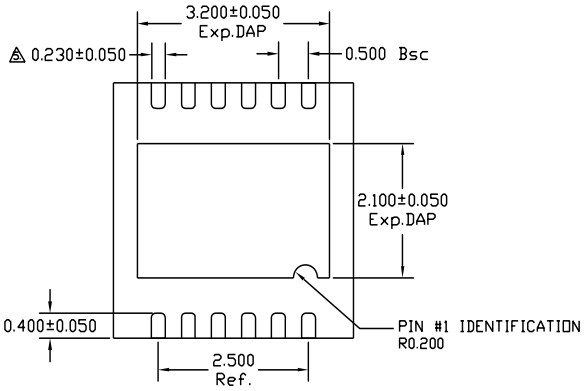
The following guidelines should be followed to insure proper operation of the circuit.

- Signal and power grounds should be kept separate and connected at only one location. Large currents or high di/dt signals that occur when the MOSFETs turn on and off must be kept away from the small signal connections.
- The connection between the current-sense resistor and the MIC2199 current-sense inputs (pin 4 and 5) should have separate traces, through a 10Ω resistor on each pin. The traces should be routed as closely as possible to each other and their length should be minimized. Avoid running the traces under the inductor and other switching components. The 10Ω resistor should be placed close as possible to pins 4 and 5 on the MIC2199 and a 1nF to 0.1µF capacitor placed between pins 4 and 5 will help attenuate switching noise on the current sense traces. This capacitor should be placed close to pins 4 and 5.
- When the high-side MOSFET is switched on, the critical flow of current is from the input capacitor through the MOSFET, inductor, sense resistor, output capacitor, and back to the input capacitor. These paths must be made with short, wide pieces of trace. It is good practice to locate the ground terminals of the input and output capacitors close to each.
- When the low-side MOSFET is switched on, current flows through the inductor, sense resistor, output capacitor, and MOSFET. The source of the low-side MOSFET should be located close to the output capacitor.
- The freewheeling diode, D1 in Figure 2, conducts current during the dead time, when both MOSFETs are off. The anode of the diode should be located close to the output capacitor ground terminal and the cathode should be located close to the input side of the inductor.
- The 4.7µF capacitor, which connects to the V_{DD} terminal (pin 7) must be located right at the IC. The V_{DD} terminal is very noise sensitive and placement of this capacitor is very critical. Connections must be made with wide trace. The capacitor may be located on the bottom layer of the board and connected to the IC with multiple vias.
- The V_{IN} bypass capacitor should be located close to the IC and connected between pins 6 and 9. Connections should be made with a ground and power plane or with short, wide trace.

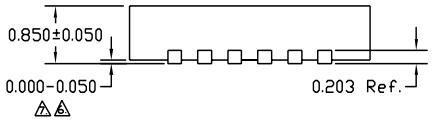
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

12-Pin 4×4 MLF® (ML)

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