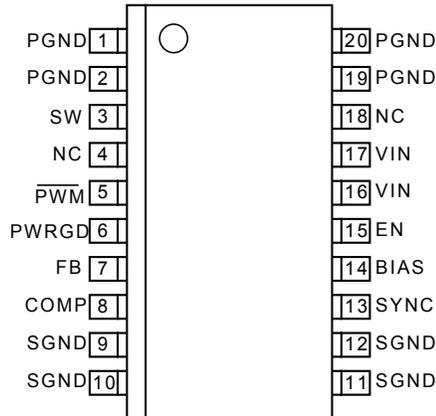


Ordering Information

Part Number		Voltage	Temperature Range	Package
Standard*	Pb-Free			
MIC2179BSM	MIC2179YSM	Adj.	-40°C to +85°C	20-Lead SSOP
MIC2179-3.3BSM	MIC2179-3.3YSM	3.3V	-40°C to +85°C	20-Lead SSOP
MIC2179-5.0BSM	MIC2179-5.0YSM	5.0V	-40°C to +85°C	20-Lead SSOP

* Standard product will be supported as Pb-Free IAW PCCN #040004 effective 1-1-2005 pending residual depletion.

Pin Configuration



20-Lead Wide SSOP

Pin Description

Pin Number	Pin Name	Pin Function
1, 2, 19, 20	PGND	Power Ground: Connect all pins to central ground point.
3	SW	Switch (Output): Internal power MOSFET output switches.
5	PWM	PWM/Skip-Mode Control (Input): Logic-level input. Controls regulator operating mode. Logic low enables PWM mode. Logic high enables skip mode. Do not allow pin to float.
6	PWRGD	Error Flag (Output): Open-drain output. Active low when FB input is 10% below the reference voltage (V_{REF}).
7	FB	Feedback (Input): Connect to output voltage divider resistors.
8	COMP	Compensation: Output of internal error amplifier. Connect capacitor or series RC network to compensate the regulator control loop.
9–12	SGND	Signal Ground: Connect all pins to ground, PGND.
13	SYNC	Frequency Synchronization (Input): Optional. Connect an external clock signal to synchronize the oscillator. Leading edge of signal above 1.7V terminates switching cycle. Connect to SGND if not used.
14	BIAS	Internal 3.3V Bias Supply: Decouple with 0.01 μ F bypass capacitor to SGND. Do not apply any external load.
15	EN	Enable (Input): Logic high enables operation. Logic low shuts down regulator. Do not allow pin to float.
16, 17	VIN	Supply Voltage (Input): Requires bypass capacitor to PGND. Both pins must be connected to V_{IN} .
4, 18	NC	not internally connected.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage [100ms transient] (V_{IN})	18V
Output Switch Voltage (V_{SW})	18V
Output Switch Current (I_{SW})	6.0A
Enable, PWM Control Voltage (V_{EN} , V_{PWM})	18V
Sync Voltage (V_{SYNC})	6V

Operating Ratings⁽²⁾

Supply Voltage (V_{IN})	4.5V to 16.5V
Junction Temperature Range (T_J)	-40°C to +125°C

Electrical Characteristics⁽³⁾

$V_{IN} = 7.0V$; $T_A = 25^\circ C$, **bold** indicates $-40^\circ C \leq T_A \leq 85^\circ C$; unless noted.

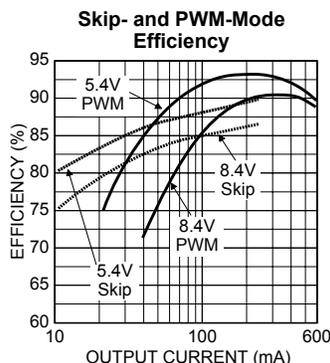
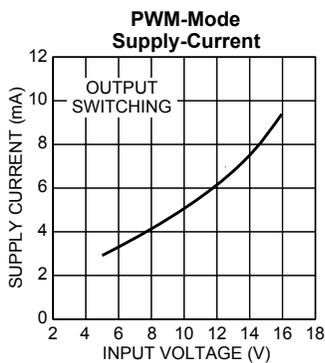
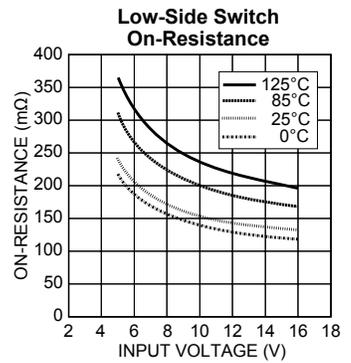
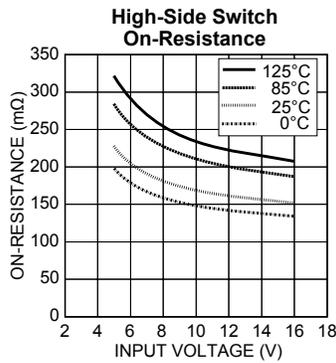
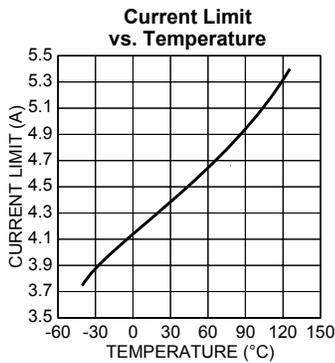
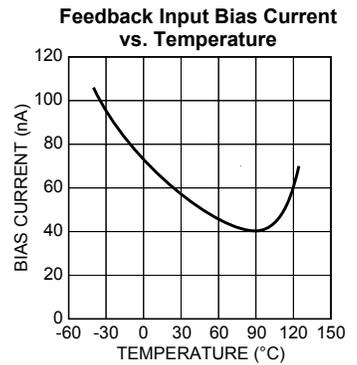
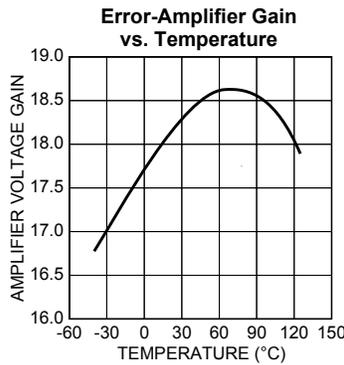
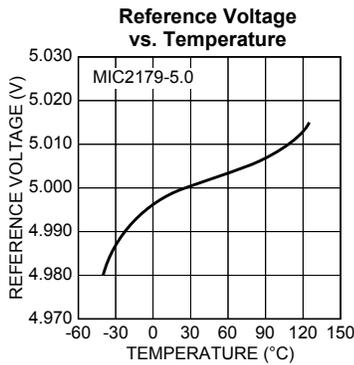
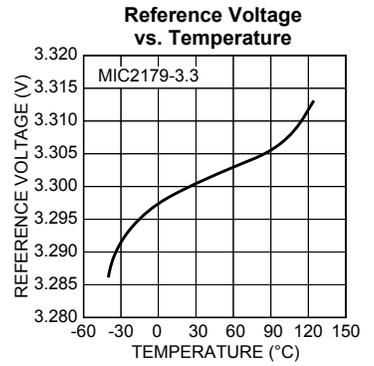
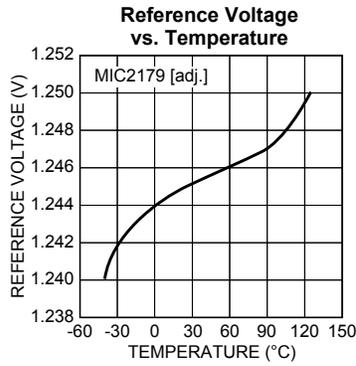
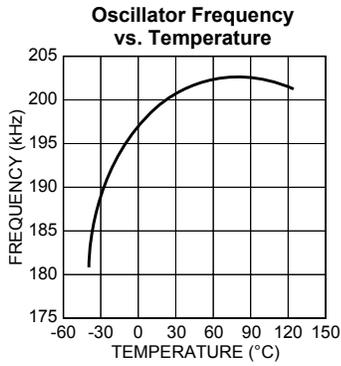
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SS}	Input Supply Current	PWM mode, output not switching, $4.5V \leq V_{IN} \leq 16.5V$		1.0	1.5	mA
		skip mode, output not switching, $4.5V \leq V_{IN} \leq 16.5V$		600	750	μA
		$V_{EN} = 0V$, $4.5V \leq V_{IN} \leq 16.5V$		1	25	μA
V_{BIAS}	Bias Regulator Output Voltage	$V_{IN} = 16.5V$	3.10	3.30	3.4	V
V_{FB}	Feedback Voltage	MIC2179 [adj.]: $V_{OUT} = 3.3V$, $I_{LOAD} = 0$	1.22	1.245	1.27	V
V_{OUT}	Output Voltage	MIC2179 [adj.]: $V_{OUT} = 3.3V$, $5V \leq V_{IN} \leq 16V$, $10mA \leq I_{LOAD} \leq 1A$	3.20	3.3	3.40	V
			3.14		3.46	V
		MIC2179-5.0: $I_{LOAD} = 0$	4.85	5.0	5.15	V
		MIC2179-5.0: $6V \leq V_{IN} \leq 16V$, $10mA \leq I_{LOAD} \leq 1A$	4.85	5.0	5.15	V
			4.75		5.25	V
		MIC2179-3.3: $I_{LOAD} = 0$	3.20	3.3	3.40	V
	MIC2179-3.3: $5V \leq V_{IN} \leq 16V$, $10mA \leq I_{LOAD} \leq 1A$	3.20	3.3	3.40	V	
		3.14		3.46	V	
V_{TH}	Undervoltage Lockout	upper threshold		4.25	4.35	V
V_{TL}		lower threshold	3.90	4.15		V
I_{FB}	Feedback Bias Current	MIC2179 [adj.]		60	150	nA
		MIC2179-5.0, MIC2179-3.3		20	40	μA
A_{VOL}	Error Amplifier Gain	$0.6V \leq V_{COMP} \leq 0.8V$	15	18	20	
	Error Amplifier Output Swing	upper limit	0.9	1.5		V
		lower limit		0.05	0.1	V
	Error Amplifier Output Current	source and sink	15	25	35	μA
f_O	Oscillator Frequency		160	200	240	kHz
D_{MAX}	Maximum Duty Cycle	$V_{FB} = 1.0V$	100			%
$t_{ON\ min}$	Minimum On-Time	$V_{FB} = 1.5V$		300	400	ns
	SYNC Frequency Range		220		300	kHz
	SYNC Threshold		0.8	1.6	2.2	V
	SYNC Minimum Pulse Width		500			ns
	I_{SYNC}	SYNC Leakage	$V_{SYNC} = 0V$ to 5.5V	-1	0.01	1
I_{LIM}	Current Limit	PWM mode, $V_{IN} = 12V$	3.4	4.3	5.5	A
		skip mode		600		mA
R_{ON}	Switch On-Resistance	high-side switch, $V_{IN} = 12V$		160	350	m Ω
		low-side switch, $V_{IN} = 12V$		140	350	m Ω
I_{SW}	Output Switch Leakage	$V_{SW} = 16.5V$		1	10	μA

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Enable Threshold		0.8	1.6	2.2	V
I_{EN}	Enable Leakage	$V_{EN} = 0V \text{ to } 5.5V$	-1	0.01	1	μA
	PWM Threshold		0.6	1.1	1.4	V
I_{PWM}	PWM Leakage	$V_{PWM} = 0V \text{ to } 5.5V$	-1	0.01	1	μA
	PWRGD Threshold	MIC2179 [adj.]: measured at FB pin	1.09	1.13	1.17	V
		MIC2179-5.0: measured at FB pin	4.33	4.54	4.75	V
		MIC2179-3.3: measured at FB pin	2.87	3.00	3.13	V
	PWRGD Output Low	$I_{SINK} = 1.0mA$		0.25	0.4	V
	PWRGD Off Leakage	$V_{PWRGD} = 5.5V$		0.01	1	μA

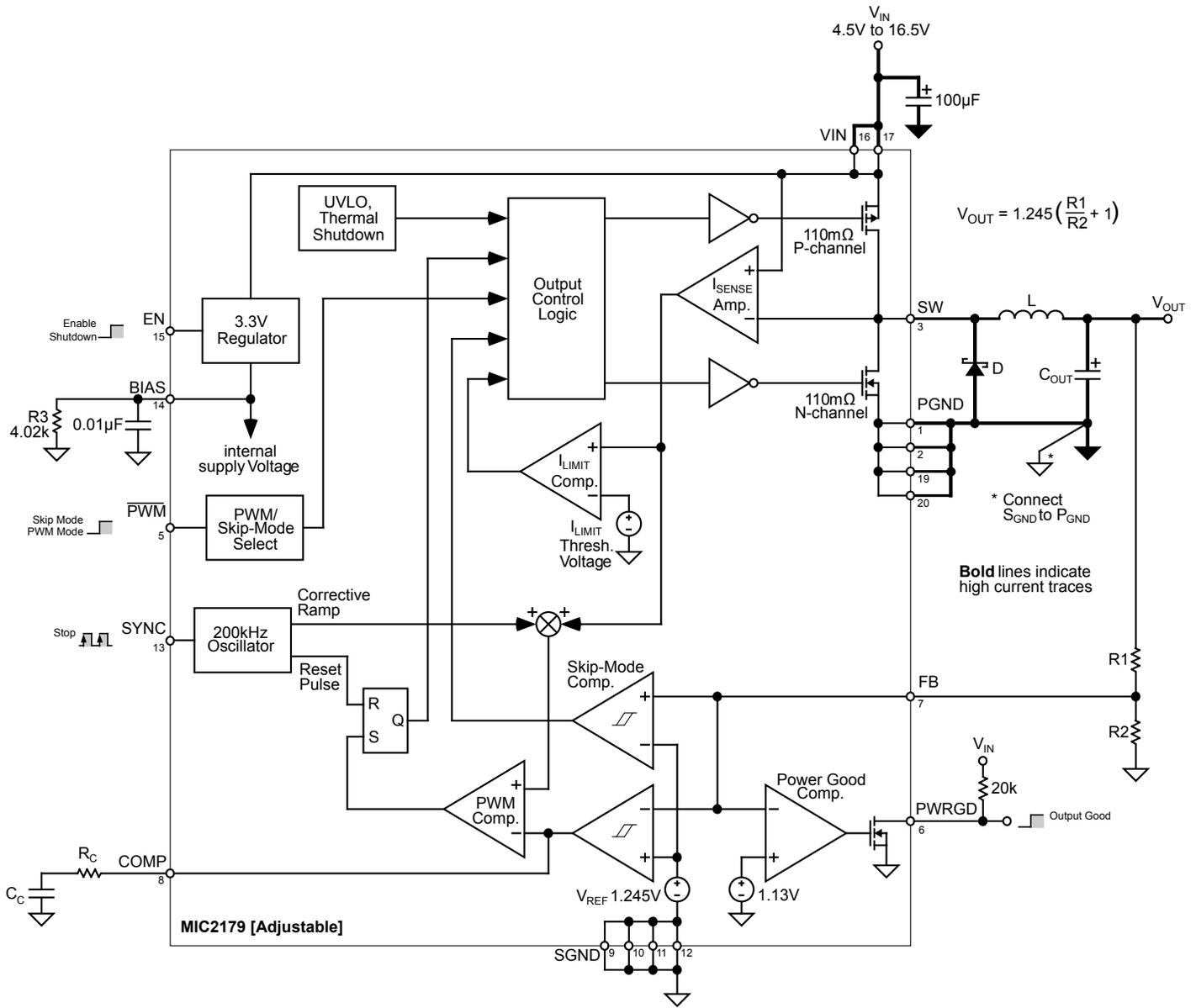
Notes:

1. Exceeding the absolute maximum rating may damage the device.
 2. The device is not guaranteed to function outside its operating rating.
 3. Specification for packaged product only.
- General.** Devices are ESD sensitive. Handling precautions recommended.

Typical Characteristics



Block Diagram



Functional Description

Micrel's MIC2179 is a synchronous buck regulator that operates from an input voltage of 4.5V to 16.5V and provides a regulated output voltage of 1.25V to 16.5V. It has internal power MOSFETs that supply up to 1.5A load current and operates with up to 100% duty cycle to allow low-dropout operation. To optimize efficiency, the MIC2179 operates in PWM and skip mode. Skip mode provides the best efficiency when load current is less than 150mA, while PWM mode is more efficient at higher current. PWM or skip-mode operation is selected externally, allowing an intelligent system (i.e. microprocessor controlled) to select the correct operating mode for efficiency and noise requirements.

During PWM operation, the MIC2179 uses current-mode control which provides superior line regulation and makes the control loop easier to compensate. The PWM switching frequency is set internally to 200kHz and can be synchronized to an external clock frequency up to 300kHz. Other features include a low-current shutdown mode, current limit, under-voltage lockout, and thermal shutdown. See the following sections for more detail.

Switch Output

The switch output (SW) is a half H-bridge consisting of a high-side P-channel and low-side N-channel power MOSFET. These MOSFETs have a typical on-resistance of 150mΩ when the MIC2179 operates from a 12V supply. Antishoot-through circuitry prevents the P-channel and N-channel from turning on at the same time.

Current Limit

The MIC2179 uses pulse-by-pulse current limiting to protect the output. During each switching period, a current limit comparator detects if the P-Channel current exceeds 4.3A. When it does, the P-channel is turned off until the next switching period begins.

Undervoltage Lockout

Undervoltage lockout (UVLO) turns off the output when the input voltage (V_{IN}) is too low to provide sufficient gate drive for the output MOSFETs. It prevents the output from turning on until V_{IN} exceeds 4.3V. Once operating, the output will not shut off until V_{IN} drops below 4.2V.

Thermal Shutdown

Thermal shutdown turns off the output when the MIC2179 junction temperature exceeds the maximum value for safe operation. After thermal shutdown occurs, the output will not turn on until the junction temperature drops approximately 10°C.

Shutdown Mode

The MIC2179 has a low-current shutdown mode that is controlled by the enable input (EN). When a logic 0 is applied to EN, the MIC2179 is in shutdown mode, and its quiescent current drops to less than 5μA.

Internal Bias Regulator

An internal 3.3V regulator provides power to the MIC2179 control circuits. This internal supply is brought out to the BIAS pin for bypassing by an external 0.01μF capacitor. Do not

connect an external load to the BIAS pin. It is not designed to provide an external supply voltage.

Frequency Synchronization

The MIC2179 operates at a preset switching frequency of 200kHz. It can be synchronized to a higher frequency by connecting an external clock to the SYNC pin. The SYNC pin is a logic level input that synchronizes the oscillator to the rising edge of an external clock signal. It has a frequency range of 220kHz to 300kHz, and can operate with a minimum pulse width of 500ns. If synchronization is not required, connect SYNC to ground.

Power Good Flag

The power good flag (PWRGD) is an error flag that alerts a system when the output is not in regulation. When the output voltage is 10% below its nominal value, PWRGD is logic low, signaling that V_{OUT} is too low. PWRGD is an open-drain output that can sink 1mA from a pull-up resistor connected to V_{IN} .

Low-Dropout Operation

Output regulation is maintained in PWM or skip mode even when the difference between V_{IN} and V_{OUT} decreases below 1V. As $V_{IN} - V_{OUT}$ decreases, the duty cycle increases until it reaches 100%. At this point, the P-channel is kept on for several cycles at a time, and the output stays in regulation until $V_{IN} - V_{OUT}$ falls below the dropout voltage (dropout voltage = P-channel on-resistance × load current).

PWM-Mode Operation

Refer to "PWM Mode Functional Diagram" which is a simplified block diagram of the MIC2179 operating in PWM mode and its associated waveforms.

When operating in PWM mode, the output P-channel and N-channel MOSFETs are alternately switched on at a constant frequency and variable duty cycle. A switching period begins when the oscillator generates a reset pulse. This pulse resets the RS latch which turns on the P-channel and turns off the N-channel. During this time, inductor current (I_{L1}) increases and energy is stored in the inductor. The current sense amplifier (I_{SENSE} Amp) measures the P-channel drain-to-source voltage and outputs a voltage proportional to I_{L1} . The output of I_{SENSE} Amp is added to a sawtooth waveform (corrective ramp) generated by the oscillator, creating a composite waveform labeled I_{SENSE} on the timing diagram. When I_{SENSE} is greater than the error amplifier output, the PWM comparator will set the RS latch which turns off the P-channel and turns on the N-channel. Energy is then discharged from the inductor and I_{L1} decreases until the next switching cycle begins. By varying the P-channel on-time (duty cycle), the average inductor current is adjusted to whatever value is required to regulate the output voltage.

The MIC2179 uses current-mode control to adjust the duty cycle and regulate the output voltage. Current-mode control has two signal loops that determine the duty cycle. One is an outer loop that senses the output voltage, and the other is a faster inner loop that senses the inductor current. Signals from these two loops control the duty cycle in the following way: V_{OUT} is fed back to the error amplifier which compares the feedback voltage (V_{FB}) to an internal reference voltage

(V_{REF}). When V_{OUT} is lower than its nominal value, the error amplifier output voltage increases. This voltage then intersects the current sense waveform later in switching period which increases the duty cycle and the average inductor current. If V_{OUT} is higher than nominal, the error amplifier output voltage decreases, reducing the duty cycle.

The PWM control loop is stabilized in two ways. First, the inner signal loop is compensated by adding a corrective ramp to the output of the current sense amplifier. This allows the regulator to remain stable when operating at greater than 50% duty cycle. Second, a series resistor-capacitor load is connected to the error amplifier output (COMP pin). This places a pole-zero pair in the regulator control loop.

One more important item is synchronous rectification. As mentioned earlier, the N-channel output MOSFET is turned on after the P-channel turns off. When the N-channel turns on, its on-resistance is low enough to create a short across the output diode. As a result, inductor current flows through the N-channel and the voltage drop across it is significantly lower than a diode forward voltage. This reduces power dissipation and improves efficiency to greater than 95% under certain operating conditions.

To prevent shoot through current, the output stage employs break-before-make circuitry that provides approximately 50ns of delay from the time one MOSFET turns off and the other turns on. As a result, inductor current briefly flows through the output diode during this transition.

Skip-Mode Operation

Refer to “Skip Mode Functional Diagram” which is a simplified block diagram of the MIC2179 operating in skip mode and its associated waveforms.

Skip-mode operation turns on the output P-channel at a frequency and duty cycle that is a function of V_{IN} , V_{OUT} , and the output inductor value. While in skip mode, the N-channel is kept off to optimize efficiency by reducing gate charge dissipation. V_{OUT} is regulated by skipping switching cycles that turn on the P-channel.

To begin analyzing MIC2179 skip mode operation, assume the skip-mode comparator output is high and the latch output has been reset to a logic 1. This turns on the P-channel and causes I_{L1} to increase linearly until it reaches a current limit of 400mA. When I_{L1} reaches this value, the current limit comparator sets the RS latch output to logic 0, turning off

the P-channel. The output switch voltage (V_{SW}) then swings from V_{IN} to 0.4V below ground, and I_{L1} flows through the Schottky diode. L1 discharges its energy to the output and I_{L1} decreases to zero. When $I_{L1} = 0$, V_{SW} swings from -0.4V to V_{OUT} , and this triggers a one-shot that resets the RS latch. Resetting the RS latch turns on the P-channel, and this begins another switching cycle.

The skip-mode comparator regulates V_{OUT} by controlling when the MIC2179 skips cycles. It compares V_{FB} to V_{REF} and has 10mV of hysteresis to prevent oscillations in the control loop. When V_{FB} is less than $V_{REF} - 5mV$, the comparator output is logic 1, allowing the P-channel to turn on. Conversely, when V_{FB} is greater than $V_{REF} + 5mV$, the P-channel is turned off.

Note that this is a self oscillating topology which explains why the switching frequency and duty cycle are a function of V_{IN} , V_{OUT} , and the value of L1. It has the unique feature (for a pulse-skipping regulator) of supplying the same value of maximum load current for any value of V_{IN} , V_{OUT} , or L1. This allows the MIC2179 to always supply up to 300mA of load current when operating in skip mode.

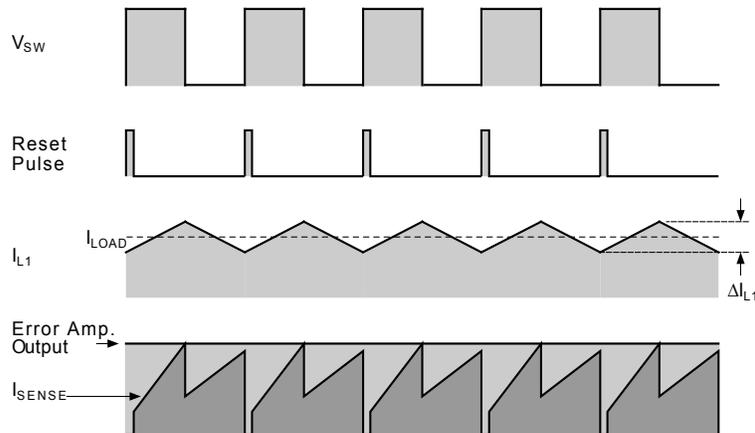
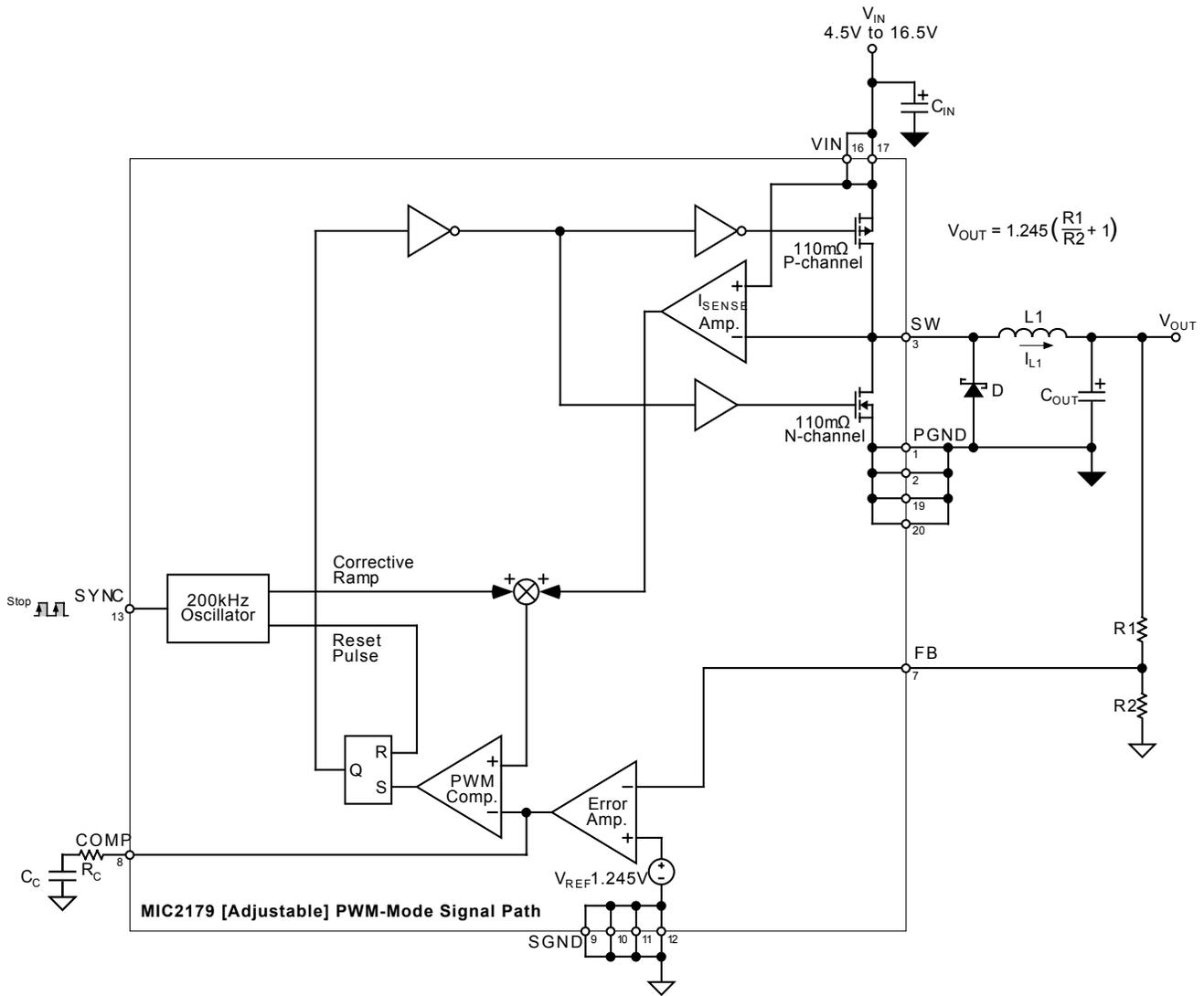
Selecting PWM- or Skip-Mode Operation

PWM or skip mode operation is selected by an external logic signal applied to the \overline{PWM} pin. A logic low places the MIC2179 into PWM mode, and logic high places it into skip mode. Skip mode operation provides the best efficiency when load current is less than 150mA, and PWM operation is more efficient at higher currents.

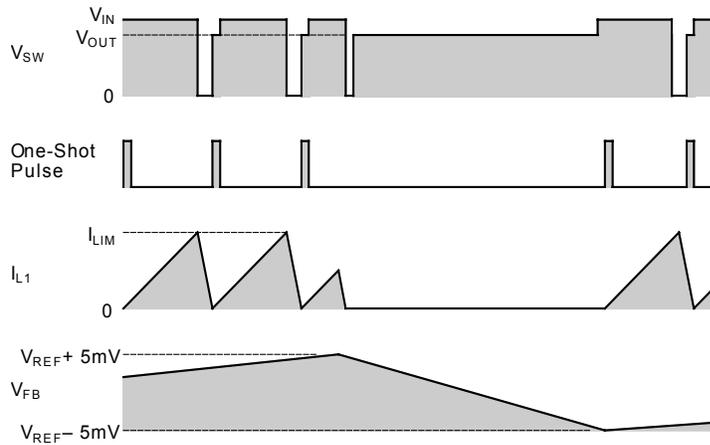
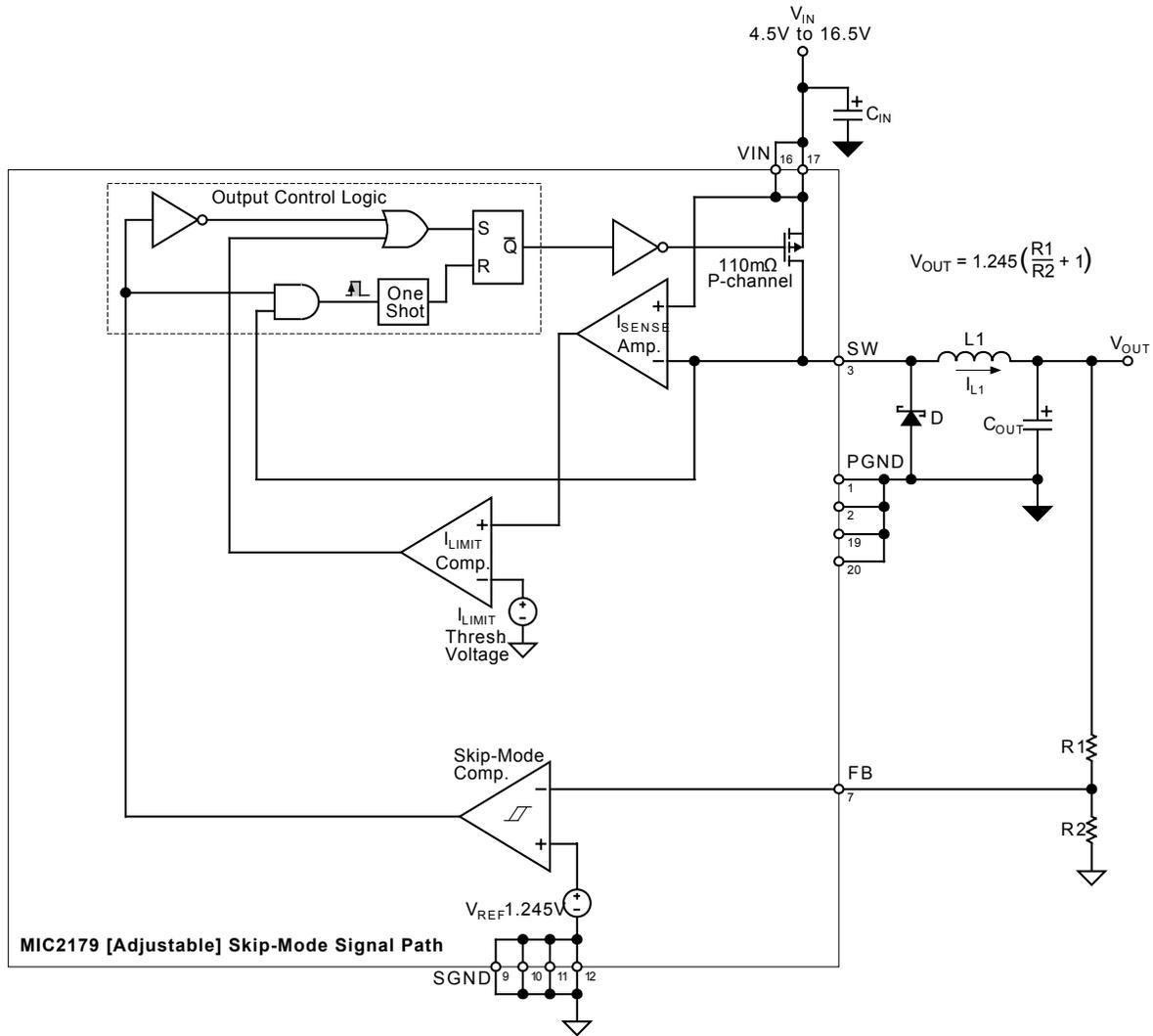
The MIC2179 was designed to be used in intelligent systems that determine when it should operate in PWM or skip mode. This makes the MIC2179 ideal for applications where a regulator must guarantee low noise operation when supplying light load currents, such as cellular telephone, audio, and multimedia circuits.

There are two important items to be aware of when selecting PWM or skip mode. First, the MIC2179 can start-up only in PWM mode, and therefore requires a logic low at \overline{PWM} during start-up. Second, in skip mode, the MIC2179 will supply a maximum load current of approximately 300mA, so the output will drop out of regulation when load current exceeds this limit. To prevent this from occurring, the MIC2179 should change from skip to PWM mode when load current exceeds 200mA.

PWM-Mode Functional Diagram



Skip-Mode Functional Diagram



Application Information

Feedback Resistor Selection (Adjustable Version)

The output voltage is programmed by connecting an external resistive divider to the FB pin as shown in "MIC2179 Block Diagram." The ratio of R1 to R2 determines the output voltage. To optimize efficiency during low output current operation, R2 should not be less than 20kΩ. However, to prevent feedback error due to input bias current at the FB pin, R2 should not be greater than 100kΩ. After selecting R2, calculate R1 with the following formula:

$$R1 = R2 \left(\left(\frac{V_{OUT}}{1.245V} \right) - 1 \right)$$

Input Capacitor Selection

The input capacitor is selected for its RMS current and voltage rating and should be a low ESR (equivalent series resistance) electrolytic or tantalum capacitor. As a rule of thumb, the voltage rating for a tantalum capacitor should be twice the value of V_{IN} , and the voltage rating for an electrolytic should be 40% higher than V_{IN} . The RMS current rating must be equal or greater than the maximum RMS input ripple current. A simple, worst case formula for calculating this RMS current is:

$$I_{RMS(max)} = \frac{I_{LOAD(max)}}{2}$$

Tantalum capacitors are a better choice for applications that require the most compact layout or operation below 0°C. The input capacitor must be located very close to the VIN pin (within 0.2in, 5mm). Also, place a 0.1μF ceramic bypass capacitor as close as possible to VIN.

Inductor Selection

The MIC2179 is a current-mode controller with internal slope compensation. As a result, the inductor must be at least a minimum value to prevent subharmonic oscillations. This minimum value is calculated by the following formula:

$$L_{MIN} = V_{OUT} \times 3.0 \mu H/V$$

In general, a value at least 20% greater than L_{MIN} should be selected because inductor values have a tolerance of ±20%.

Two other parameters to consider in selecting an inductor are winding resistance and peak current rating. The inductor must have a peak current rating equal or greater than the peak inductor current. Otherwise, the inductor may saturate, causing excessive current in the output switch. Also, the inductor's core loss may increase significantly. Both of these effects will degrade efficiency. The formula for peak inductor current is:

$$I_{L(peak)} = I_{LOAD(max)} + \frac{\Delta I_{L(max)}}{2}$$

Where:

$$\Delta I_{L(max)} = V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right) \times \frac{1}{L \cdot f}$$

To maximize efficiency, the inductor's resistance must be less than the output switch on-resistance (preferably, 50mΩ or less).

Output Capacitor Selection

Select an output capacitor that has a low value of ESR. This parameter determines a regulator's output ripple voltage (V_{RIPPLE}) which is generated by $\Delta I_L \times ESR$. Therefore, ESR must be equal or less than a maximum value calculated for a specified V_{RIPPLE} (typically less than 1% of the output voltage) and $\Delta I_{L(max)}$:

$$ESR_{MAX} = \frac{V_{RIPPLE}}{\Delta I_{L(max)}}$$

Typically, capacitors in the range of 100 to 220μF have ESR less than this maximum value. The output capacitor can be a low ESR electrolytic or tantalum capacitor, but tantalum is a better choice for compact layout and operation at temperatures below 0°C. The voltage rating of a tantalum capacitor must be $2 \times V_{OUT}$, and the voltage rating of an electrolytic must be $1.4 \times V_{OUT}$.

Output Diode Selection

In PWM operation, inductor current flows through the output diode approximately 50ns during the dead time when one output MOSFET turns off the other turns on. In skip mode, the inductor current flows through the diode during the entire P-channel off time. The correct diode for both of these conditions is a 1A diode with a reverse voltage rating greater than V_{IN} . It must be a schottky or ultrafast-recovery diode ($t_R < 100ns$) to minimize power dissipation from the diode's reverse-recovery charge.

Compensation

Compensation is provided by connecting a series RC load to the COMP pin. This creates a pole-zero pair in the regulator control loop, allowing the regulator to remain stable with enough low frequency loop-gain for good load and line regulation. At higher frequencies, the pole-zero reduces loop-gain to a level referred to as the mid-band gain. The mid-band gain is low enough so that the loop gain crosses 0db with sufficient phase margin. Typical values for the RC load are 4.7nF to 10nF for the capacitor and 5kΩ to 20kΩ for the resistor.

Printed Circuit Board Layout

A well designed PC board will prevent switching noise and ground bounce from interfering with the operation of the MIC2179. A good design takes into consideration component placement and routing of power traces.

The first thing to consider is the locations of the input capacitor, inductor, output diode, and output capacitor. The input capacitor must be placed very close to the VIN pin, the inductor and output diode very close to the SW pin, and the output capacitor near the inductor. These components pass large high-frequency current pulses, so they must use short, wide power traces. In addition, their ground pins and PGND are connected to a ground plane that is nearest the power supply ground bus.

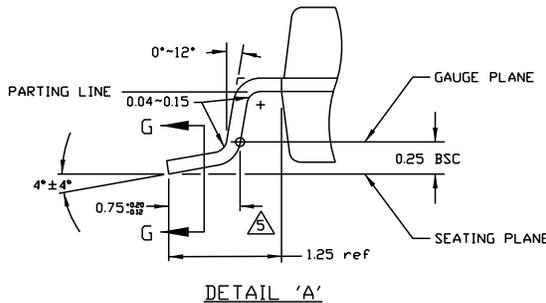
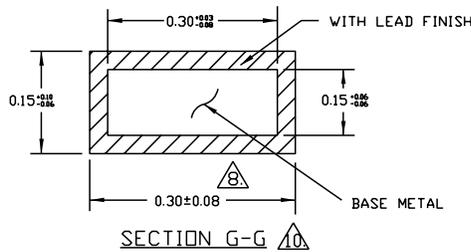
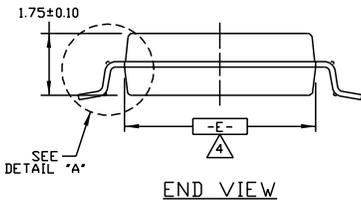
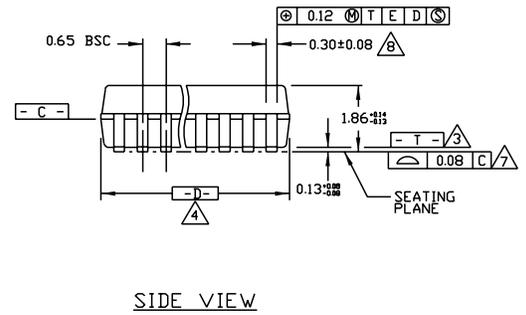
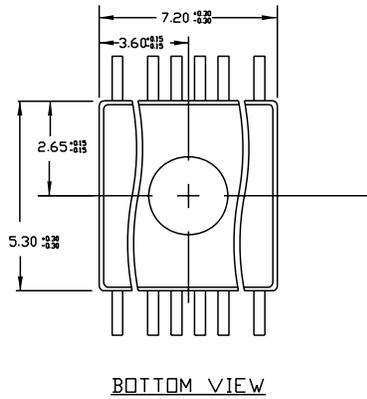
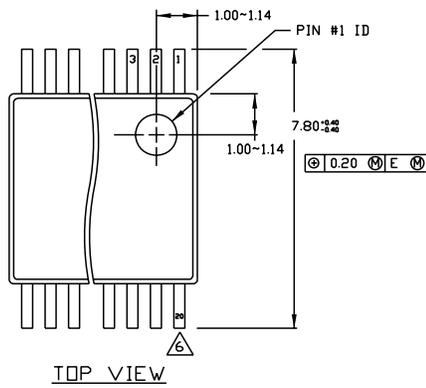
The feedback resistors, RC compensation network, and BIAS pin bypass capacitor should be located close to their respective pins. To prevent ground bounce, their ground traces and SGND should not be in the path of switching

currents returning to the power supply ground bus. SGND and PGND should be tied together by a ground plane that extends under the MIC2179.

Suggested Manufacturers List

Inductors	Capacitors	Diodes	Transistors
<i>Coilcraft</i> 1102 Silver Lake Rd. Cary, IL 60013 tel: (708) 639-2361 fax: (708) 639-1469	<i>AVX Corp.</i> 801 17th Ave. South Myrtle Beach, SC 29577 tel: (803) 448-9411 fax: (803) 448-1943	<i>General Instruments (GI)</i> 10 Melville Park Rd. Melville, NY 11747 tel: (516) 847-3222 fax: (516) 847-3150	<i>Siliconix</i> 2201 Laurelwood Rd. Santa Clara, CA 96056 tel: (800) 554-5565
<i>Coiltronics</i> 6000 Park of Commerce Blvd. Boca Raton, FL 33487 tel: (407) 241-7876 fax: (407) 241-9339	<i>Sanyo Video Components Corp.</i> 2001 Sanyo Ave. San Diego, CA 92173 tel: (619) 661-6835 fax: (619) 661-1055	<i>International Rectifier Corp.</i> 233 Kansas St. El Segundo, CA 90245 tel: (310) 322-3331 fax: (310) 322-3332	
<i>Bi Technologies</i> 4200 Bonita Place Fullerton, CA tel: (714) 447-2345 fax: (714) 447-2500	<i>Sprague Electric</i> Lower Main St. 60005 Sanford, ME 04073 tel: (207) 324-4140	<i>Motorola Inc.</i> MS 56-126 3102 North 56th St. Phoenix, AZ 85018 tel: (602) 244-3576 fax: (602) 244-4015	

Package Information



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (0.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
- △ 'T' IS A REFERENCE DATUM
- △ 'D' & 'E' ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
- △ DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- △ TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- △ FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
- △ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
- △ ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF DIMENSION AT MAXIMUM MATERIAL CONDITION.
- △ DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSIONS: MILLIMETERS.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN.

20-Pin SSOP (SM)

MICREL INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
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