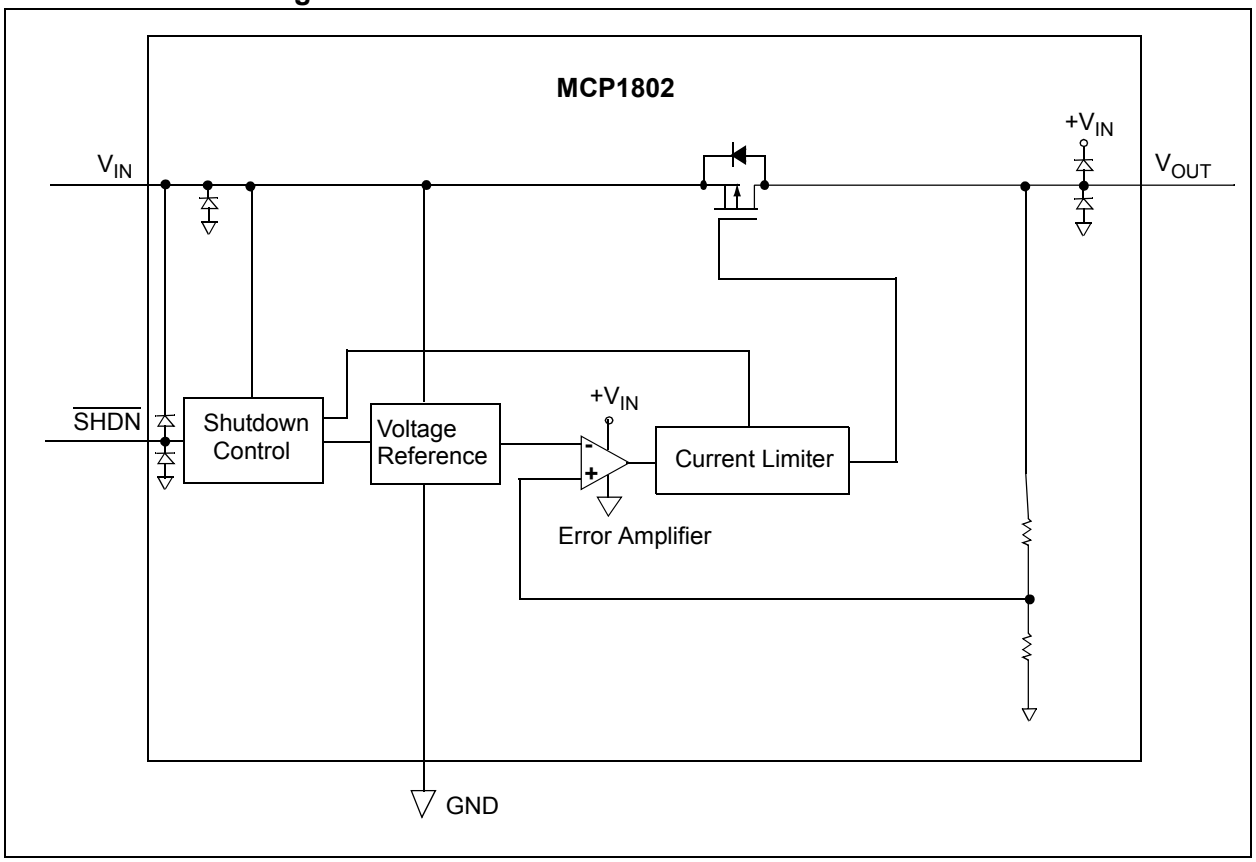
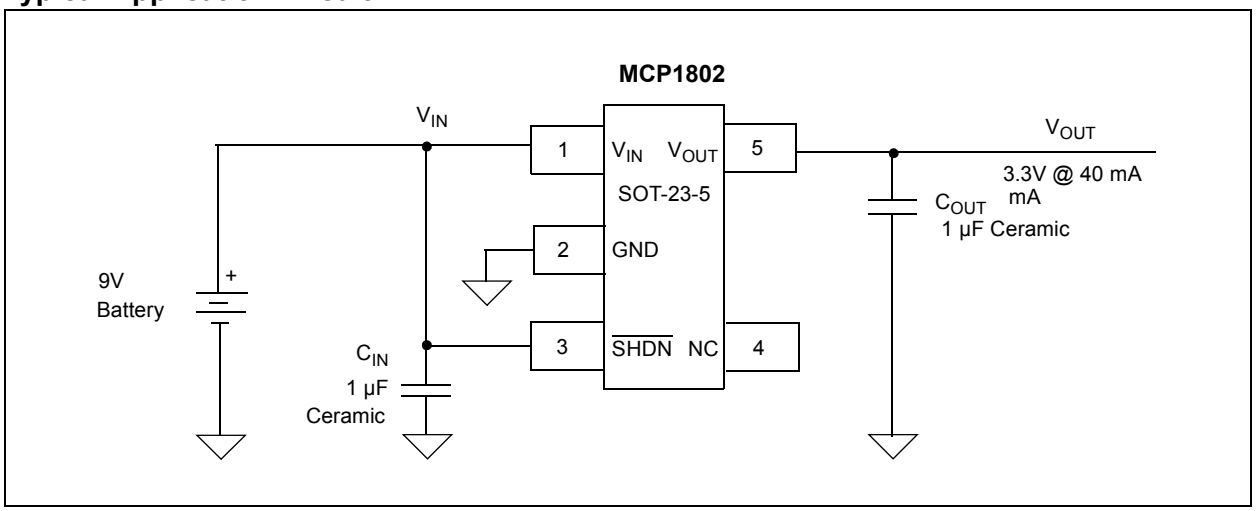
Functional Block Diagram



Typical Application Circuit



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage ..... +12V
Output Current (Continuous) ..... $P_D/(V_{IN}-V_{OUT})$mA
Output Current (Peak) ..... 500 mA
Output Voltage ..... (V_{SS}-0.3V) to (V_{IN}+0.3V)
$\overline{SHDN}$ Voltage ..... (V_{SS}-0.3V) to (V_{IN}+0.3V)
Continuous Power Dissipation:
5-Pin SOT-23-5 ..... 250 mW

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1.0V$, **Note 1**, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), $V_{\overline{SHDN}} = V_{IN}$, T_A = +25°C

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input / Output Characteristics						
Input Operating Voltage	V_{IN}	2.0	—	10.0	V	**Note 1**
Input Quiescent Current	I_q	—	25	50	µA	I_L = 0 mA
Shutdown Current	I_{SHDN}	—	0.01	0.10	µA	$\overline{SHDN}$ = 0V
Maximum Output Current	I_{OUT_mA}	300 300 260 260	— — — —	— — — —	mA	$V_R \geq 2V$, $V_{IN} = V_R + 1.0V$ $1.5V \leq V_R < 2.0V$, V_{IN}=3.0V $1.0V \leq V_R < 1.5V$, $V_{IN} = V_R + 1.5V$ $0.9V \leq V_R < 1.0V$, V_{IN}=2.5V
Current Limiter	I_{LIMIT}	—	380	—	mA	if $V_R \leq 1.75V$, then $V_{IN} = V_R + 2.0V$
Output Short Circuit Current	I_{OUT_SC}	—	50	—	mA	if $V_R \leq 1.75V$, then $V_{IN} = V_R + 2.0V$
Output Voltage Regulation	V_{OUT}	V_R-2.0%	V_R	V_R+2.0%	V	$V_R \geq 1.45V$, I_{OUT} = 30 mA, **Note 2**
		V_R-30 mV	V_R	V_R+30 mV		$V_R < 1.45V$, I_{OUT} = 30 mA
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	100	—	ppm/°C	I_{OUT} = 30 mA, -40°C ≤ T_A ≤ +85°C, **Note 3**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} X \Delta V_{IN})$	-0.2	±0.01	+0.2	%/V	$(V_R + 1V) \leq V_{IN} \leq 10V$, **Note 1** $V_R > 1.75V$, I_{OUT} = 30 mA $V_R \leq 1.75V$, I_{OUT} = 10 mA
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	— —	15 —	50 100	mV	I_L = 1.0 mA to 100 mA, **Note 4** I_L = 1.0 mA to 300 mA,
Dropout Voltage, **Note 5**	$V_{DROPOUT}$	—	60	90	mV	I_L = 30 mA, $3.1V \leq V_R \leq 6.0V$
		—	200	250		I_L = 100 mA, $3.1V \leq V_R \leq 6.0V$
		—	80	120		I_L = 30 mA, $2.0V \leq V_R < 3.1V$
		—	240	350		I_L = 100 mA, $2.0V \leq V_R < 3.1V$
		—	2.07 - V_R	2.10 - V_R	V	I_L = 30 mA, $V_R < 2.0V$
		—	2.23 - V_R	2.33 - V_R		I_L = 100 mA, $V_R < 2.0V$
Power Supply Ripple Rejection Ratio	PSRR	—	70	—	dB	f = 10 kHz, I_L = 50 mA, V_{INAC} = 1V pk-pk, C_{IN} = 0 µF, if $V_R < 1.5V$, then V_{IN} = 2.5V
Output Noise	e_N	—	0.46	—	µV/√Hz	I_{OUT} = 100 mA, f = 1 kHz, C_{OUT} = 1 µF (X7R Ceramic), V_{OUT} = 2.5V

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.0V$ and $V_{IN} \geq (V_R + 1.0V)$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.8V, 2.5V, 3.0V, 3.3V, or 5.0V. The input voltage $V_{IN} = V_R + 1.0V$ or Vi_{IN} = 2.0V (whichever is greater); I_{OUT} = 100 µA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of $V_R + 1.0V$ or 2.0V, whichever is greater.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1.0V$, **Note 1**, $C_{OUT} = 1\ \mu F$ (X7R), $C_{IN} = 1\ \mu F$ (X7R), $V_{\overline{SHDN}} = V_{IN}$, $T_A = +25°C$

Parameters	Sym	Min	Typ	Max	Units	Conditions
Shutdown Input						
Logic High Input	$V_{SHDN-HIGH}$	1.6	—	—	V	—
Logic Low Input	$V_{SHDN-LOW}$	—	—	0.25	V	—

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.0V$ and $V_{IN} \geq (V_R + 1.0V)$.

2: V_R is the nominal regulator output voltage. For example: $V_R = 1.8V$, 2.5V, 3.0V, 3.3V, or 5.0V. The input voltage $V_{IN} = V_R + 1.0V$ or $Vi_{IN} = 2.0V$ (whichever is greater); $I_{OUT} = 100\ \mu A$.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of $V_R + 1.0V$ or 2.0V, whichever is greater.

TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	Tstg	-55	—	+125	°C	
Thermal Package Resistance						
Thermal Resistance, SOT-23-5	θ_{JA} θ_{JC}	— —	256 81	— —	°C/W	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1.0V, SOT-23-5.

Note: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

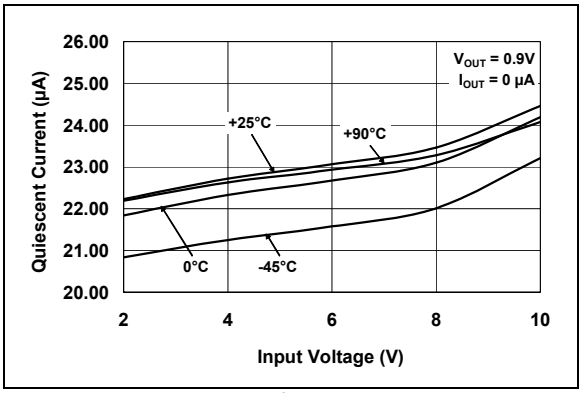

FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

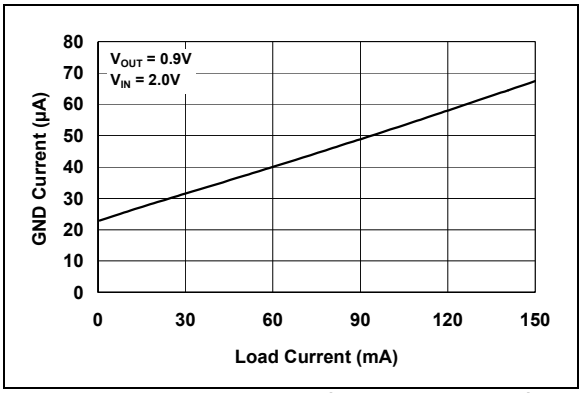

FIGURE 2-4: *Ground Current vs Load Current.*

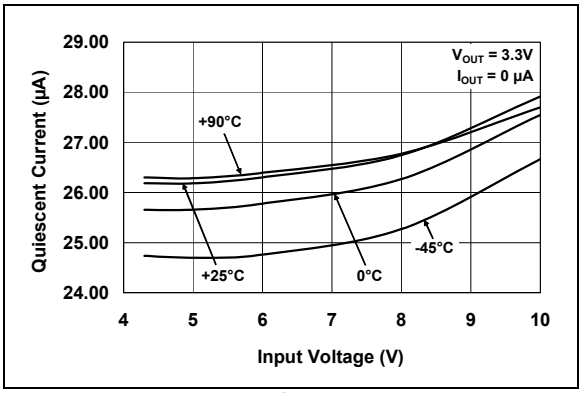

FIGURE 2-2: *Quiescent Current vs. Input Voltage.*

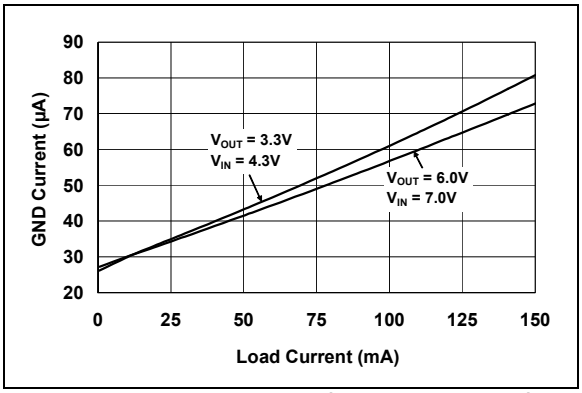

FIGURE 2-5: *Ground Current vs Load Current.*

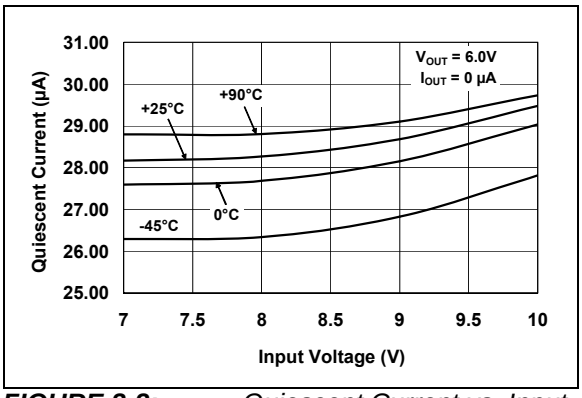

FIGURE 2-3: *Quiescent Current vs. Input Voltage.*

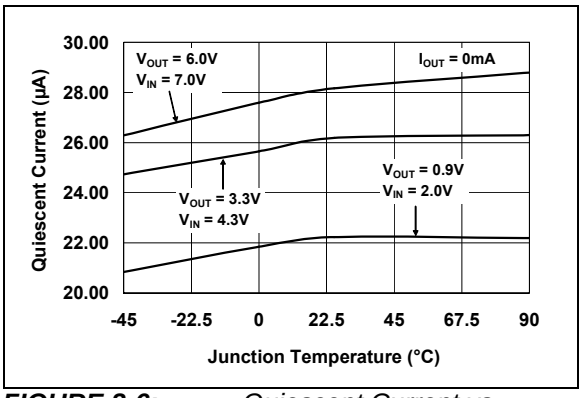

FIGURE 2-6: *Quiescent Current vs. Junction Temperature.*

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Note: Unless otherwise indicated: V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1.0V, SOT-23-5.

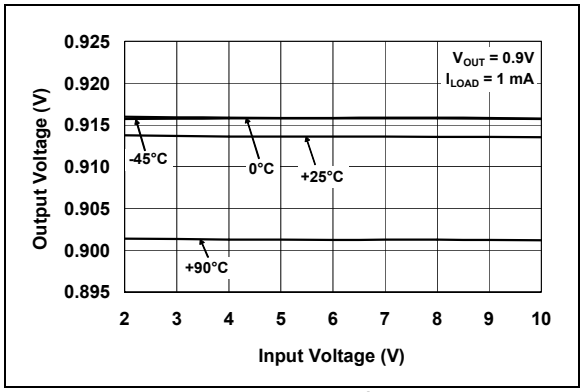

FIGURE 2-7: *Output Voltage vs. Input Voltage.*

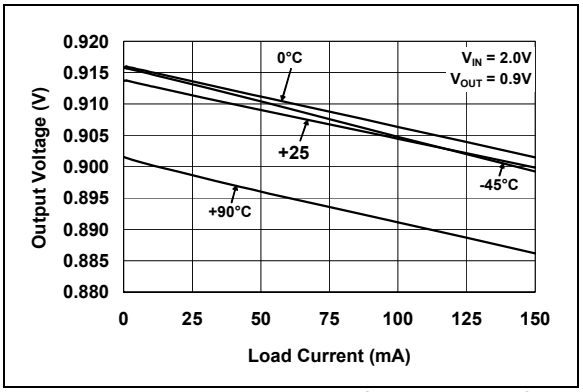

FIGURE 2-10: *Output Voltage vs. Load Current.*

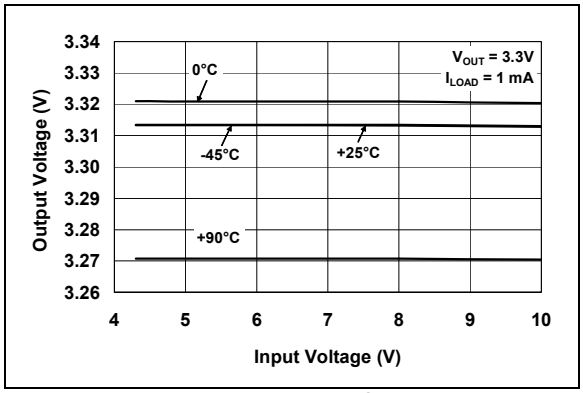

FIGURE 2-8: *Output Voltage vs. Input Voltage.*

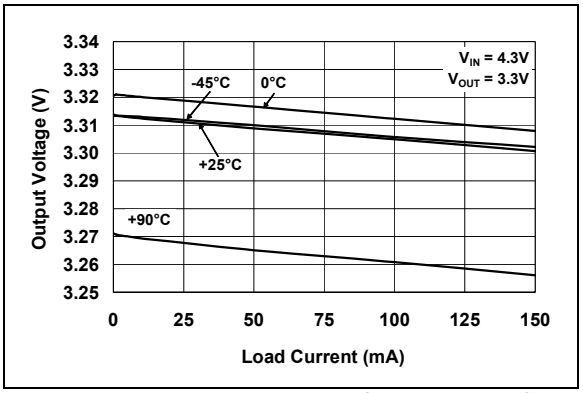

FIGURE 2-11: *Output Voltage vs. Load Current.*

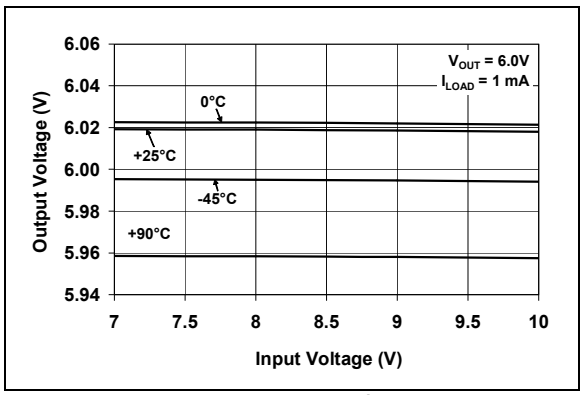

FIGURE 2-9: *Output Voltage vs. Input Voltage.*

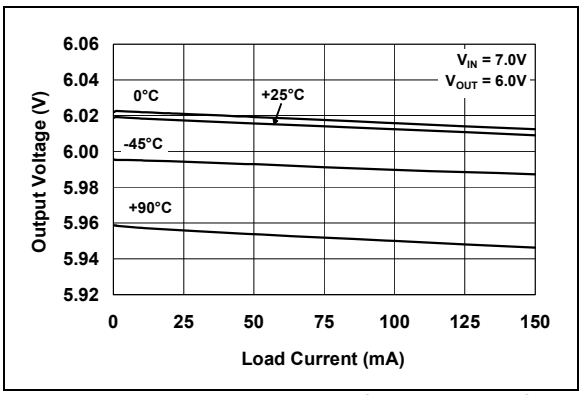

FIGURE 2-12: *Output Voltage vs. Load Current.*

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Note: Unless otherwise indicated: V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1.0V, SOT-23-5.

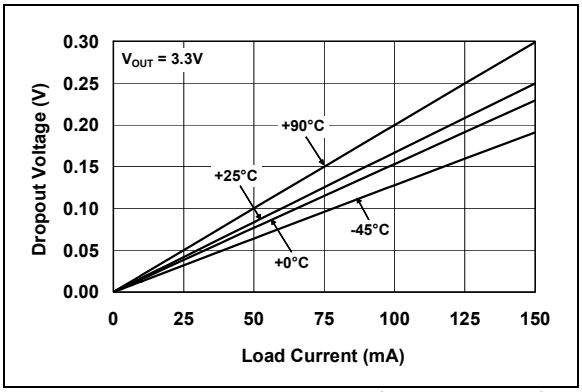

FIGURE 2-13: *Dropout Voltage vs. Load Current.*

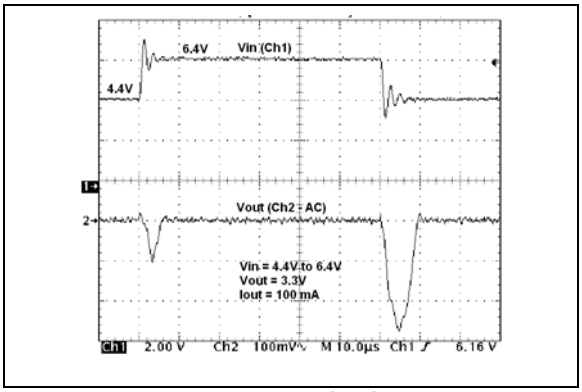

FIGURE 2-16: *Dynamic Line Response.*

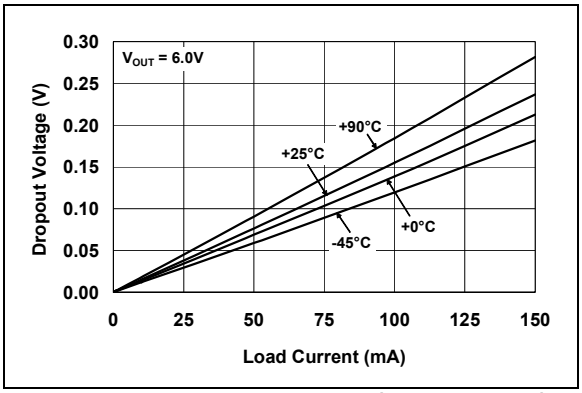

FIGURE 2-14: *Dropout Voltage vs. Load Current.*

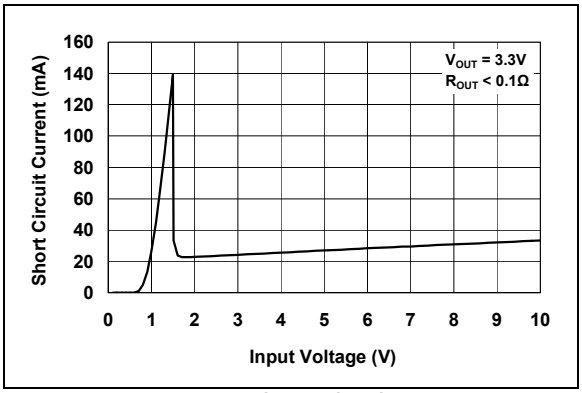

FIGURE 2-17: *Short Circuit Current vs. Input Voltage.*

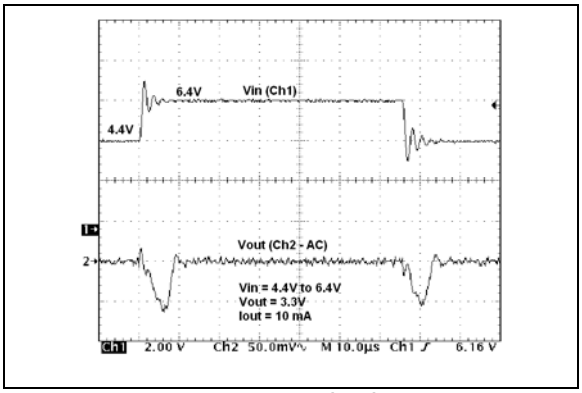

FIGURE 2-15: *Dynamic Line Response.*

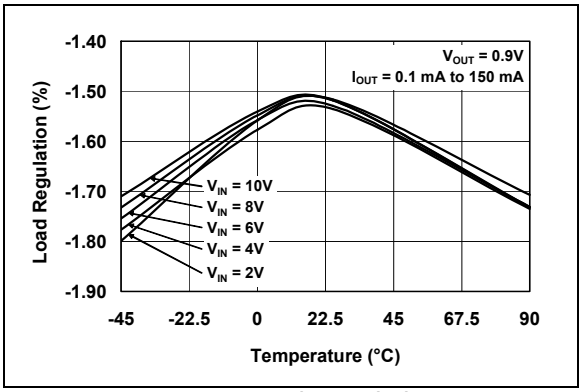

FIGURE 2-18: *Load Regulation vs. Temperature.*

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Note: Unless otherwise indicated: V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_R + 1.0V$, SOT-23-5.

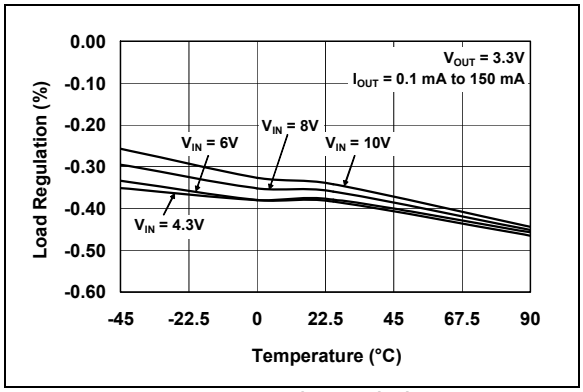

FIGURE 2-19: *Load Regulation vs. Temperature.*

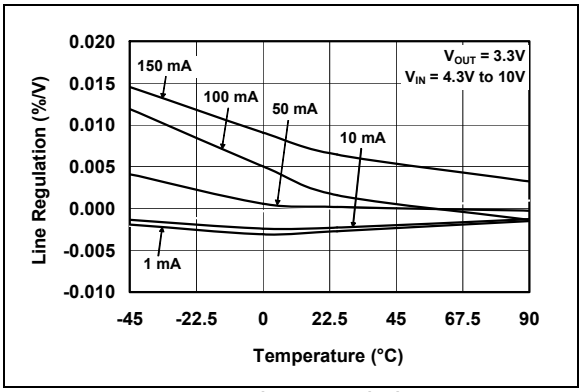

FIGURE 2-22: *Line Regulation vs. Temperature.*

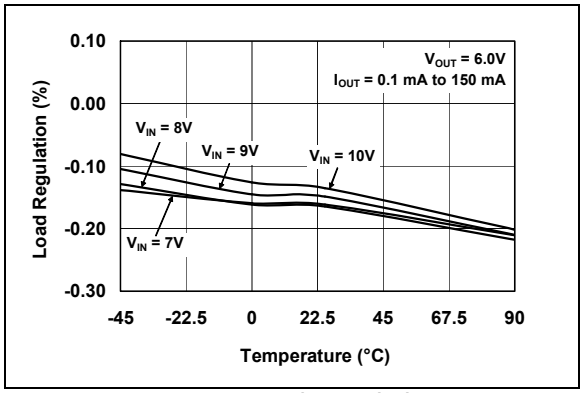

FIGURE 2-20: *Load Regulation vs. Temperature.*

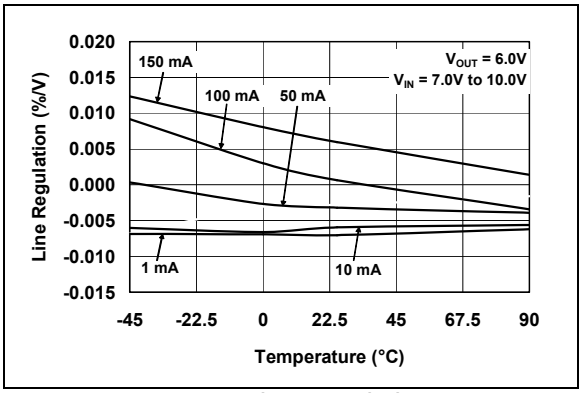

FIGURE 2-23: *Line Regulation vs. Temperature.*

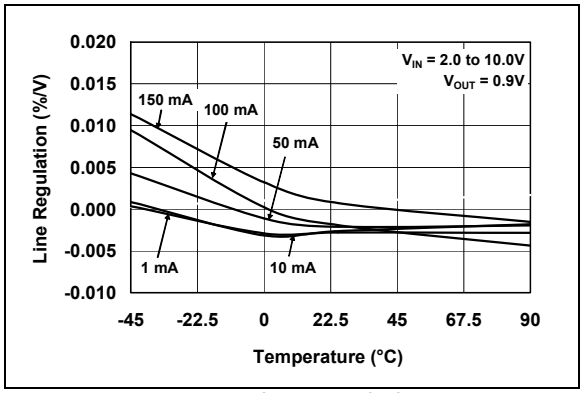

FIGURE 2-21: *Line Regulation vs. Temperature.*

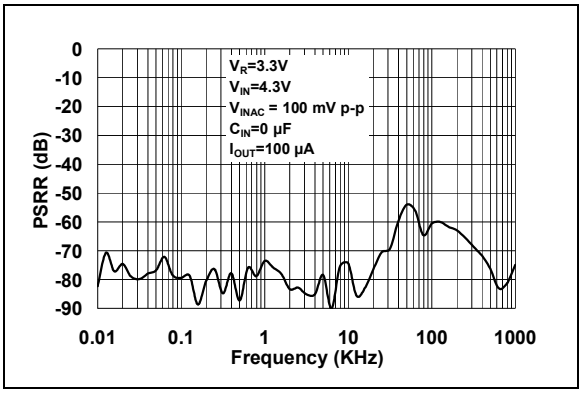

FIGURE 2-24: *PSRR vs. Frequency.*

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Note: Unless otherwise indicated: V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, V_{IN} = V_R + 1.0V, SOT-23-5.

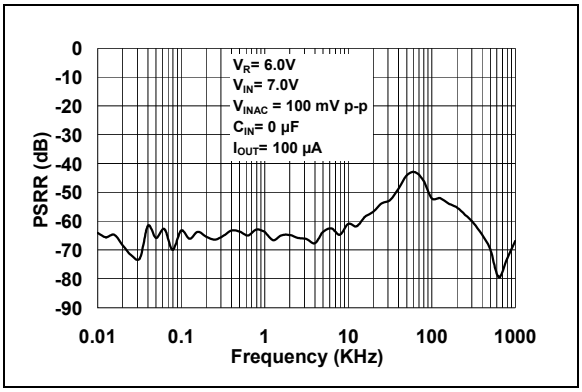

FIGURE 2-25: *PSRR vs Frequency.*

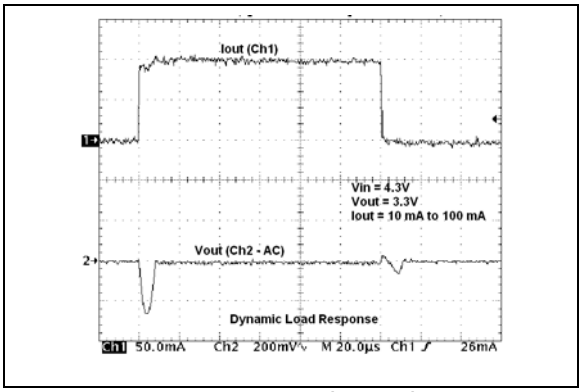

FIGURE 2-28: *Dynamic Load Response.*

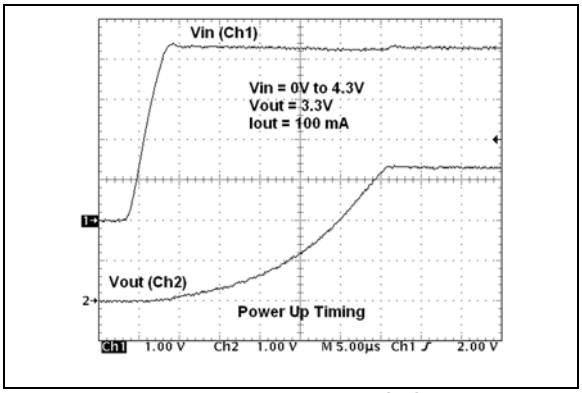

FIGURE 2-26: *Power Up Timing.*

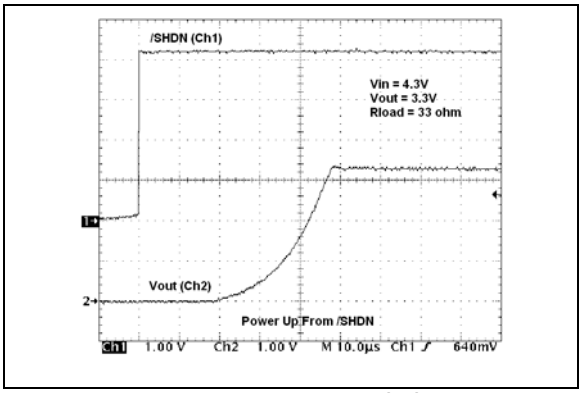

FIGURE 2-29: *Power Up Timing From SHDN.*

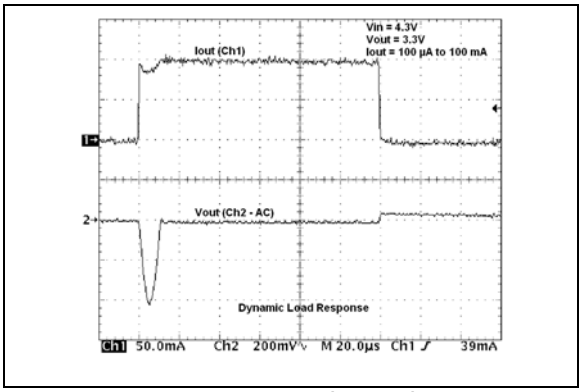

FIGURE 2-27: *Dynamic Load Response.*

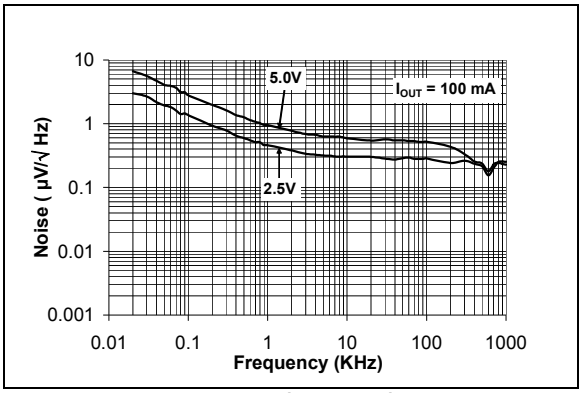

FIGURE 2-30: *Noise Graph.*

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NOTES:

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. SOT-23-5	Name	Function
1	V_{IN}	Unregulated Supply Voltage
2	GND	Ground Terminal
3	$\overline{SHDN}$	Shutdown
4	NC	No connection
5	V_{OUT}	Regulated Voltage Output

3.1 Unregulated Input Voltage (V_{IN})

Connect V_{IN} to the input unregulated source voltage. Like all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 0.1 µF of capacitance will ensure stable operation of the LDO circuit. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.2 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (25 µA typical) flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.3 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO output voltage is disabled and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.01 µA. The $\overline{SHDN}$ pin does not have an internal pull-up or pull-down resistor. The the $\overline{SHDN}$ pin must be connected to either V_{IN} or GND to prevent the device from becoming unstable.

3.4 Regulated Output Voltage (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO V_{OUT} pin as is practical. The current flowing out of this pin is equal to the DC load current.

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4.0 DETAILED DESCRIPTION

4.1 Output Regulation

A portion of the LDO output voltage is fed back to the internal error amplifier and compared with the precision internal bandgap reference. The error amplifier output will adjust the amount of current that flows through the P-Channel pass transistor, thus regulating the output voltage to the desired value. Any changes in input voltage or output current will cause the error amplifier to respond and adjust the output voltage to the target voltage (refer to Figure 4-1).

4.2 Overcurrent

The MCP1802 internal circuitry monitors the amount of current flowing through the P-Channel pass transistor. In the event that the load current reaches the current limiter level of 380 mA (typical), the current limiter circuit will operate and the output voltage will drop. As the output voltage drops, the internal current foldback circuit will further reduce the output voltage causing the output current to decrease. When the output is shorted, a typical output current of 50 mA flows.

4.3 Shutdown

The $\overline{\text{SHDN}}$ input is used to turn the LDO output voltage on and off. When the $\overline{\text{SHDN}}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{\text{SHDN}}$ input is pulled to a logic-low level, the LDO output voltage is disabled and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.01 µA. The $\overline{\text{SHDN}}$ pin does not have an internal pull-up or pull-down resistor. Therefore the $\overline{\text{SHDN}}$ pin must be pulled either high or low to prevent the device from becoming unstable. The internal device current will increase when the device is operational and current flows through the pull-up or pull-down resistor to the $\overline{\text{SHDN}}$ pin internal logic. The $\overline{\text{SHDN}}$ pin internal logic is equivalent to an inverter input.

4.4 Output Capacitor

The MCP1802 requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 milli-ohms.

Larger LDO output capacitors can be used with the MCP1802 to improve dynamic performance and power supply ripple rejection performance. Aluminum-electrolytic capacitors are not recommended for low temperature applications of ≤ 25°C.

4.5 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 0.1 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent (or higher) value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

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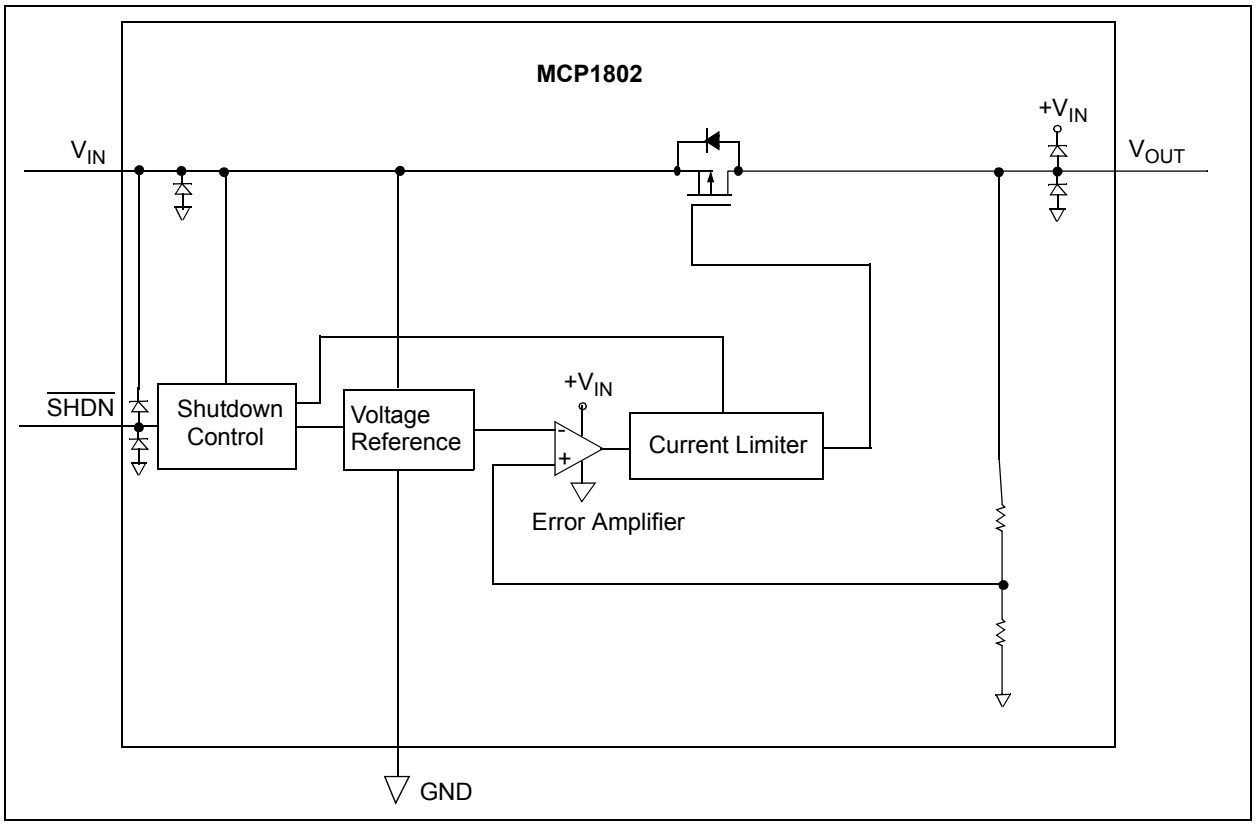

FIGURE 4-1: *Block Diagram.*

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5.0 FUNCTIONAL DESCRIPTION

The MCP1802 CMOS low dropout linear regulator is intended for applications that need the low current consumption while maintaining output voltage regulation. The operating continuous load range of the MCP1802 is from 0 mA to 300 mA. The input operating voltage range is from 2.0V to 10.0V, making it capable of operating from three or more alkaline cells or single and multiple Li-Ion cell batteries.

5.1 Input

The input of the MCP1802 is connected to the source of the P-Channel PMOS pass transistor. As with all LDO circuits, a relatively low source impedance (10Ω) is needed to prevent the input impedance from causing the LDO to become unstable. The size and type of the capacitor needed depends heavily on the input source type (battery, power supply) and the output current range of the application. For most applications a 0.1 µF ceramic capacitor will be sufficient to ensure circuit stability. Larger values can be used to improve circuit AC performance.

5.2 Output

The maximum rated continuous output current for the MCP1802 is 300 mA.

A minimum output capacitance of 1.0 µF is required for small signal stability in applications that have up to 300 mA output current capability. The capacitor type can be ceramic, tantalum or aluminum electrolytic.

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6.0 APPLICATION CIRCUITS & ISSUES

6.1 Typical Application

The MCP1802 is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for many battery-powered applications.

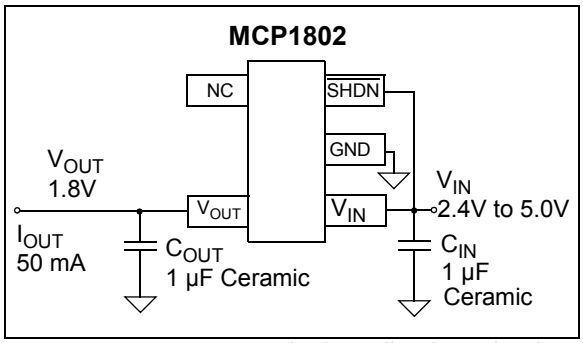

FIGURE 6-1: *Typical Application Circuit.*

6.1.1 APPLICATION INPUT CONDITIONS

Package Type	=	SOT-23-5
Input Voltage Range	=	2.4V to 5.0V
V_{IN} maximum	=	5.0V
V_{OUT} typical	=	1.8V
I_{OUT}	=	50 mA maximum

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1802 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant (25.0 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

Where:

P_{LDO}	=	LDO Pass device internal power dissipation
$V_{IN(MAX)}$	=	Maximum input voltage
$V_{OUT(MIN)}$	=	LDO minimum output voltage

The maximum continuous operating temperature specified for the MCP1802 is +85°C. To estimate the internal junction temperature of the MCP1802, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-23-5 package is estimated at 256°C/W.

EQUATION 6-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

Where:

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction to ambient
T_{AMAX}	=	Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 6-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$	=	Maximum device power dissipation
$T_{J(MAX)}$	=	Maximum continuous junction temperature
$T_{A(MAX)}$	=	Maximum ambient temperature
$R\theta_{JA}$	=	Thermal resistance from junction to ambient

EQUATION 6-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

Where:

$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
P_{TOTAL}	=	Maximum device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction to ambient

EQUATION 6-5:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J	=	Junction Temperature
$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
T_A	=	Ambient temperature

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6.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = SOT-23-5

Input Voltage

V_{IN} = 2.4V to 5.0V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 50 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

$P_{LDO} = (5.0V - (0.98 \times 1.8V)) \times 50$ mA

P_{LDO} = 161.8 milli-Watts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, *"High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages"*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"*, (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times Rq_{JA}$

T_{JRISE} = 161.8 milli-Watts x 256.0°C/Watt

T_{JRISE} = 41.42°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated in the following table.

$T_J = T_{JRISE} + T_{A(MAX)}$

T_J = 81.42°C

Maximum Package Power Dissipation at +25°C Ambient Temperature

SOT-23-5 (256°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (85°C - 25°C) / 256°C/W

$P_{D(MAX)}$ = 234 milli-Watts

6.4 Voltage Reference

The MCP1802 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1802 LDO. The low cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1802 as a voltage reference.

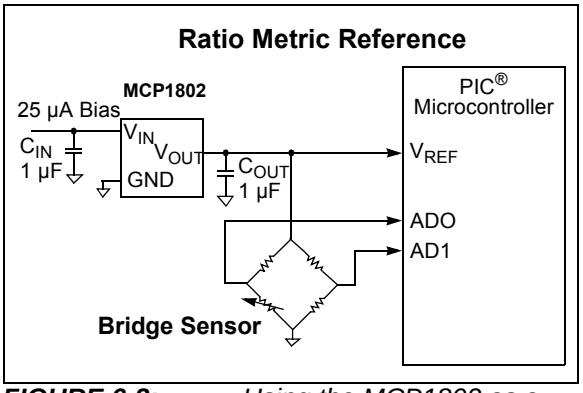

FIGURE 6-2: *Using the MCP1802 as a Voltage Reference.*

6.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 300 mA maximum specification of the MCP1802. The internal current limit of the MCP1802 will prevent high peak load demands from causing non-recoverable damage. The 300 mA rating is a maximum average continuous rating. As long as the average current does not exceed 300 mA nor the max power dissipation of the packaged device, pulsed higher load currents can be applied to the MCP1802. The typical current limit for the MCP1802 is 380 mA (T_A +25°C).

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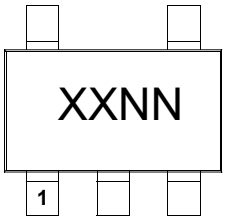
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

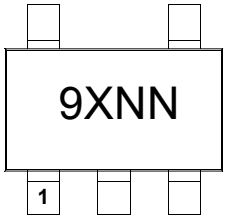
5-Lead SOT-23



Standard Options for SOT-23			
Symbol	**Voltage ***	**Symbol**	**Voltage ***
9X_8#	0.9	9X_Z#	3.0
9X_B#	1.2	9B_2#	3.3
9X_K#	1.8	9B_M#	5.0
9X_T#	2.5	9B_Z#	6.0

* Custom output voltages available upon request. Contact your local Microchip sales office for more information.

Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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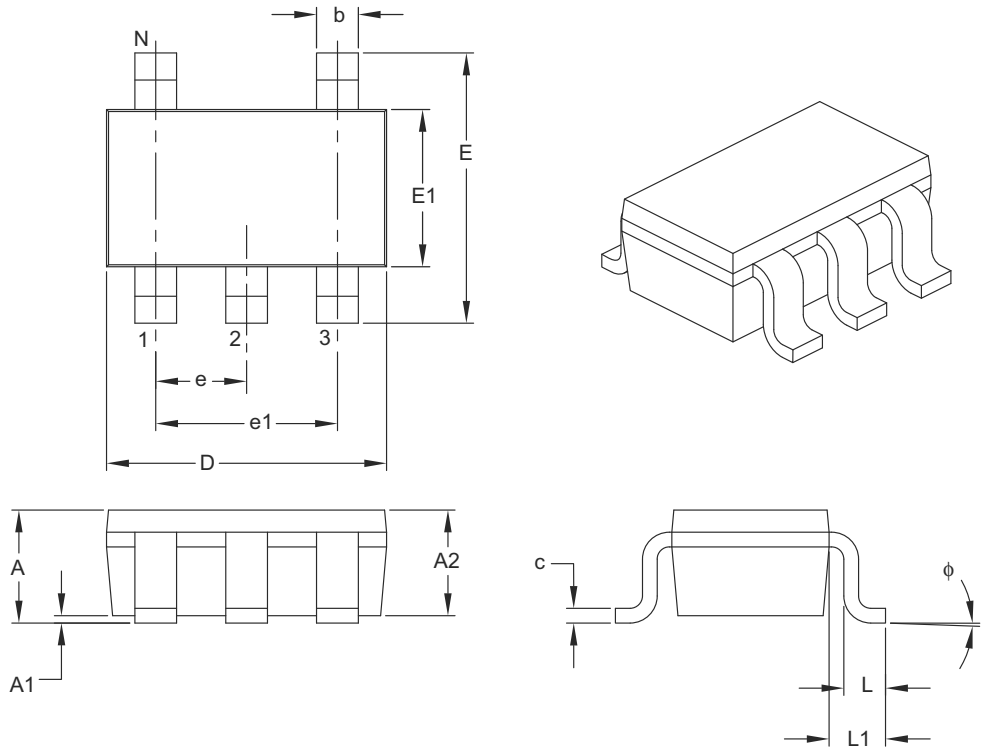
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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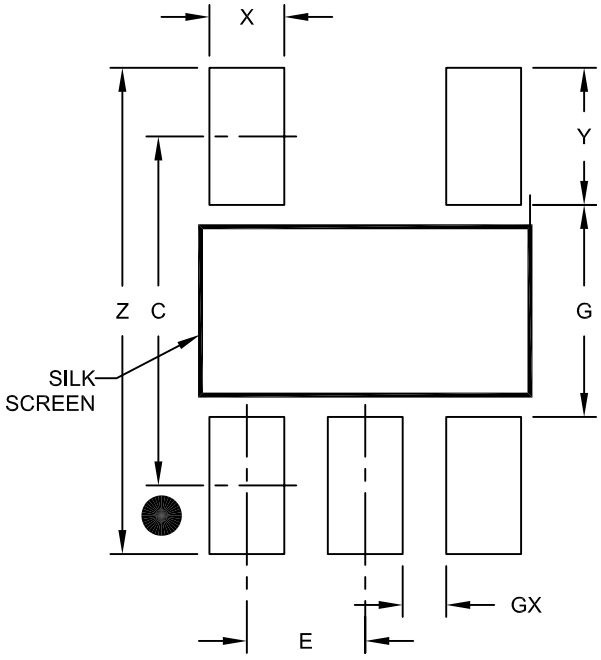
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision C (October 2010)

The following is the list of modifications:

1. Removed Note 1 reference from the Dropout Voltage Parameter in the Electrical Characteristics table.
2. Added Land Pattern package outline drawing C04-2091A.

Revision B (January 2009)

The following is the list of modifications:

1. Added Shutdown Input information to the **"Electrical characteristics"** table.
2. Added Figure 2-30.

Revision A (June 2007)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	XX	X	X	X/	XX
Device	Tape and Reel	Output Voltage	Feature Code	Tolerance	Temp.	Package

Device:	MCP1802: 150 mA, Low Quiescent Current LDO
Tape and Reel:	T = Tape and Reel
Output Voltage *:	09 = 0.9V “Standard” 12 = 1.2V “Standard” 18 = 1.8V “Standard” 25 = 2.5V “Standard” 30 = 3.0V “Standard” 33 = 3.3V “Standard” 50 = 5.0V “Standard” 60 = 6.0V “Standard” *Contact factory for other output voltage options.
Extra Feature Code:	0 = Fixed
Tolerance:	2 = 2.0% (Standard)
Temperature:	I = -40°C to +85°C
Package Type:	OT = Plastic Small Outline Transistor (SOT-23) 5-lead,

Examples:

a) MCP1802T-0902I/OT: Tape and Reel, 0.9V

b) MCP1802T-1202I/OT: Tape and Reel, 1.2V

c) MCP1802T-1802I/OT: Tape and Reel, 1.8V

d) MCP1802T-2502I/OT: Tape and Reel, 2.5V

e) MCP1802T-3002I/OT: Tape and Reel, 3.0V

f) MCP1802T-3302I/OT: Tape and Reel, 3.3V

g) MCP1802T-5002I/OT: Tape and Reel, 5.0V

h) MCP1802T-6002I/OT: Tape and Reel, 6.0V

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