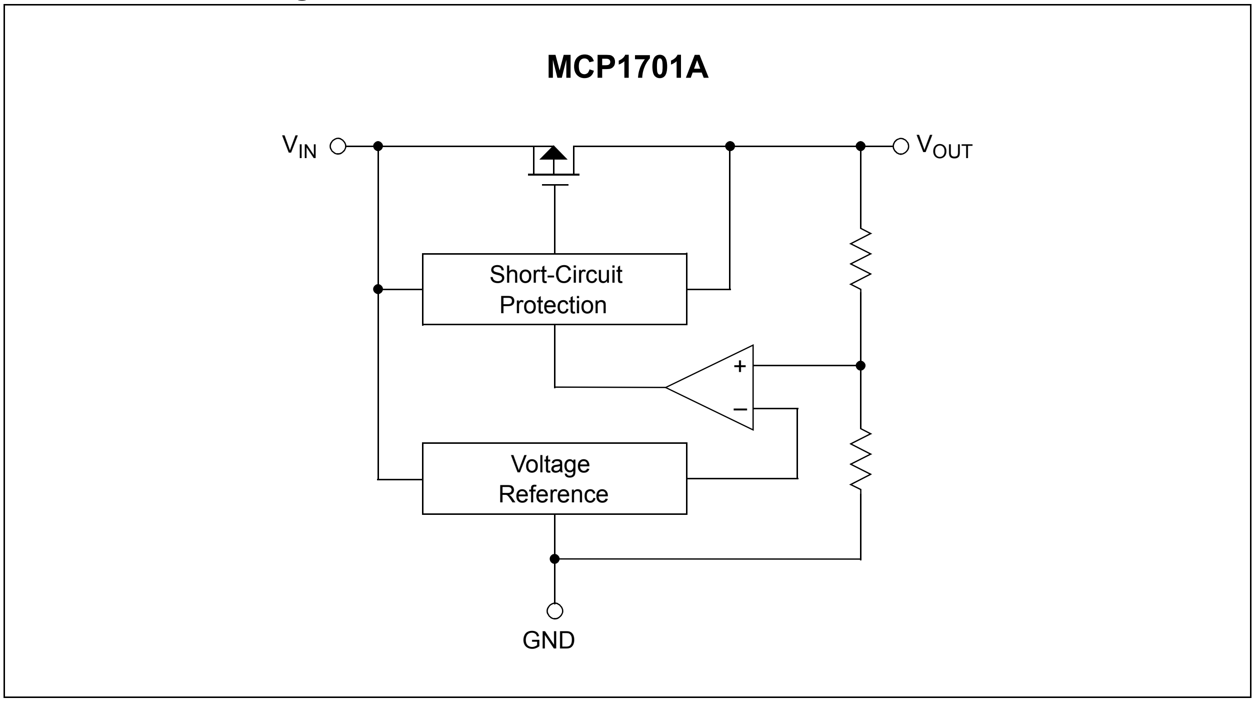
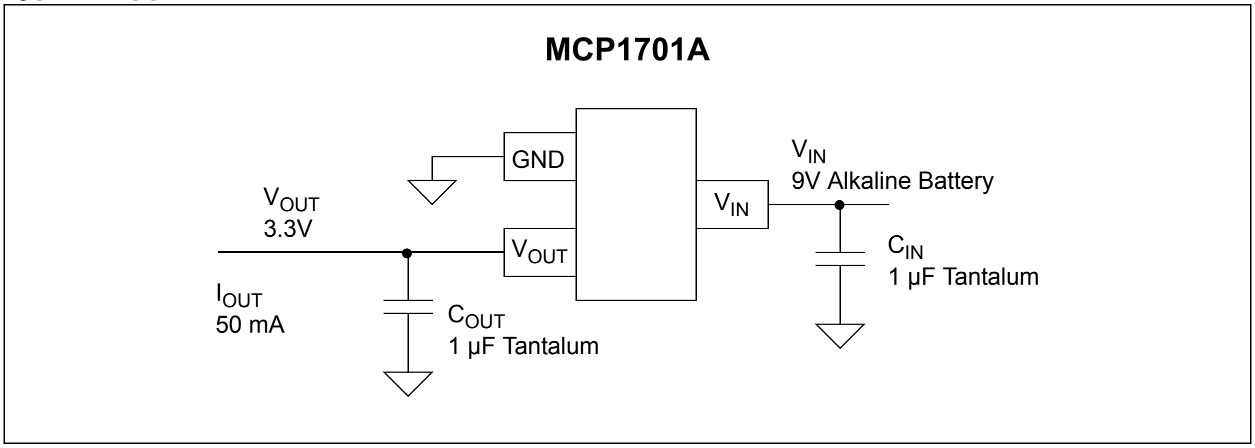
Functional Block Diagram



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage ....+12V
Output Current (Continuous)..........$P_D/(V_{IN} – V_{OUT})$mA
Output Current (peak) .... 500 mA
Output Voltage .... (GND – 0.3V) to (V_{IN} + 0.3V)
Continuous Power Dissipation:
- 3-Pin SOT-23A .... 150 mW
- 3-Pin SOT-89... 500 mW
- 3-Pin TO-92 .... 300 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for an ambient temperature of T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output Voltage Regulation	V_{OUT}	V_R - 2%	V_R±0.5%	V_R + 2%	V	I_{OUT} = 40 mA **(Note 1)**
Maximum Output Current	I_{OUTMAX}	250	—	—	mA	V_{OUT} = 5.0V ($V_{IN} = V_R$ + 1.0V)
		200	—	—		V_{OUT} = 4.0V
		150	—	—		V_{OUT} = 3.3V
		150	—	—		V_{OUT} = 3.0V
		125	—	—		V_{OUT} = 2.5V
		110	—	—		V_{OUT} = 1.8V
Load Regulation **(Note 3)**	$\Delta V_{OUT}/V_{OUT}$	-1.60	±0.8	+1.60	%	V_{OUT} = 5.0V, 1 mA ≤ I_{OUT} ≤ 100 mA
		-2.25	±1.1	+2.25		V_{OUT} = 4.0V, 1 mA ≤ I_{OUT} ≤ 100 mA
		-2.72	±1.3	+2.72		V_{OUT} = 3.3V, 1 mA ≤ I_{OUT} ≤ 80 mA
		-3.00	±1.5	+3.00		V_{OUT} = 3.0V, 1 mA ≤ I_{OUT} ≤ 80 mA
		-3.60	±1.8	+3.60		V_{OUT} = 2.5V, 1 mA ≤ I_{OUT} ≤ 60 mA
		-1.60	±0.8	+1.60		V_{OUT} = 1.8V, 1 mA ≤ I_{OUT} ≤ 30 mA
Dropout Voltage	$V_{IN} - V_{OUT}$	—	380	600	mV	I_{OUT} = 200 mA, V_R = 5.0V
		—	400	630		I_{OUT} = 200 mA, V_R = 4.0V
		—	400	700		I_{OUT} = 150 mA, V_R = 3.3V
		—	400	700		I_{OUT} = 150 mA, V_R = 3.0V
		—	400	700		I_{OUT} = 120 mA, V_R = 2.5V
		—	180	300		I_{OUT} = 20 mA, V_R = 1.8V
Input Quiescent Current	I_Q	—	2.0	4.5	µA	$V_{IN} = V_R$ + 1.0V
Line Regulation	$\frac{\Delta V_{OUT} \cdot 100}{\Delta V_{IN} \cdot V_{OUT}}$	—	0.2	0.3	%/V	I_{OUT} = 40 mA, (V_R +1) ≤ V_{IN} ≤ 10.0V
Input Voltage	V_{IN}	—	—	10	V	
Temperature Coefficient of Output Voltage	TCV_{OUT}	—	±100	—	ppm/°C	I_{OUT} = 40 mA, -40°C ≤ T_A ≤ +85°C **(Note 2)**
Output Rise Time	T_R	—	200	—	µs	10% V_R to 90% V_R, V_{IN} = 0V to V_R +1V, R_L = 25Ω resistive

1: V_R is the nominal regulator output voltage. For example: V_R = 1.8V, 2.5V, 3.3V, 4.0V, 5.0V. The input voltage $V_{IN} = V_R$ + 1.0V, I_{OUT} = 40 mA.

2: $TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = Highest voltage measured over the temperature range. $V_{OUT-LOW}$ = Lowest voltage measured over the temperature range.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (I)	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-40	—	+125	°C	
Package Thermal Resistances						
Thermal Resistance, 3L-SOT-23A	θ_{JA}	—	335	—	°C/W	Minimum trace width single layer application
		—	230	—	°C/W	Typical FR4, 4-layer application
Thermal Resistance, 3L-SOT-89	θ_{JA}	—	52	—	°C/W	Typical, when mounted on 1 square inch of copper
Thermal Resistance, 3L-TO-92	θ_{JA}	—	131.9	—	°C/W	EIA/JEDEC JESD51-751-7 4-layer board

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Notes: Unless otherwise specified, V_{OUT} = 1.8V, 3.3V, 5.0V, T_A = +25°C, C_{IN} = 1 µF Tantalum, C_{OUT} = 1 µF Tantalum.

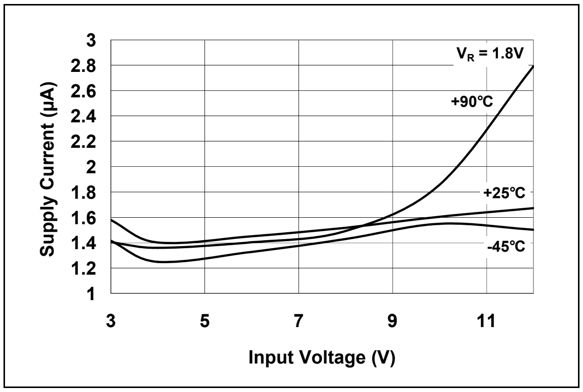


FIGURE 2-1: *Supply Current vs. Input Voltage (V_R = 1.8V).*

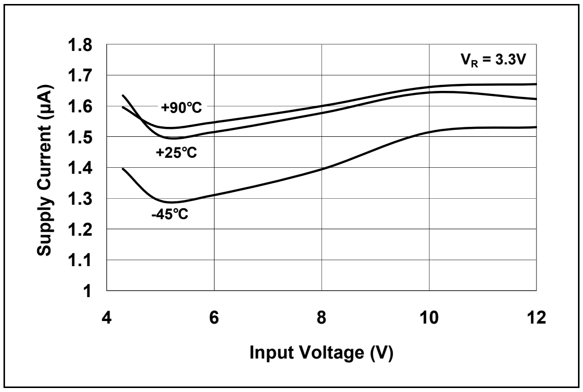


FIGURE 2-2: *Supply Current vs. Input Voltage (V_R = 3.3V).*

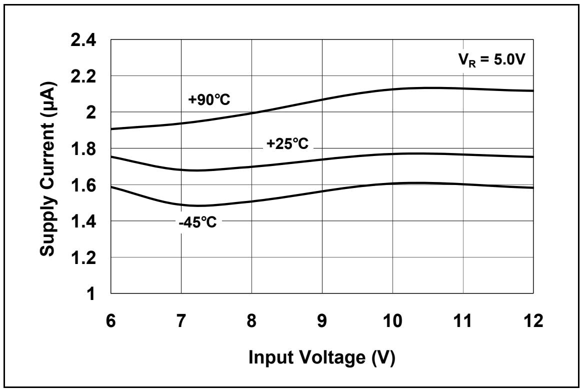


FIGURE 2-3: *Supply Current vs. Input Voltage (V_R = 5.0V).*

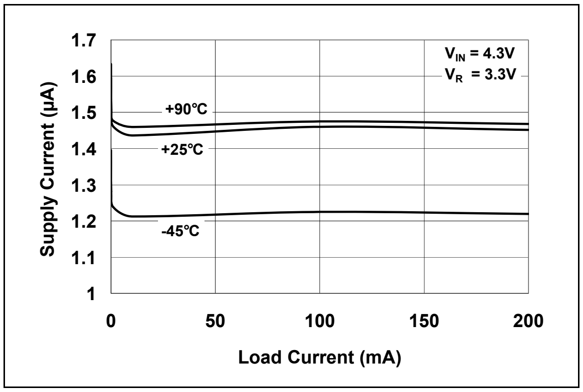


FIGURE 2-4: *Supply Current vs. Load Current (V_R = 3.3V).*

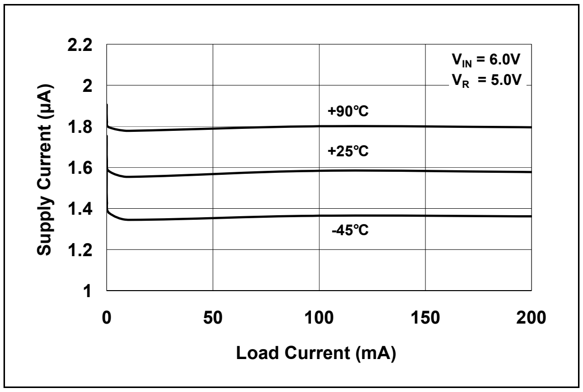


FIGURE 2-5: *Supply Current vs. Load Current (V_R = 5.0V).*

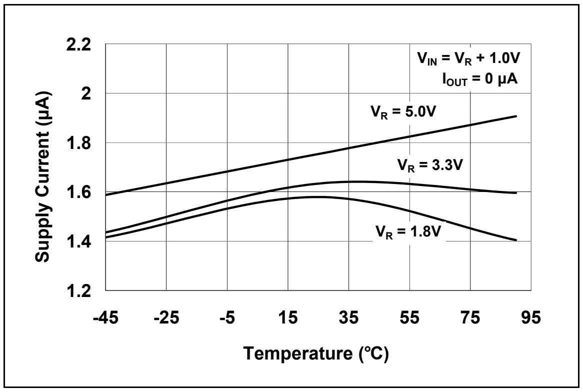


FIGURE 2-6: *Supply Current vs. Temperature.*

Note: Unless otherwise indicated, V_{OUT} = 1.8V, 3.3V, 5.0V, T_A = +25°C, C_{IN} = 1 µF Tantalum, C_{OUT} = 1 µF Tantalum.

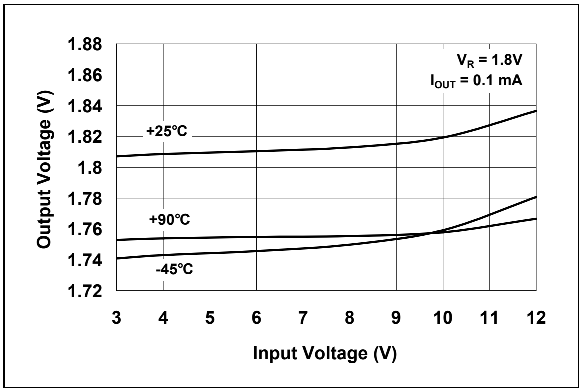


FIGURE 2-7: *Output Voltage vs. Input Voltage (V_R = 1.8V).*

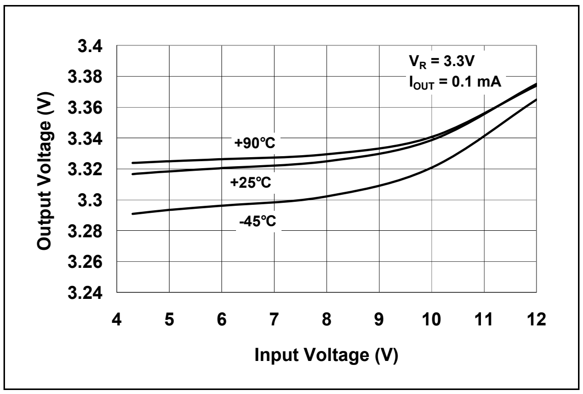


FIGURE 2-8: *Output Voltage vs. Input Voltage (V_R = 3.3V).*

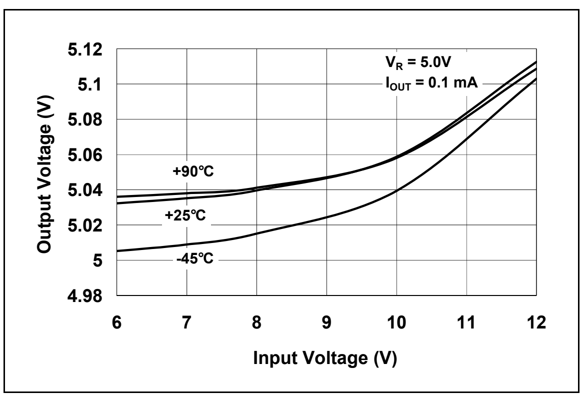


FIGURE 2-9: *Output Voltage vs. Input Voltage (V_R = 5.0V).*

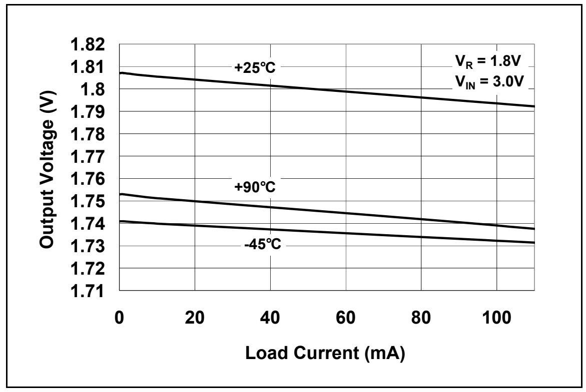


FIGURE 2-10: *Output Voltage vs. Load Current (V_R = 1.8V).*

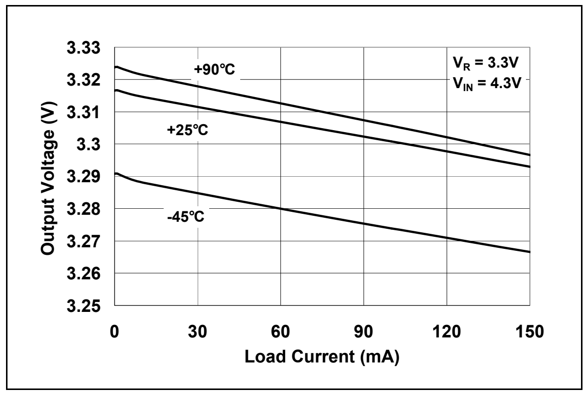


FIGURE 2-11: *Output Voltage vs. Load Current (V_R = 3.3V).*

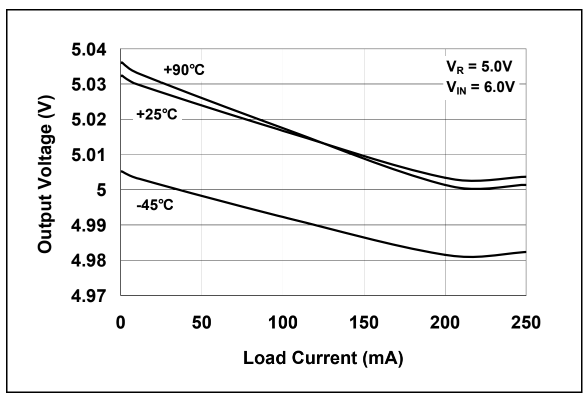


FIGURE 2-12: *Output Voltage vs. Load Current (V_R = 5.0V).*

Note: Unless otherwise indicated, V_{OUT} = 1.8V, 3.3V, 5.0V, T_A = +25°C, C_{IN} = 1 µF Tantalum, C_{OUT} = 1 µF Tantalum.

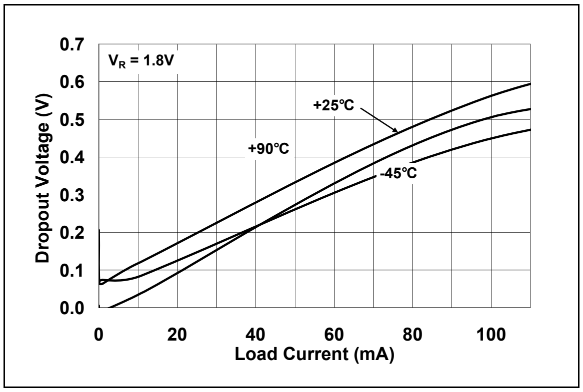


FIGURE 2-13: *Dropout Voltage vs. Load Current (V_R = 1.8V).*

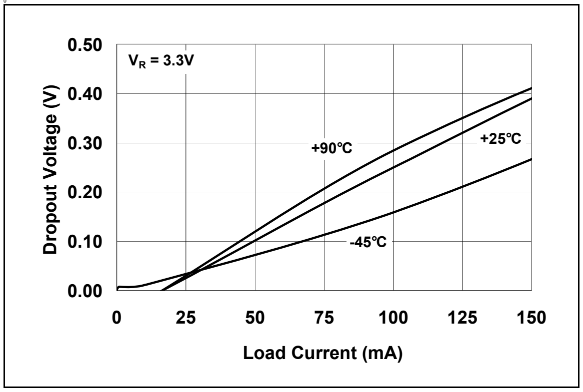


FIGURE 2-14: *Dropout Voltage vs. Load Current (V_R = 3.3V).*

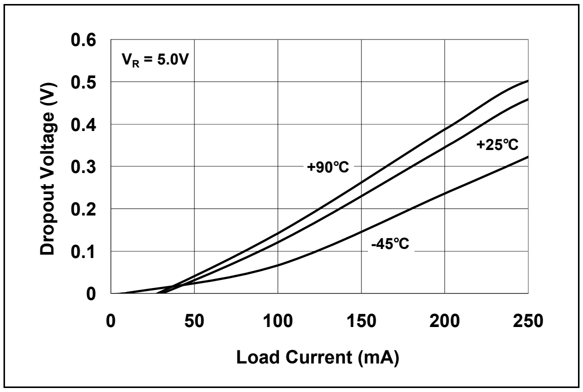


FIGURE 2-15: *Dropout Voltage vs. Load Current (V_R = 5.0V).*

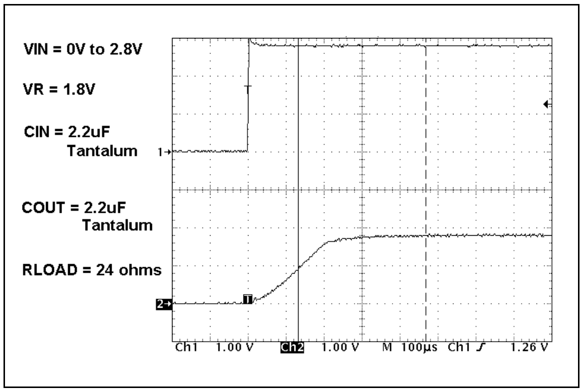


FIGURE 2-16: *Start-up From V_{IN} (V_R = 1.8V).*

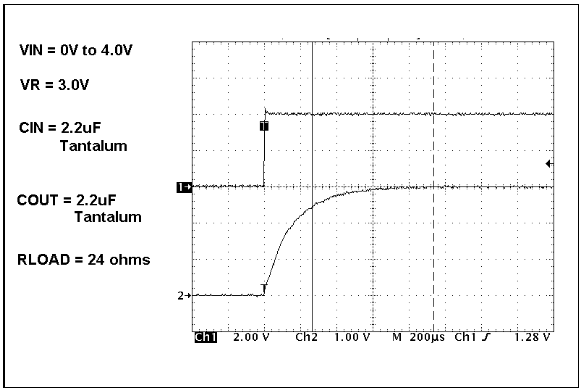


FIGURE 2-17: *Start-up From V_{IN} (V_R = 3.3V).*

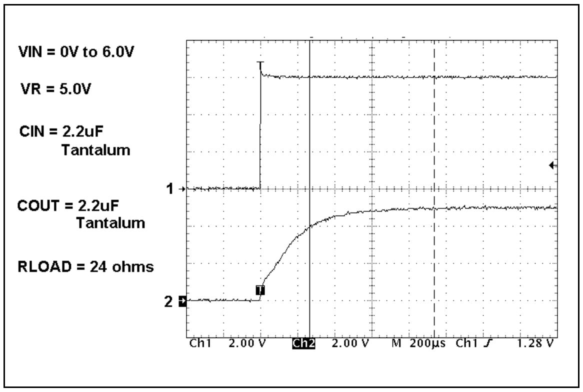


FIGURE 2-18: *Start-up From V_{IN} (V_R = 5.0V).*

Note: Unless otherwise indicated, V_{OUT} = 1.8V, 3.3V, 5.0V, T_A = +25°C, C_{IN} = 1 µF Tantalum, C_{OUT} = 1 µF Tantalum.

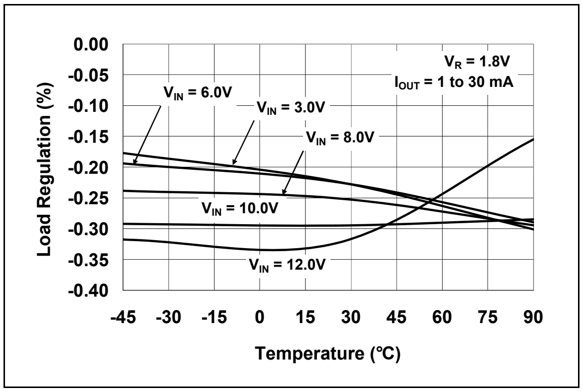


FIGURE 2-19: *Load Regulation vs. Temperature (V_R = 1.8V).*

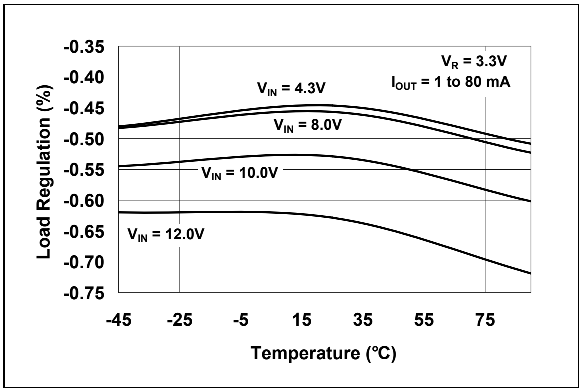


FIGURE 2-20: *Load Regulation vs. Temperature (V_R = 3.3V).*

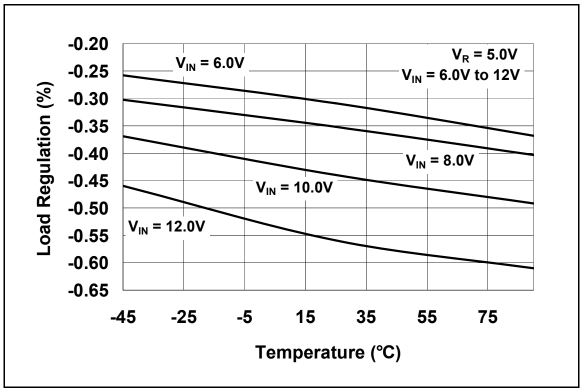


FIGURE 2-21: *Load Regulation vs. Temperature (V_R = 5.0V).*

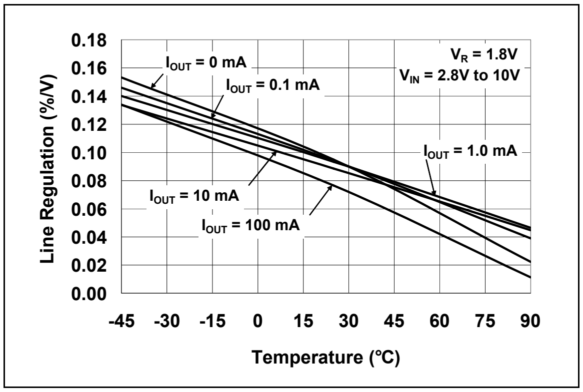


FIGURE 2-22: *Line Regulation vs. Temperature (V_R = 1.8V).*

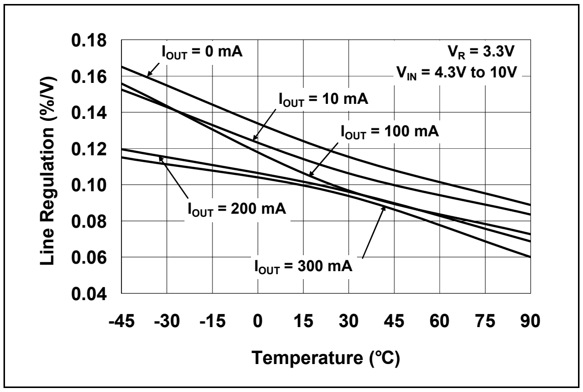


FIGURE 2-23: *Line Regulation vs. Temperature (V_R = 3.3V).*

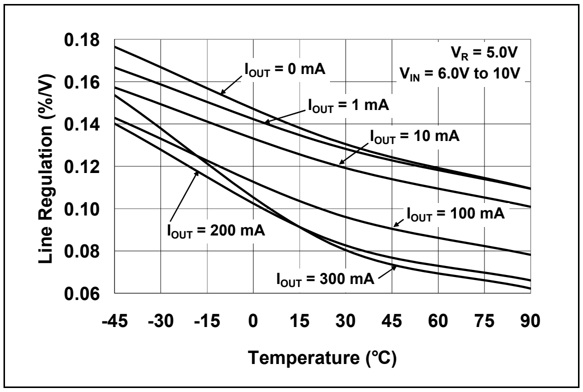


FIGURE 2-24: *Line Regulation vs. Temperature (V_R = 5.0V).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. SOT-23A	Pin No. SOT-89	Pin No. TO-92	Name	Function
1	1	1	GND	Ground Terminal
2	3	3	V_{OUT}	Regulated Voltage Output
3	2	2	V_{IN}	Unregulated Supply Input

3.1 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (2 µA, typ.) flows out of this pin, there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.2 Regulated Voltage Output (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close as possible to the LDO V_{OUT} pin. The current flowing out of this pin is equal to the DC load current.

3.3 Unregulated Supply Input (V_{IN})

Connect the input supply voltage and the positive side of the input capacitor to V_{IN}. Like all low-dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. The input capacitor should be physically located as close as possible to the V_{IN} pin. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. For applications that have load currents below 100 mA, the input capacitance requirement can be lowered. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low equivalent series resistance characteristics of the ceramic will yield better noise and PSRR performance at high frequency. The current flow into this pin is equal to the DC load current, plus the LDO bias current (2 µA, typical).

4.0 DETAILED DESCRIPTION

The MCP1701A is a low-quiescent current, precision, fixed-output voltage LDO. Unlike bipolar regulators, the MCP1701A supply current does not increase proportionally with load current.

4.1 Output Capacitor

A minimum of 1 µF output capacitor is required. The output capacitor should have an ESR greater than 0.1Ω and less than 5Ω, plus a resonant frequency above 1 MHz. Larger output capacitors can be used to improve supply noise rejection and transient response. Care should be taken when increasing C_{OUT} to ensure that the input impedance is not high enough to cause high input impedance oscillation.

4.2 Input Capacitor

A 1 µF input capacitor is recommended for most applications when the input impedance is on the order of 10Ω. Larger input capacitance may be required for stability when operating from a battery input, or if there is a large distance from the input source to the LDO. When large values of output capacitance are used, the input capacitance should be increased to prevent high source impedance oscillations.

4.3 Overcurrent

The MCP1701 internal circuitry monitors the amount of current flowing through the P-channel pass transistor. In the event of a short circuit or excessive output current, the MCP1701 will act to limit the output current.

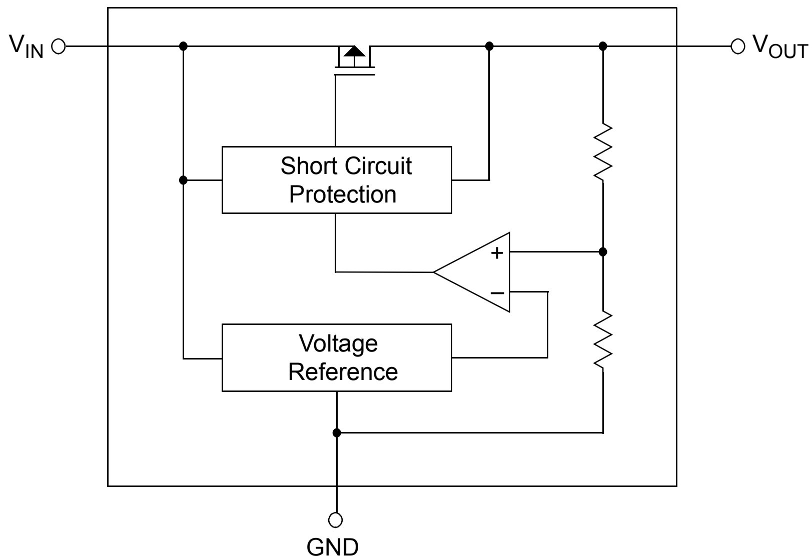


FIGURE 4-1: *MCP1701A Block Diagram.*

5.0 THERMAL CONSIDERATIONS

5.1 Power Dissipation

The amount of power dissipated internal to the LDO linear regulator is the sum of the power dissipation within the linear pass device (P-channel MOSFET) and the quiescent current required to bias the internal reference and error amplifier. The internal linear pass device power dissipation is calculated as shown in Equation 5-1.

EQUATION 5-1:

$$P_D\ (Pass\ Device) = (V_{IN} - V_{OUT})\ x\ I_{OUT}$$

The internal power dissipation, as a result of the bias current for the LDO internal reference and error amplifier, is calculated as shown in Equation 5-2.

EQUATION 5-2:

$$P_D\ (Bias) = V_{IN}\ x\ I_{GND}$$

The total internal power dissipation is the sum of P_D (pass device) and P_D (bias).

EQUATION 5-3:

$$P_{TOTAL} = P_D\ (Pass\ Device) + P_D\ (Bias)$$

For the MCP1701A, the internal quiescent bias current is so low (2 µA, typ.) that the P_D (bias) term of the power dissipation equation can be ignored. The maximum power dissipation can be estimated by using the maximum input voltage and the minimum output voltage to obtain a maximum voltage differential between input and output. The next step would be to multiply the maximum voltage differential by the maximum output current.

EQUATION 5-4:

$$P_D = (V_{INMAX} - V_{OUTMIN})\ x\ I_{OUTMAX}$$

Given:

V_{IN}	=	3.3V to 4.1V
V_{OUT}	=	3.0V ± 2%
I_{OUT}	=	1 mA to 100 mA
T_{AMAX}	=	55°C
P_{MAX}	=	(4.1V – (3.0V x 0.98)) x 100 mA

To determine the junction temperature of the device, the thermal resistance from junction-to-ambient must be known. The 3-pin SOT-23A thermal resistance from junction-to-air ($R_{\theta JA}$) is estimated to be approximately 335°C/W. The SOT-89 $R_{\theta JA}$ is estimated to be approximately 52°C/W when mounted on 1 square inch of copper. The $R_{\theta JA}$ will vary with physical layout, airflow and other application-specific conditions.

The device junction temperature is determined by calculating the junction temperature rise above ambient, then adding the rise to the ambient temperature.

EQUATION 5-5: JUNCTION TEMPERATURE – SOT-23A EXAMPLE:

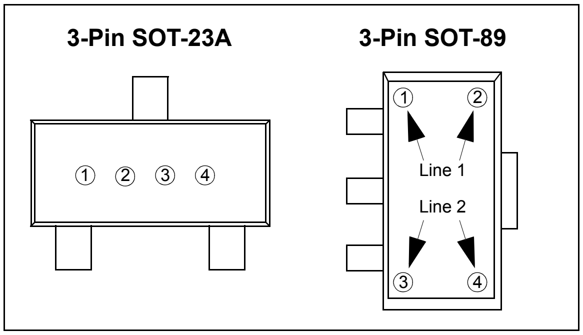
$$T_J = P_{DMAX} \times R_{\theta JA} + T_A$$
$$T_J = 116.0\ milliwatts \times 335°C/W + 55°C$$
$$T_J = 93.9°C$$

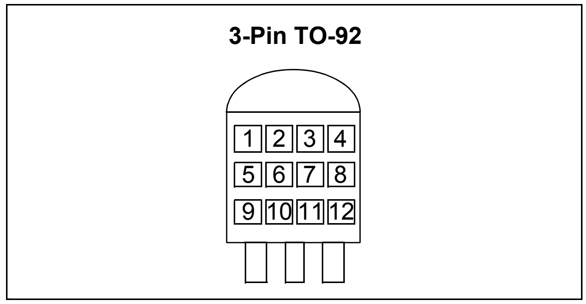
EQUATION 5-6: JUNCTION TEMPERATURE – SOT-89 EXAMPLE:

$$T_J = 116.0\ milliwatts \times 52°C/W + 55°C$$
$$T_J = 61°C$$

6.0 PACKAGING INFORMATION

6.1 Package Marking Information





① represents first voltage digit
1V, 2V, 3V, 4V, 5V, 6V

Ex: 3.xV = ③ ○ ○ ○

② represents first decimal place voltage (x.0 - x.9)

Ex: 3.4V = ③ Ⓔ ○ ○

Symbol	Voltage	Symbol	Voltage
A	x.0	F	x.5
B	x.1	H	x.6
C	x.2	K	x.7
D	x.3	L	x.8
E	x.4	M	x.9

③ represents polarity
0 = Positive (fixed)

④ represents assembly lot number

①, ②, ③ & ④ = 701A (fixed)

⑤ represents first voltage digit (1-6)

⑥ represents first voltage decimal (0-9)

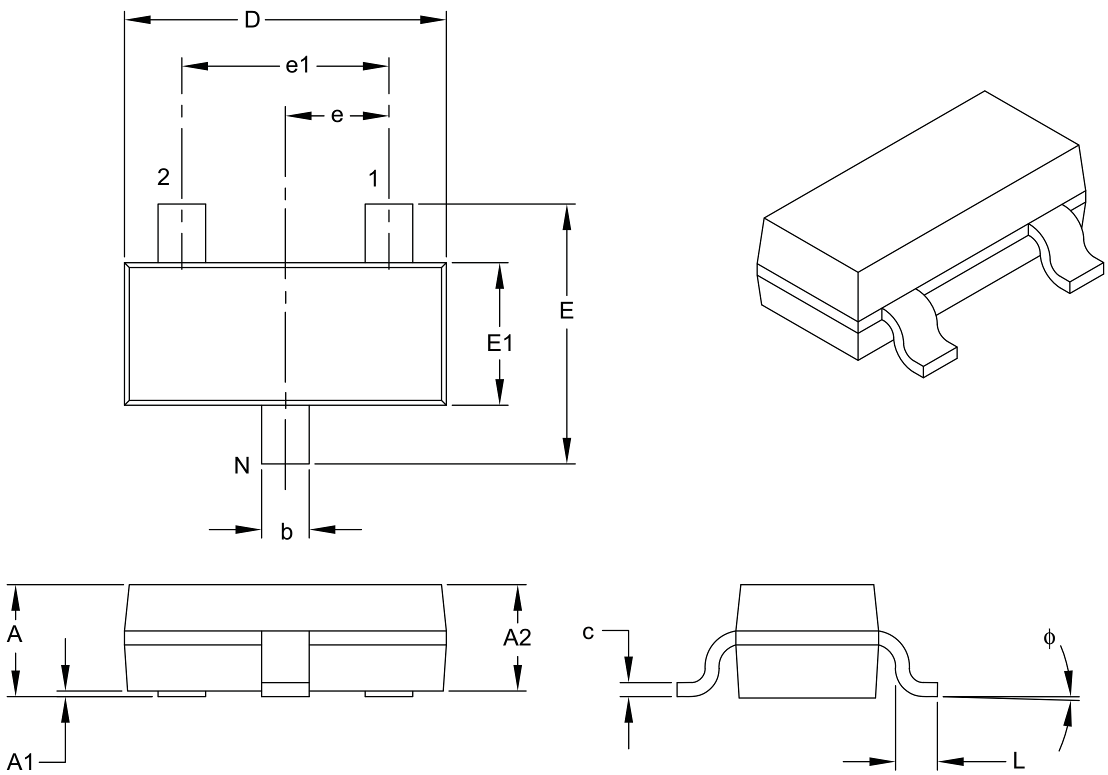
⑦ represents extra feature code: fixed: 0

⑧ represents regulation accuracy
2 = ±2.0% (standard)

⑨, ⑩, ⑪ & ⑫ represents assembly lot number

3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	3		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.89	–	1.45
Molded Package Thickness	A2	0.90	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.10	–	3.00
Molded Package Width	E1	1.20	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.15	–	0.60
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.09	–	0.26
Lead Width	b	0.30	–	0.51

Notes:

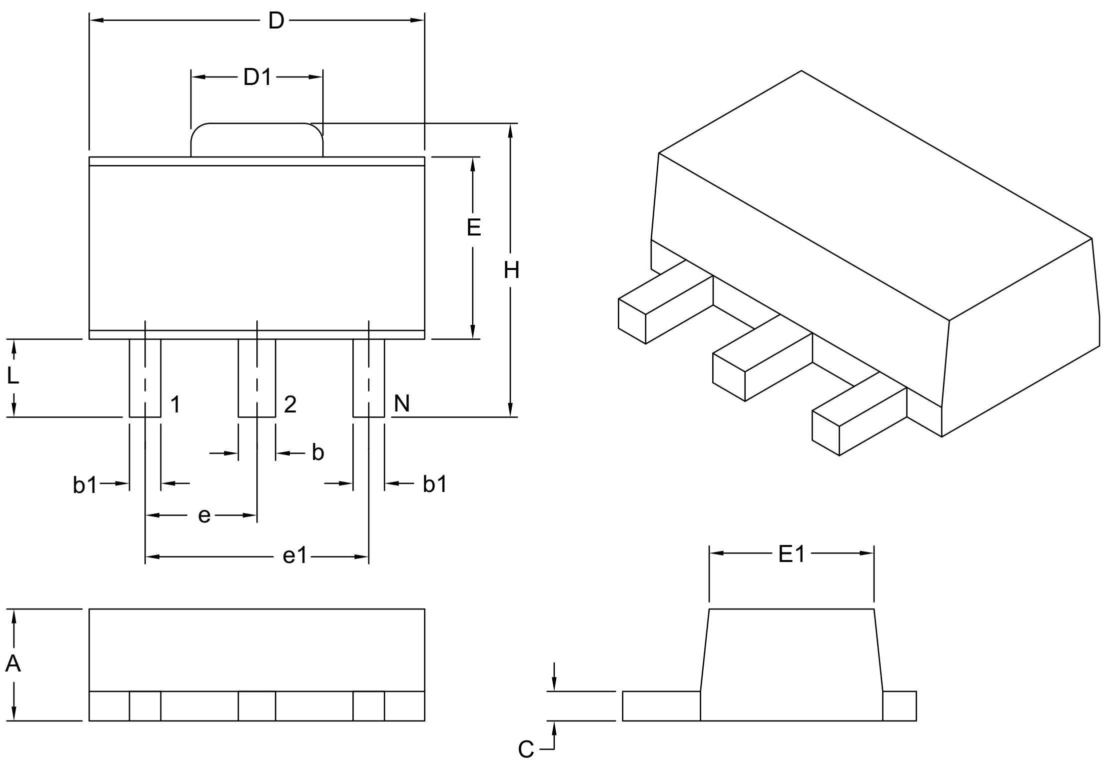
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-130B

3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS	
Dimension Limits		MIN	MAX
Number of Leads	N	3	
Pitch	e	1.50 BSC	
Outside Lead Pitch	e1	3.00 BSC	
Overall Height	A	1.40	1.60
Overall Width	H	3.94	4.25
Molded Package Width at Base	E	2.29	2.60
Molded Package Width at Top	E1	2.13	2.29
Overall Length	D	4.39	4.60
Tab Length	D1	1.40	1.83
Foot Length	L	0.79	1.20
Lead Thickness	c	0.35	0.44
Lead 2 Width	b	0.41	0.56
Leads 1 & 3 Width	b1	0.36	0.48

Notes:

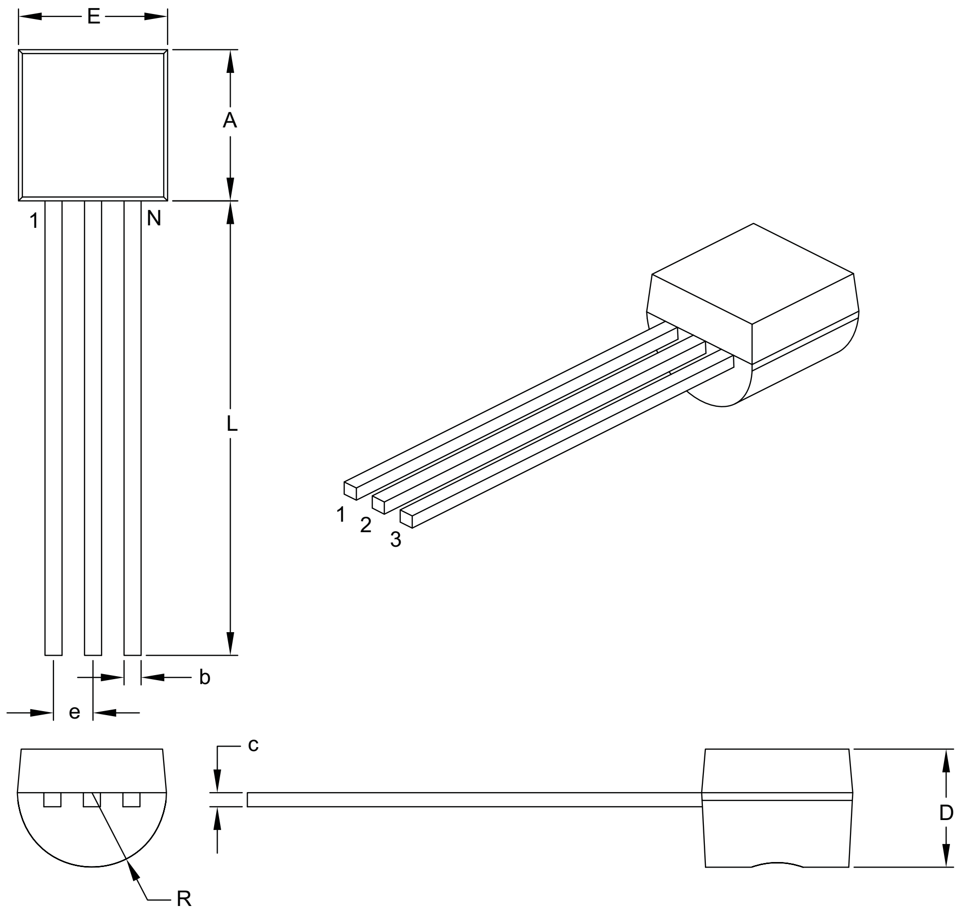
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029B

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES	
Dimension Limits		MIN	MAX
Number of Pins	N	3	
Pitch	e	.050 BSC	
Bottom to Package Flat	D	.125	.165
Overall Width	E	.175	.205
Overall Length	A	.170	.210
Molded Package Radius	R	.080	.105
Tip to Seating Plane	L	.500	–
Lead Thickness	c	.014	.021
Lead Width	b	.014	.022

Notes:

1. Dimensions A and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101B

NOTES:

APPENDIX A: REVISION HISTORY

Revisions C (February 2007)

- Updated Packaging Information

Revision B (September 2006)

- Numerous changes to Section 1.0. Electrical Characteristics
- Added disclaimer to package outline drawings.

Revision A (February 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	XX	X	X	X	/XX
Device	Tape and Reel	Output Voltage	Feature Code	Tolerance	Temp.	Package

Device:	MCP1701A: 2 µA Low-Dropout Positive Voltage Regulator		
Tape and Reel:	T	=	Tape and Reel
Output Voltage:	18	=	1.8V "Standard"
	25	=	2.5V "Standard"
	30	=	3.0V "Standard"
	33	=	3.3V "Standard"
	50	=	5.0V "Standard"
	*Contact factory for other output voltage options.		
Extra Feature Code:	0	=	Fixed
Tolerance:	2	=	2.0% (Standard)
Temperature:	I	=	-40°C to +85°C
Package Type:	CB	=	3-Pin SOT-23A (equivalent to EIAJ SC-59)
	MB	=	3-Pin SOT-89
	TO	=	3-Pin TO-92

Examples:

a) MCP1701AT-1802I/CB: 1.8V LDO Positive Voltage Regulator, SOT-23A-3 pkg.
b) MCP1701AT-1802I/MB: 1.8V LDO Positive Voltage Regulator, SOT89-3 pkg.
c) MCP1701A-1802I/TO: 1.8V LDO Positive Voltage Regulator, TO-92 pkg.
d) MCP1701AT-2502I/CB: 2.5V LDO Positive Voltage Regulator, SOT-23A-3 pkg.
e) MCP1701A-2502I/TO: 2.5V LDO Positive Voltage Regulator, TO-92 pkg.
f) MCP1701AT-3002I/CB: 3.0V LDO Positive Voltage Regulator, SOT-23A-3 pkg.
g) MCP1701AT-3002I/MB: 3.0V LDO Positive Voltage Regulator, SOT89-3 pkg.
h) MCP1701A-3002I/TO: 3.0V LDO Positive Voltage Regulator, TO-92 pkg.
i) MCP1701AT-3302I/CB: 3.3V LDO Positive Voltage Regulator, SOT-23A-3 pkg.
j) MCP1701AT-3302I/MB: 3.3V LDO Positive Voltage Regulator, SOT89-3 pkg.
k) MCP1701AT-5002I/CB: 5.0V LDO Positive Voltage Regulator, SOT-23A-3 pkg.
l) MCP1701AT-5002I/MB: 5.0V LDO Positive Voltage Regulator, SOT89-3 pkg.
m) MCP1701A-5002I/TO: 5.0V LDO Positive Voltage Regulator, TO-92 pkg.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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