







# MC14549B, MC14559B







## TRUTH TABLES

**MC14549B**

| SC | SC(t-1) | MR | MR(t-1) | Clock   | Action                      |
|----|---------|----|---------|---|-----------------------------|
| X  | X       | X  | X       |  | None                        |
| X  | X       | 1  | X       |  | Reset                       |
| 1  | 0       | 0  | 0       |  | Start Conversion            |
| 1  | X       | 0  | 1       |  | Start Conversion            |
| 1  | 1       | 0  | 0       |  | Continue Conversion         |
| 0  | X       | 0  | X       |  | Continue Previous Operation |

X = Don't Care t-1 = State at Previous Clock 

**MC14559B**

| SC | SC(t-1) | EOC | Clock   | Action                   |
|----|---------|-----|---|--------------------------|
| X  | X       | X   |  | None                     |
| 1  | 0       | 0   |  | Start Conversion         |
| X  | 1       | 0   |  | Continue Conversion      |
| 0  | 0       | 0   |  | Continue Conversion      |
| 0  | X       | 1   |  | Retain Conversion Result |
| 1  | X       | 1   |  | Start Conversion         |

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

| Characteristic  | Symbol                       | V <sub>DD</sub><br>Vdc | - 55°C  |        | 25°C  |                 |        | 125°C |        | Unit     |
|---|------------------------------|------------------------|---|--------|-------|-----------------|--------|-------|--------|----------|
|   |                              |                        | Min   | Max    | Min   | Typ<br>(Note 2) | Max    | Min   | Max    |          |
| Output Voltage<br>V <sub>in</sub> = V <sub>DD</sub> or 0  | "0" Level<br>V <sub>OL</sub> | 5.0                    | –   | 0.05   | –     | 0               | 0.05   | –     | 0.05   | Vdc      |
|   |                              | 10                     | –   | 0.05   | –     | 0               | 0.05   | –     | 0.05   |          |
|   |                              | 15                     | –   | 0.05   | –     | 0               | 0.05   | –     | 0.05   |          |
| V <sub>in</sub> = 0 or V <sub>DD</sub>  | "1" Level<br>V <sub>OH</sub> | 5.0                    | 4.95  | –      | 4.95  | 5.0             | –      | 4.95  | –      | Vdc      |
|   |                              | 10                     | 9.95  | –      | 9.95  | 10              | –      | 9.95  | –      |          |
|   |                              | 15                     | 14.95   | –      | 14.95 | 15              | –      | 14.95 | –      |          |
| Input Voltage (Note 2)<br>(V <sub>O</sub> = 4.5 or 0.5 Vdc)<br>(V <sub>O</sub> = 9.0 or 1.0 Vdc)<br>(V <sub>O</sub> = 13.5 or 1.5 Vdc)  | "0" Level<br>V <sub>IL</sub> | 5.0                    | –   | 1.5    | –     | 2.25            | 1.5    | –     | 1.5    | Vdc      |
|   |                              | 10                     | –   | 3.0    | –     | 4.50            | 3.0    | –     | 3.0    |          |
|   |                              | 15                     | –   | 4.0    | –     | 6.75            | 4.0    | –     | 4.0    |          |
|   | "1" Level<br>V <sub>IH</sub> | 5.0                    | 3.5   | –      | 3.5   | 2.75            | –      | 3.5   | –      | Vdc      |
|   |                              | 10                     | 7.0   | –      | 7.0   | 5.50            | –      | 7.0   | –      |          |
|   |                              | 15                     | 11  | –      | 11    | 8.25            | –      | 11    | –      |          |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc)<br>(V <sub>OH</sub> = 4.6 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc)<br><br>(V <sub>OL</sub> = 0.4 Vdc)<br>(V <sub>OL</sub> = 0.5 Vdc)<br>(V <sub>OL</sub> = 1.5 Vdc)<br><br>(V <sub>OL</sub> = 0.4 Vdc)<br>(V <sub>OL</sub> = 0.5 Vdc)<br>(V <sub>OL</sub> = 1.5 Vdc) | Source                       | I <sub>OH</sub>        | 5.0   | – 1.2  | –     | – 1.0           | – 1.7  | –     | – 0.7  | mAd<br>c |
|   |                              |                        | 5.0   | – 0.25 | –     | – 0.2           | – 0.36 | –     | – 0.14 |          |
|   |                              |                        | 10  | – 0.62 | –     | – 0.5           | – 0.9  | –     | – 0.35 |          |
|   |                              |                        | 15  | – 1.8  | –     | – 1.5           | – 3.5  | –     | – 1.1  |          |
|   | Sink<br>Q Outputs            | I <sub>OL</sub>        | 5.0   | 1.28   | –     | 1.02            | 1.76   | –     | 0.72   | mAd<br>c |
|   |                              |                        | 10  | 3.2    | –     | 2.6             | 4.5    | –     | 1.8    |          |
|   |                              |                        | 15  | 8.4    | –     | 6.8             | 17.6   | –     | 4.8    |          |
|   | Sink<br>Pin 5, 11 only       | I <sub>OL</sub>        | 5.0   | 0.64   | –     | 0.51            | 0.88   | –     | 0.36   | mAd<br>c |
|   |                              |                        | 10  | 1.6    | –     | 1.3             | 2.25   | –     | 0.9    |          |
|   |                              |                        | 15  | 4.2    | –     | 3.4             | 8.8    | –     | 2.4    |          |
| Input Current   | I <sub>in</sub>              | 15                     | –   | ±0.1   | –     | ±0.00001        | ±0.1   | –     | ±1.0   | μAdc     |
| Input Capacitance   | C <sub>in</sub>              | –                      | –   | –      | –     | 5.0             | 7.5    | –     | –      | pF       |
| Quiescent Current<br>(Per Package)<br>(Clock = 0 V,<br>Other Inputs = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 μA)  | I <sub>DD</sub>              | 5.0                    | –   | 5.0    | –     | 0.005           | 5.0    | –     | 150    | μAdc     |
|   |                              | 10                     | –   | 10     | –     | 0.010           | 10     | –     | 300    |          |
|   |                              | 15                     | –   | 20     | –     | 0.015           | 20     | –     | 600    |          |
| Total Supply Current (Note 3, 4)<br>(Dynamic plus Quiescent,<br>Per Package) (C <sub>L</sub> = 50 pF on all<br>outputs, all buffers switching)  | I <sub>T</sub>               | 5.0<br>10<br>15        | I <sub>T</sub> = (0.8 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (1.6 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (2.4 μA/kHz) f + I <sub>DD</sub> |        |       |                 |        |       |        | μAdc     |

2. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level  
= 1.0 V min @ V<sub>DD</sub> = 5.0 V  
= 2.0 V min @ V<sub>DD</sub> = 10 V  
= 2.5 V min @ V<sub>DD</sub> = 15 V

3. To calculate total supply current at loads other than 50 pF: I<sub>T</sub>(C<sub>L</sub>) = I<sub>T</sub>(50 pF) + 3.5 × 10<sup>-3</sup> (C<sub>L</sub> = 50) V<sub>DD</sub>f where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V<sub>DD</sub> in V, and f in kHz is input frequency.

4. The formulas given are for the typical characteristics only at 25°C.

# MC14549B, MC14559B

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

| Characteristic   | Symbol             | $V_{DD}$  | Min   | Typ   | Max   | Unit          |
|--|--------------------|---|---|---|---|---------------|
| Output Rise Time<br>$t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$<br>$t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$<br>$t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$  | $t_{TLH}$          | 5.0<br>10<br>15   | —<br>—<br>—                                       | 180<br>90<br>65   | 360<br>180<br>130   | ns            |
| Output Fall Time<br>$t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$   | $t_{THL}$          | 5.0<br>10<br>15   | —<br>—<br>—                                       | 100<br>50<br>40   | 200<br>100<br>80  | ns            |
| Propagation Delay Time<br>Clock to Q<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 177 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$<br>Clock to $S_{out}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 665 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 277 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 195 \text{ ns}$<br>Clock to EOC<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ | $t_{PLH}, t_{PHL}$ | 5.0<br>10<br>15<br><br>5.0<br>10<br>15<br><br>5.0<br>10<br>15 | —<br>—<br>—<br><br>—<br>—<br>—<br><br>—<br>—<br>— | 500<br>210<br>155<br><br>750<br>310<br>220<br><br>300<br>130<br>100 | 1000<br>420<br>310<br><br>1500<br>620<br>440<br><br>600<br>260<br>200 | ns            |
| SC, D, FF or MR Setup Time   | $t_{su}$           | 5.0<br>10<br>15   | 250<br>100<br>80                                  | 125<br>50<br>40   | —<br>—<br>—   | ns            |
| Clock Pulse Width  | $t_{WH(cl)}$       | 5.0<br>10<br>15   | 700<br>270<br>200                                 | 350<br>135<br>100   | —<br>—<br>—   | ns            |
| Pulse Width — D, SC, FF or MR  | $t_{WH}$           | 5.0<br>10<br>15   | 500<br>200<br>160                                 | 250<br>100<br>80  | —<br>—<br>—   | ns            |
| Clock Rise and Fall Time   | $t_{TLH}, t_{THL}$ | 5.0<br>10<br>15   | —<br>—<br>—                                       | —<br>—<br>—   | 15<br>1.0<br>0.5  | $\mu\text{s}$ |
| Clock Pulse Frequency  | $f_{cl}$           | 5.0<br>10<br>15   | —<br>—<br>—                                       | 1.5<br>3.0<br>4.0   | 0.8<br>1.5<br>2.0   | MHz           |

5. The formulas given are for the typical characteristics only.

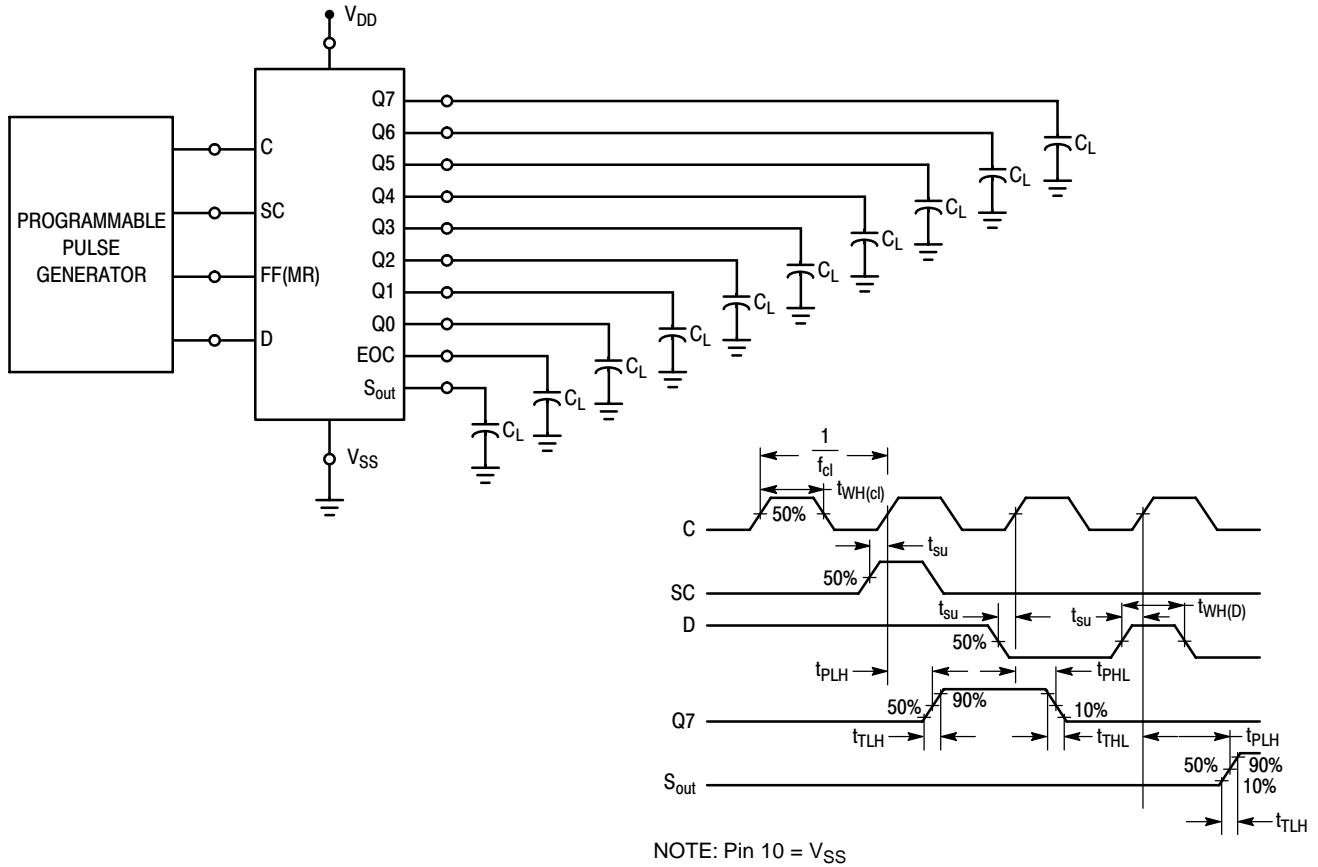
## ORDERING INFORMATION

| Device        | Package              | Shipping†          |
|---------------|----------------------|--------------------|
| MC14549BCP    | PDIP–16              | 25 / Rail          |
| MC14549BCPG   | PDIP–16<br>(Pb–Free) |                    |
| MC14549BDWR2  | SOIC–16              | 1000 / Tape & Reel |
| MC14549BDWR2G | SOIC–16<br>(Pb–Free) |                    |
| MC14559BCP    | PDIP–16              | 25 / Rail          |
| MC14559BCPG   | PDIP–16<br>(Pb–Free) |                    |
| MC14559BDWR2  | SOIC–16              | 1000 / Tape & Reel |
| MC14559BDWR2G | SOIC–16<br>(Pb–Free) |                    |

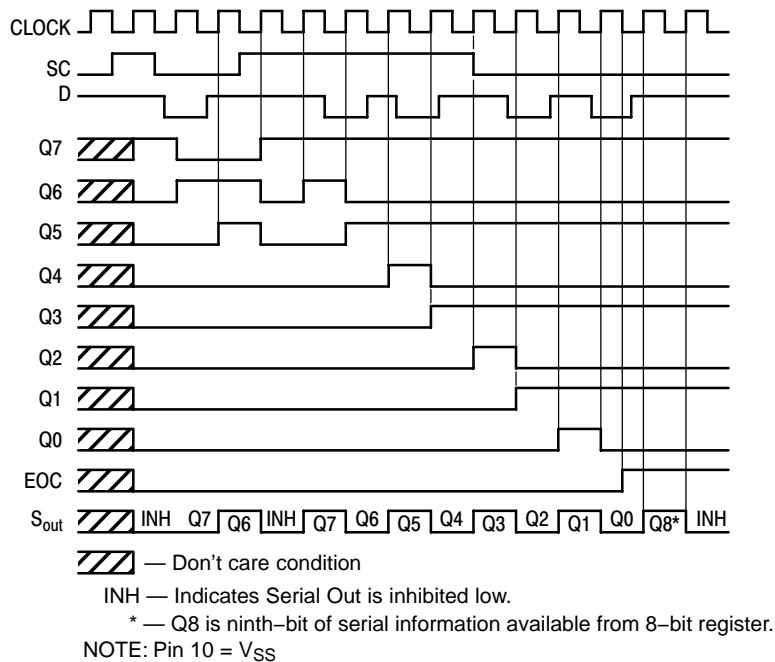
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC14549B, MC14559B

## SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



## TIMING DIAGRAM



## OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the “free run” or “strobed operation” mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with  $EOC = 0$  (and with  $SC = 1$  for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after  $EOC = 1$  during externally strobed operation, provided  $SC = 1$ .

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

**C = Clock** — A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

**SC = Start Convert** — A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

**D = Data in** — Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

**MR = Master Reset (MC14549B Only)** — Resets all output to 0 on positive-going transitions of the clock. If removed while  $SC = 0$ , the circuit will remain reset until  $SC = 1$ . This allows easy cascading of circuits.

**FF = Feed Forward (MC14559B Only)** — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit

conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded.

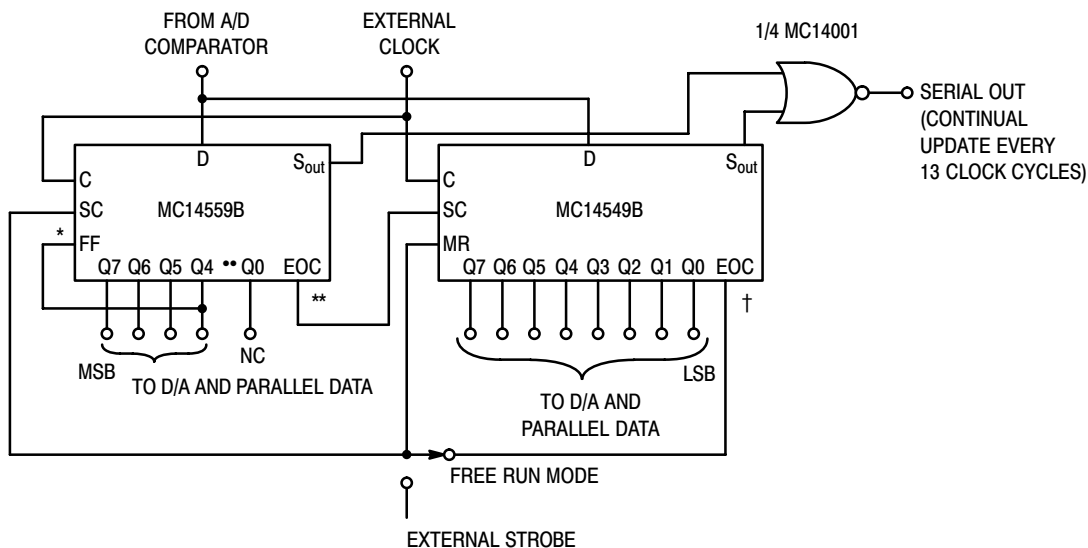
For 8-bit operation, FF is tied to  $V_{SS}$ .

For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out ( $S_{out}$ ) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while  $S_{out}$  of the MC14549B remains inhibited until the second clock cycle of its operation.

**$Q_n$  = Data Outputs** — After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

**EOC = End of Convert** — This output goes high on the negative-going transition of the clock following  $FF = 1$  (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

**$S_{out}$  = Serial Out** — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.



\* FF allows EOC to activate as if in 4-stage register.

\*\* Cascading using EOC guaranteed; no stable unfunctional state.

† Completion of conversion automatically re-initiates cycle in free run mode.

Figure 1. 12-Bit Conversion Scheme

## TYPICAL APPLICATIONS

**Externally Controlled 6–Bit ADC (Figure 2)**

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

**Continuously Cycling 8–Bit ADC (Figure 3)**

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

**Continuously Cycling 12–Bit ADC (Figure 4)**

Because each successive approximation register (SAR) has a capability of handling only an eight–bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch–on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non–functional condition.

This 12–bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of the 12–bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

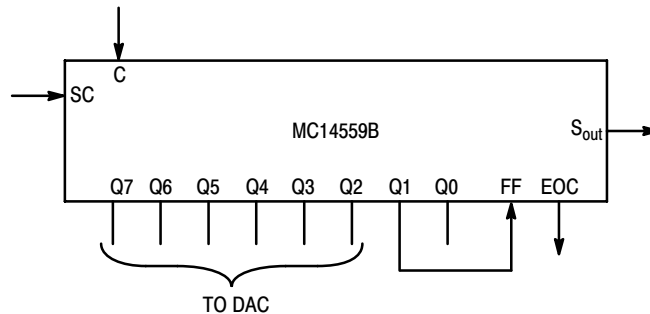


Figure 2. Externally Controlled 6–Bit ADC

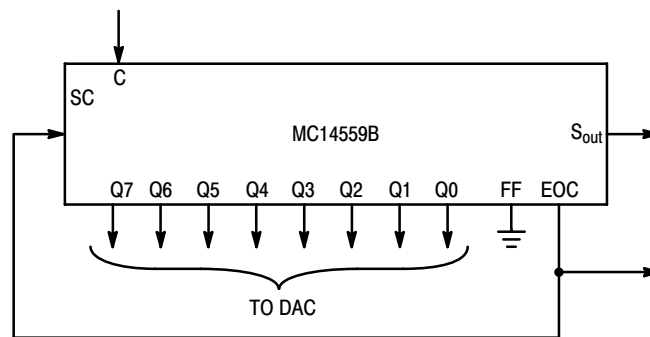


Figure 3. Continuously Cycling 8–Bit ADC

## MC14549B, MC14559B

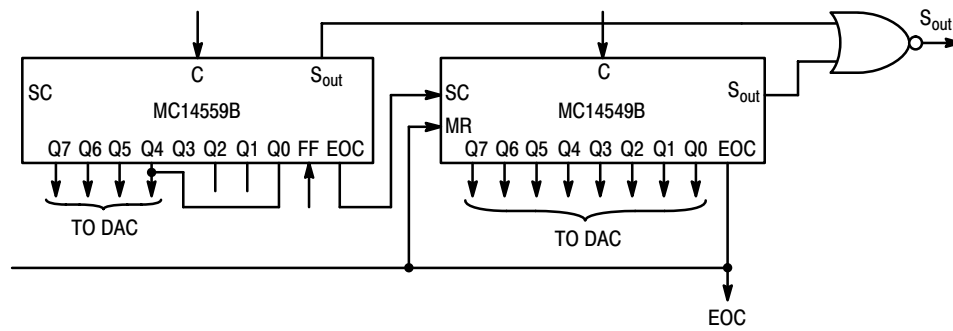


Figure 4. Continuously Cycling 12-Bit ADC

### Externally Controlled 12-Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

### Additional Motorola Parts for Successive Approximation ADC

**Monolithic digital-to-analog converters** — The MC1408/1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. **The amplifier-comparator block** — The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.

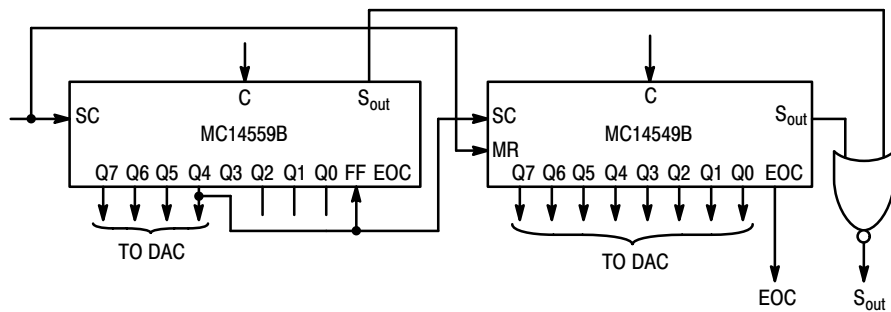
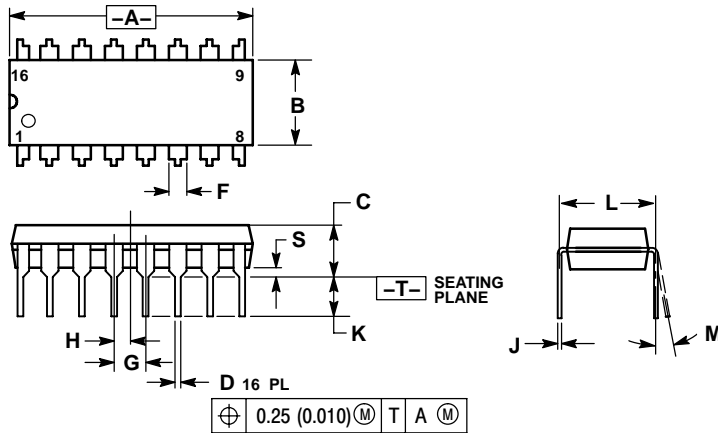


Figure 5. Externally Controlled 12-Bit ADC

# MC14549B, MC14559B

## PACKAGE DIMENSIONS

### PDIP-16 CASE 648-08 ISSUE T

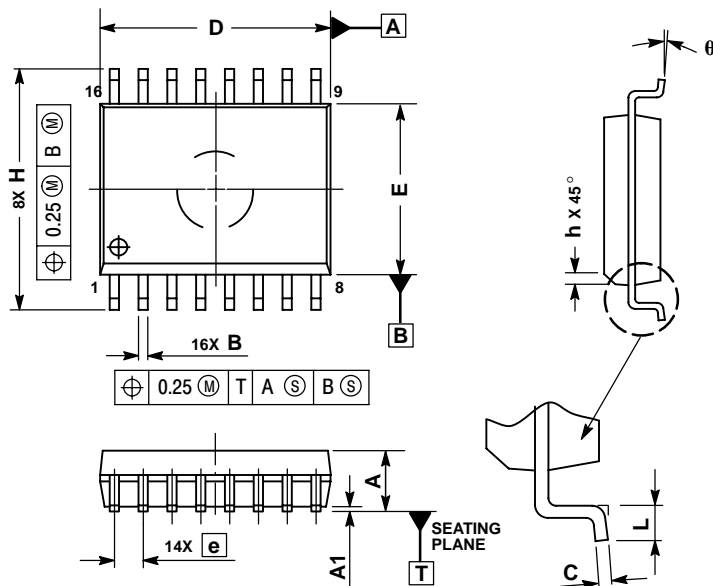


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

### SO-16 WB CASE 751G-03 ISSUE C




#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 10.15       | 10.45 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| q   | 0°          | 7°    |

## MC14549B, MC14559B

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