

MC10ELT20, MC100ELT20

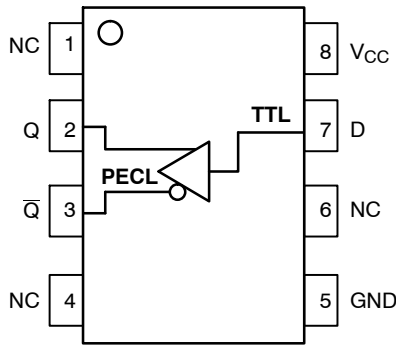


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q, $\bar{Q}$	PECL Differential Outputs*
D	TTL Input
V _{CC}	Positive Supply
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

*Output state undetermined when inputs are open.

Table 2. ATTRIBUTES

Characteristics	Value	
Internal Input Pulldown Resistor	N/A	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
SO-8 TSSOP-8 DFN8	Level 1 Level 1 Level 1	Level 1 Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	51 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		7	V
V _{IN}	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	7	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SO-8 SO-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SO-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T _{sol}	Wave Solder	Pb Pb-Free	< 3 s @ 248°C < 3 s @ 260°C	265 265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

MC10ELT20, MC100ELT20

Table 4. 10ELT SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $GND = 0.0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			16			16			16	mA
V_{OH}	Output HIGH Voltage (Note 4)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 4)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25\text{ V}$.

4. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2\text{ V}$.

Table 5. 100ELT SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $GND = 0.0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			16			16			16	mA
V_{OH}	Output HIGH Voltage (Note 6)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 6)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25\text{ V}$.

6. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2\text{ V}$.

Table 6. TTL INPUT DC CHARACTERISTICS $V_{CC} = 4.7\text{ V}$ to 5.27 V ; $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	μA
I_{IHH}	Input HIGH Current	$V_{IN} = 7.0\text{ V}$			100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	mA
V_{IK}	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

MC10ELT20, MC100ELT20

Table 7. AC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $GND = 0.0 \text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency	100			100			100			MHz
t_{PLH}	Propagation Delay 1.5 V to 50%	0.6	0.82	1.2	0.6	0.82	1.25	0.6	0.83	1.35	ns
t_{PHL}	Propagation Delay 1.5 V to 50%	0.4		1.0	0.5	0.8	1.1	0.7		1.30	ns
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r/t_f	Output Rise/Fall Time (20–80%)	0.15		1.5	0.15		1.5	0.15		1.5	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

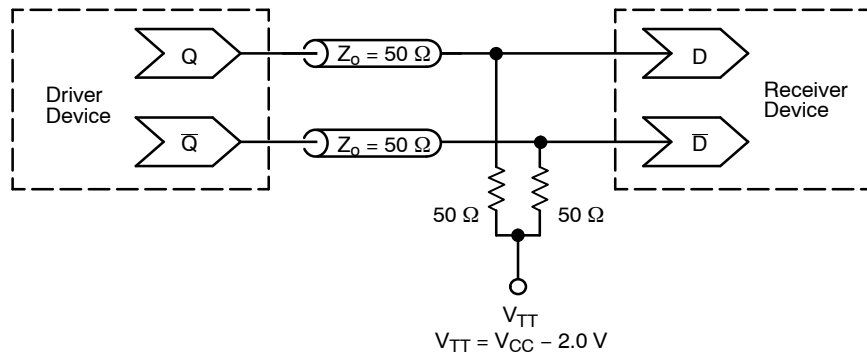


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

MC10ELT20, MC100ELT20

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10ELT20D	SO-8	98 Units / Rail
MC10ELT20DG	SO-8 (Pb-Free)	98 Units / Rail
MC10ELT20DR2	SO-8	2500 / Tape & Reel
MC10ELT20DR2G	SO-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT20DT	TSSOP-8	100 Units / Rail
MC10ELT20DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT20DTR2	TSSOP-8	2500 / Tape & Reel
MC10ELT20DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT20MNR4	DFN8	1000 / Tape & Reel
MC10ELT20MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100ELT20D	SO-8	98 Units / Rail
MC100ELT20DG	SO-8 (Pb-Free)	98 Units / Rail
MC100ELT20DR2	SO-8	2500 / Tape & Reel
MC100ELT20DR2G	SO-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT20DT	TSSOP-8	100 Units / Rail
MC100ELT20DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT20DTR2	TSSOP-8	2500 / Tape & Reel
MC100ELT20DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT20MNR4	DFN8	1000 / Tape & Reel
MC100ELT20MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

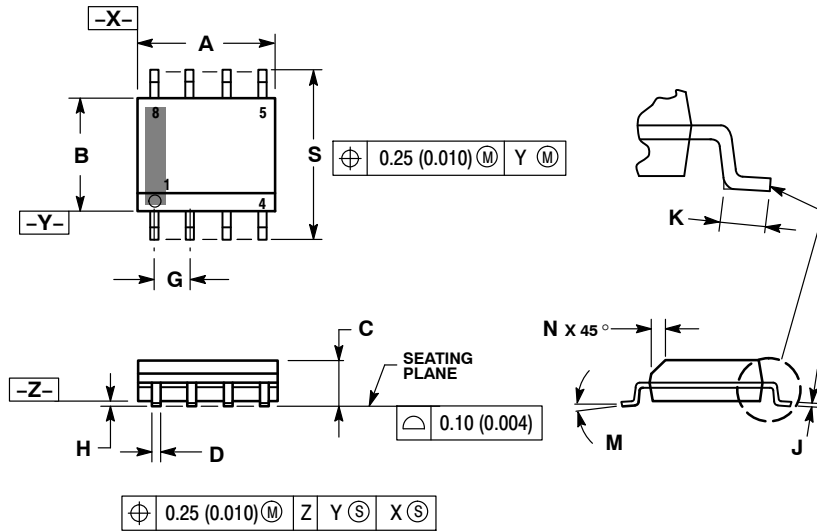
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10ELT20, MC100ELT20

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AH

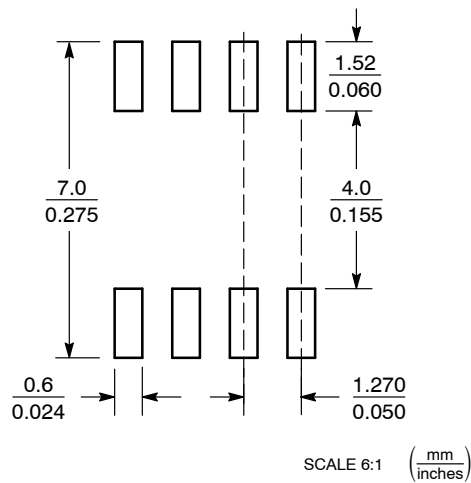


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

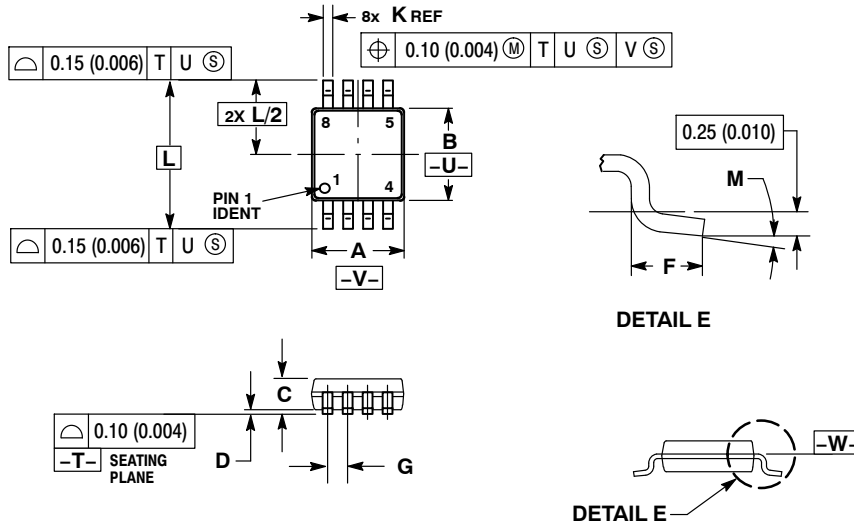


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC10ELT20, MC100ELT20

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948R-02
 ISSUE A



NOTES:

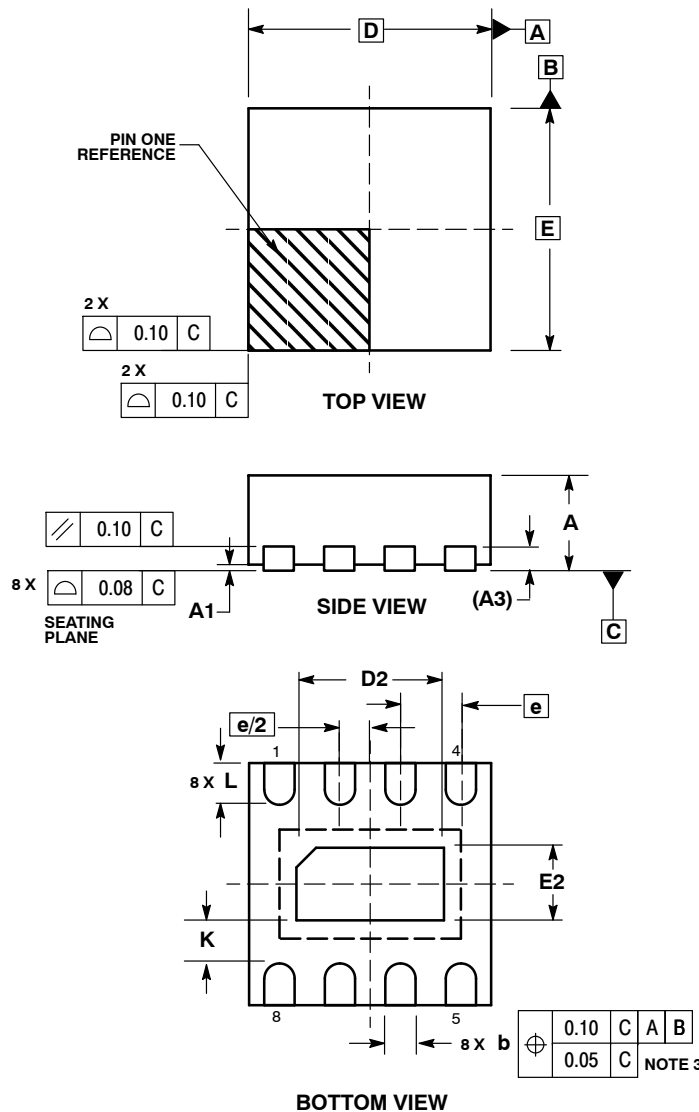
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

MC10ELT20, MC100ELT20

PACKAGE DIMENSIONS

DFN8
CASE 506AA-01
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.20	---
L	0.25	0.35

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MC10ELT20/D