ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
V_{CC} .....-0.3V to +6.0V
Open-Drain $\overline{RESET}$, $\overline{MR}$ .....-0.3V to +6.0V
RESET-IN, Push-Pull $\overline{RESET}$
and RESET .....-0.3V to (V_{CC} + 0.3V)
Input/Output Current (all pins) 20mA

Continous Power Dissipation (T_A = +70°C)
3-Pin SC70 (derate 2.9mW/°C above +70°C).....235mW
4-Pin SC70 (derate 3.1mW/°C above +70°C).....245mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +0.55V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	T_A = -40°C to +85°C MAX6832/MAX6835/MAX6838 MAX6834/MAX6837/MAX6840	0.55		3.6	V
		T_A = -40°C to +85°C MAX6833/MAX6836/MAX6839	0.85		3.6	
		T_A = 0°C to +85°C MAX6833/MAX6836/MAX6839	0.75		3.6	
Supply Current	I_{CC}	V_{CC} = 1.2V, no load, reset not asserted		7.5	13	µA
		V_{CC} = 1.8V, no load, reset not asserted		9	16	
		V_{CC} = 3.6V, no load, reset not asserted		16	25	
Reset Threshold	V_{TH}	W	1.620	1.665	1.710	V
		V	1.530	1.575	1.620	
		I	1.350	1.388	1.425	
		H	1.275	1.313	1.350	
		G	1.080	1.110	1.140	
		F (Note 2)	1.020	1.050	1.080	
RESET-IN Threshold	V_{RSTIN}	1.1V ≤ V_{CC} ≤ 3.3V, 0°C to +85°C	-2.5%	444	+2.5%	mV
		1.1V ≤ V_{CC} ≤ 3.3V, -40°C to +85°C	-3.0%	444	+3.0%	
RESET-IN Leakage Current	I_{RSTIN}		-25		+25	nA
Reset Threshold Hysteresis	V_{HYS}			0.75		%V_{TH}
V_{CC} or RESET-IN to Reset Delay		V_{CC} falling, step signal from (V_{TH} + 100mV) to (V_{TH} - 100mV)		60		µs
Reset Active Timeout Period	t_{RP}	D0		0.07		ms
		D1	1	1.5	2	
		D2	20	30	40	
		D3	140	210	280	
		D4	1120	1680	2240	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +0.55V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

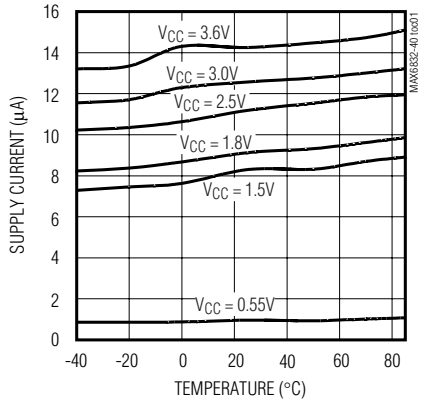
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay (D0 only)	t_P	V_{CC} rising, step signal from (V_{TH} - 100mV) to (V_{TH} + 100mV)		70		µs
Startup Time (D0 only)		V_{CC} rising from 0 to 1.1V (t_R < 1µs)		150		µs
$\overline{MR}$ Input Voltage	V_{IL}				0.3 x V_{CC}	V
	V_{IH}		0.7 x V_{CC}			
$\overline{MR}$ Minimum Input Pulse Width		$\overline{MR}$ driven from V_{CC} to 0	2			µs
$\overline{MR}$ Glitch Rejection		$\overline{MR}$ driven from V_{CC} to 0		100		ns
$\overline{MR}$ to Reset Delay		$\overline{MR}$ driven from V_{CC} to 0		500		ns
$\overline{MR}$ Pullup Resistance To V_{CC}			14	20	26	kΩ
Open-Drain $\overline{RESET}$ Output Voltage	V_{OL}	V_{CC} ≥ 0.55V, I_{SINK} =15µA, reset asserted			0.15	V
		V_{CC} ≥ 1.0V, I_{SINK} = 80µA, reset asserted			0.15	
		V_{CC} ≥ 1.5V, I_{SINK} = 200µA, reset asserted			0.2	
Open-Drain $\overline{RESET}$ Output Leakage Current	I_{LKG}	V_{CC} > V_{TH}, reset not asserted			1.0	µA
Push-Pull $\overline{RESET}$ Output Voltage	V_{OL}	V_{CC} ≥ 0.55V, I_{SINK} = 15µA, reset asserted			0.2 x V_{CC}	V
		V_{CC} ≥ 1.0V, I_{SINK} = 80µA, reset asserted			0.2 x V_{CC}	
		V_{CC} ≥ 1.5V, I_{SINK} = 200µA, reset asserted			0.2 x V_{CC}	
	V_{OH}	V_{CC} ≥ 1.1V, I_{SOURCE} = 50µA, reset not asserted	0.8 x V_{CC}			
		V_{CC} ≥ 1.5V, I_{SOURCE} = 150µA, reset asserted	0.8 x V_{CC}			
Push-Pull RESET Output Voltage	V_{OH}	V_{CC} ≥ 0.75V, I_{SOURCE} = 10µA, reset asserted (Note 2)	0.8 x V_{CC}			V
		V_{CC} ≥ 0.85V, I_{SOURCE} = 10µA, reset asserted	0.8 x V_{CC}			
		V_{CC} ≥ 1.0V, I_{SOURCE} = 50µA, reset asserted	0.8 x V_{CC}			
		V_{CC} ≥ 1.5V, I_{SOURCE} = 150µA, reset asserted	0.8 x V_{CC}			
	V_{OL}	V_{CC} ≥ 1.1V, I_{SINK} = 80µA, reset not asserted			0.2 x V_{CC}	
		V_{CC} ≥ 1.5V, I_{SINK} = 200µA, reset not asserted			0.2 x V_{CC}	

Note 1: 100% production tested at +25°C. Over temperature limits are guaranteed by design.
Note 2: Temperature range is from 0°C to +85°C.

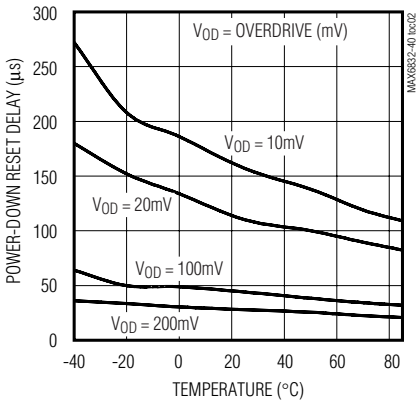
Typical Operating Characteristics

(V_{CC} = full range and T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C).

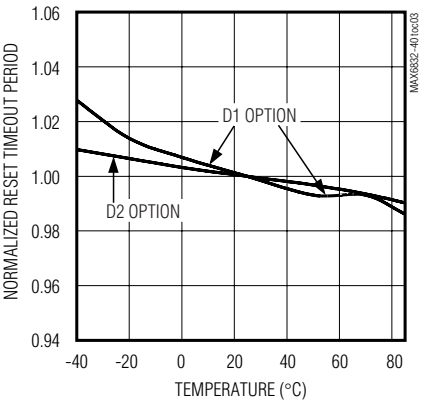
SUPPLY CURRENT vs. TEMPERATURE



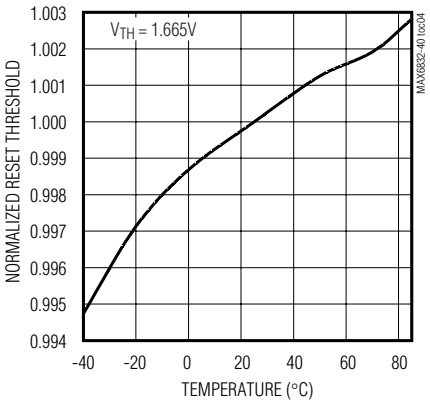
POWER-DOWN RESET DELAY vs. TEMPERATURE



NORMALIZED POWER-UP RESET TIMEOUT vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



Ultra-Low-Voltage SC70 Voltage Detectors and µP Reset Circuits

Pin Description—MAX6832–MAX6837

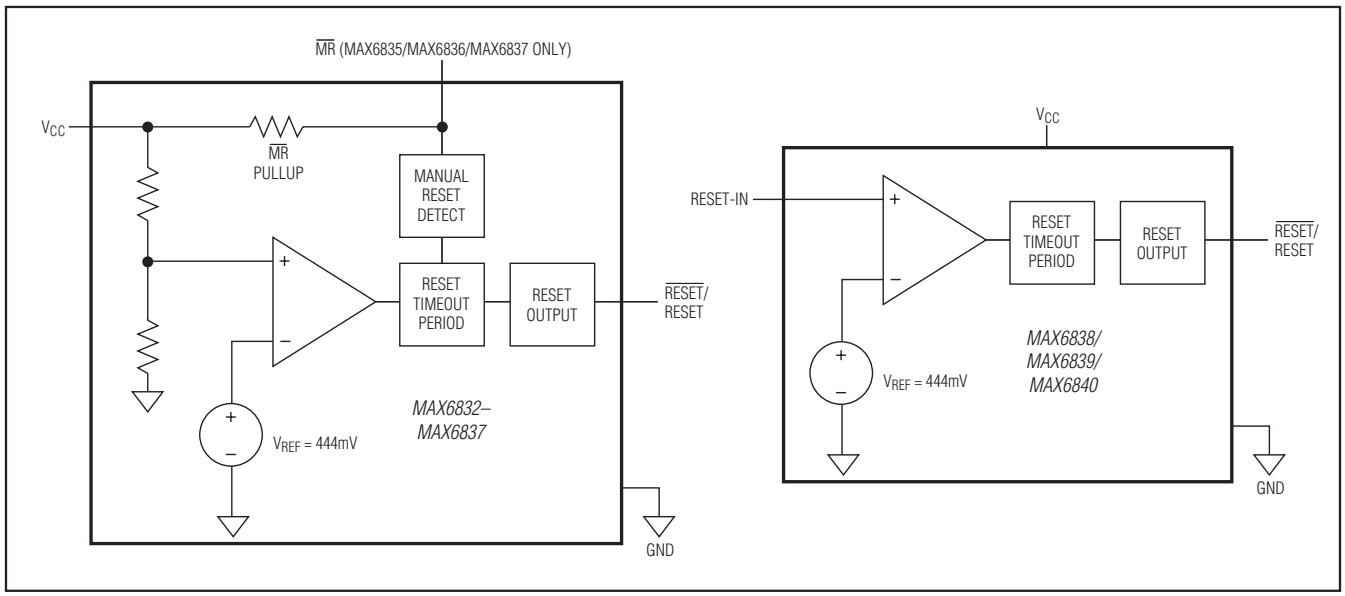
PIN				NAME	FUNCTION
MAX6833 SC70-3	MAX6832/ MAX6834 SC70-3	MAX6836 SC70-4	MAX6835/ MAX6837 SC70-4		
1	1	1	1	GND	Ground
—	2	—	2	$\overline{\text{RESET}}$	Reset Output, Open-Drain or Push-Pull, Active-Low. $\overline{\text{RESET}}$ changes from HIGH to LOW when V_{CC} drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. $\overline{\text{RESET}}$ remains LOW for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ is released high.
2	—	2	—	RESET	Reset Output, Push-Pull, Active-High. RESET changes from LOW to HIGH when the V_{CC} input drops below the selected reset threshold or $\overline{\text{MR}}$ is pulled low. RESET remains HIGH for the reset timeout period after V_{CC} exceeds the device reset threshold and $\overline{\text{MR}}$ is released high.
—	—	3	3	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Internal 20kΩ pullup to V_{CC}. Pull LOW to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is LOW and for the reset timeout period after $\overline{\text{MR}}$ goes HIGH. Leave unconnected or connect to V_{CC} if unused.
3	3	4	4	V_{CC}	Supply Voltage and Monitored Supply

Pin Description—MAX6838/MAX6839/MAX6840

PIN		NAME	FUNCTION
MAX6839 SC70-4	MAX6838/ MAX6840 SC70-4		
1	1	RESET-IN	Adjustable Reset Threshold Input. High-impedance input for reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; the typical threshold is 444mV. Reset is asserted when RESET-IN is below the threshold (V_{CC} is not monitored).
2	2	V_{CC}	Supply Voltage (1.1V to 3.3V)
3	3	GND	Ground
4	—	RESET	Reset Output, Push-Pull, Active-High. RESET changes from LOW to HIGH when the RESET-IN input drops below the typical reset threshold (444mV). RESET remains HIGH for the reset timeout period after RESET-IN exceeds the reset threshold.
—	4	$\overline{\text{RESET}}$	Reset Output, Open-Drain or Push-Pull, Active-Low. $\overline{\text{RESET}}$ changes from HIGH to LOW when RESET-IN drops below the typical reset threshold (444mV). $\overline{\text{RESET}}$ remains LOW for the reset timeout period after RESET-IN exceeds the reset threshold.

Ultra-Low-Voltage SC70 Voltage Detectors and µP Reset Circuits

Functional Diagrams



Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. The MAX6832–MAX6840 assert a reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They also assert a reset signal whenever the V_{CC} supply voltage falls below a preset threshold (MAX6832–MAX6837) or RESET-IN falls below the adjustable threshold (MAX6838/MAX6839/MAX6840), keeping reset asserted for a fixed timeout delay (Table 2) after V_{CC} or RESET-IN has risen above the reset threshold. The MAX6832/MAX6835/MAX6838 use a push-pull active-low output, the MAX6833/MAX6836/MAX6839 have a push-pull active-high output, and the MAX6834/MAX6837/MAX6840 have an open-drain active-low output stage. Connect a pullup resistor on the MAX6834/MAX6837/MAX6840's $\overline{RESET}$ output to any supply between 0 and 6V.

Manual Reset Input

Many µP-based systems require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. Reset remains asserted while $\overline{MR}$ is low, and for a fixed timeout delay after $\overline{MR}$ returns high. This input has an internal 20kΩ pullup resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with CMOS logic level, or with open-drain/collector outputs. To create a manual reset function, connect a normally open momentary switch from $\overline{MR}$ to ground; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

RESET-IN Information

The MAX6838/MAX6839/MAX6840 feature a RESET-IN input for monitoring supply voltages down to 0.44V. An external resistive-divider network can be used to set voltage monitoring thresholds as shown in Figure 1. As the monitored voltage falls, the voltage at RESET-IN decreases and asserts a reset when it falls below the RESET-IN threshold (V_{RSTIN}). The low-leakage current

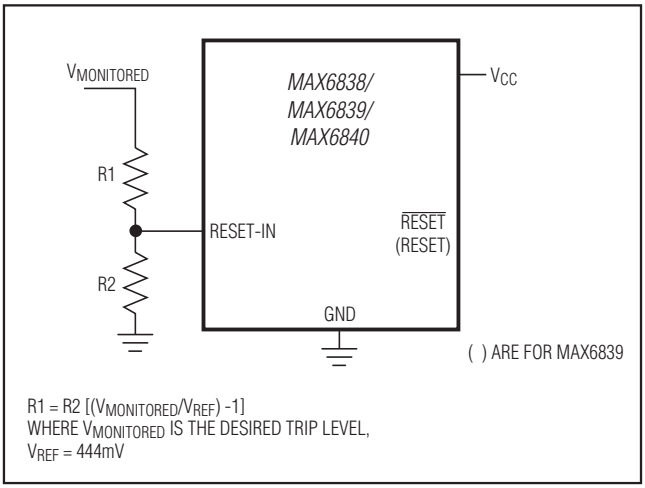


Figure 1. Setting the Adjustable Threshold Externally

at RESET-IN allows for relatively large-value resistors to be used, which reduce power consumption. For example, for a 0.6V monitored trip level, if R2 = 200kΩ, then R1 = 70.3kΩ. Note that the minimum V_{CC} of 1.1V is required to guarantee the RESET-IN threshold accuracy (see *Electrical Characteristics* table).

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the MAX6832–MAX6840 are relatively immune to short-duration negative-going V_{CC} transients (glitches).

Figure 2 shows typical transient duration vs. reset comparator overdrive, for which the MAX6832–MAX6840 do **not** generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC}, starting 0.1V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 0.55V, the MAX6832/MAX6835/MAX6838 push-pull $\overline{RESET}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications since most µP and other circuitry are inoperative with V_{CC} lower than 0.55V. However, in applications where $\overline{RESET}$ must be valid down to 0, adding a pulldown resistor to $\overline{RESET}$ causes any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 3). R3's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground.

A 100kΩ pullup resistor to V_{CC} is also recommended for the MAX6833/MAX6836/MAX6839 if RESET is required to remain valid for V_{CC} < 0.85V.

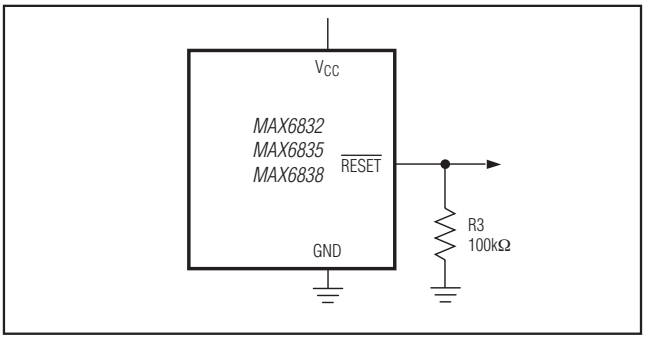


Figure 3. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

Interfacing to µPs with Bidirectional Reset Pins

Since the $\overline{RESET}$ output on the MAX6834/MAX6837/MAX6840 is open-drain, these devices interface easily with µPs that have bidirectional reset pins. Connecting the µP supervisor's $\overline{RESET}$ output directly to the µP's $\overline{RESET}$ pin with a single pullup resistor allows either device to assert a reset (Figure 4).

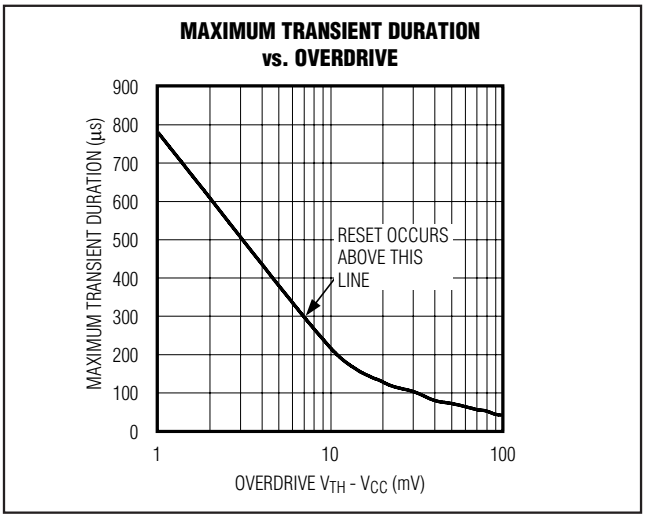


Figure 2. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

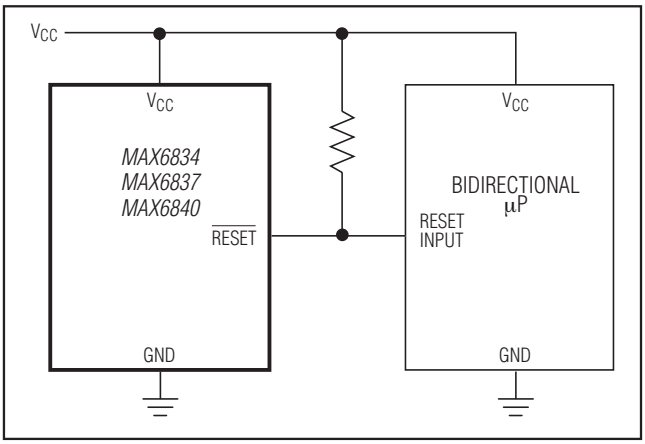


Figure 4. Interfacing to µPs with Bidirectional Reset I/O

Ultra-Low-Voltage SC70 Voltage Detectors and µP Reset Circuits

Using The MAX6834/MAX6837/MAX6840 Open-Drain RESET Output with Multiple Supplies

Generally, the pullup connected to the MAX6834/MAX6837/MAX6840 will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 5). Note that as the MAX6834/MAX6837/MAX6840's V_{CC} decreases, so does the IC's ability to sink current at $\overline{RESET}$. Also, with any pullup, $\overline{RESET}$ will be pulled high as V_{CC} declines toward 0. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

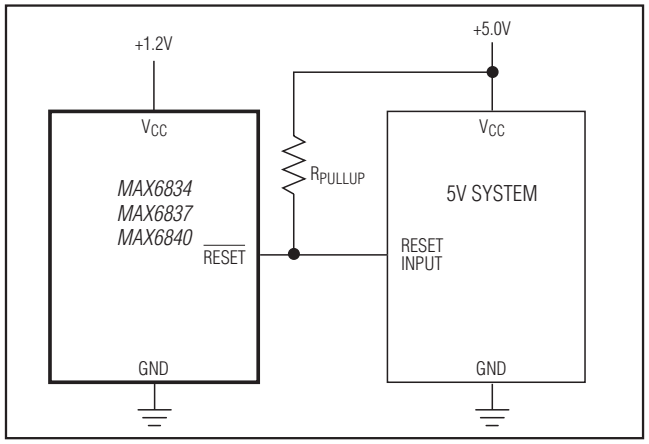


Figure 5. Using The MAX6834/MAX6837/MAX6840 Open-Drain RESET Output with Multiple Supplies

Chip Information

TRANSISTOR COUNT: 681

PROCESS: BiCMOS

Selector Guide

Table 1. Threshold Suffix Guide

SUFFIX	RESET THRESHOLD (V)
W	1.665
V	1.575
I	1.388
H	1.313
G	1.110
F	1.050

Table 2. Active Timeout Period Guide

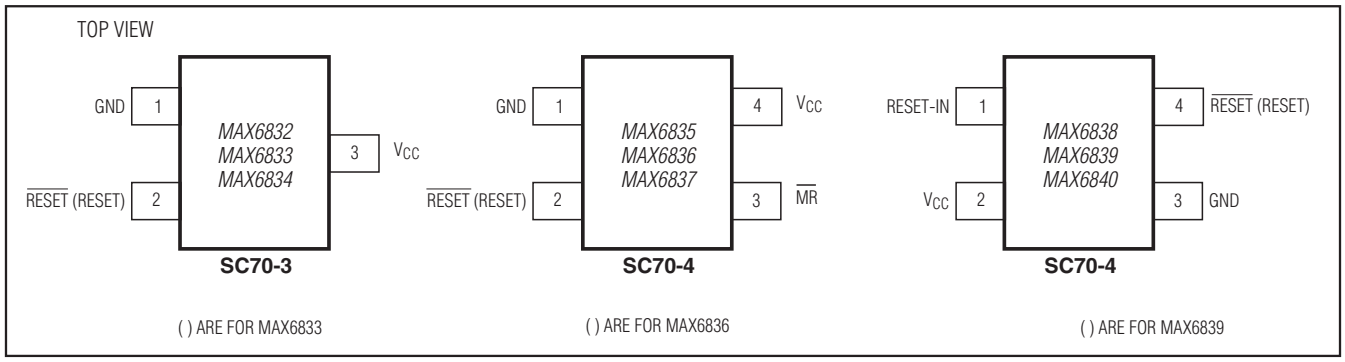
SUFFIX	TYPICAL RESET ACTIVE TIMEOUT PERIOD (ms)
D0	0.07
D1	1.5
D2	30
D3	210
D4	1680

Table 3. Standard Versions

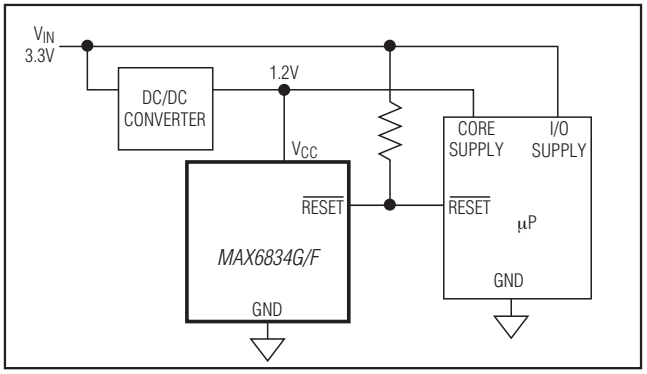
DEVICE	TOP MARK
MAX6832VXRD0	AIQ
MAX6832VXRD3	AIR
MAX6832HXRD0	AIS
MAX6832HXRD3	AIT
MAX6832FXRD0	AIU
MAX6832FXRD3	AIV
MAX6833VXRD0	AHJ
MAX6833VXRD3	AIW
MAX6833HXRD0	AIX
MAX6833HXRD3	AIY
MAX6833FXRD0	AIZ
MAX6833FXRD3	AJA
MAX6834VXRD0	AJB
MAX6834VXRD3	AJC
MAX6834HXRD0	AJD
MAX6834HXRD3	AJE
MAX6834FXRD0	AJF
MAX6834FXRD3	AJG
MAX6835VXSD0	AEX

Ultra-Low-Voltage SC70 Voltage Detectors and µP Reset Circuits

Pin Configurations



Typical Operating Circuit



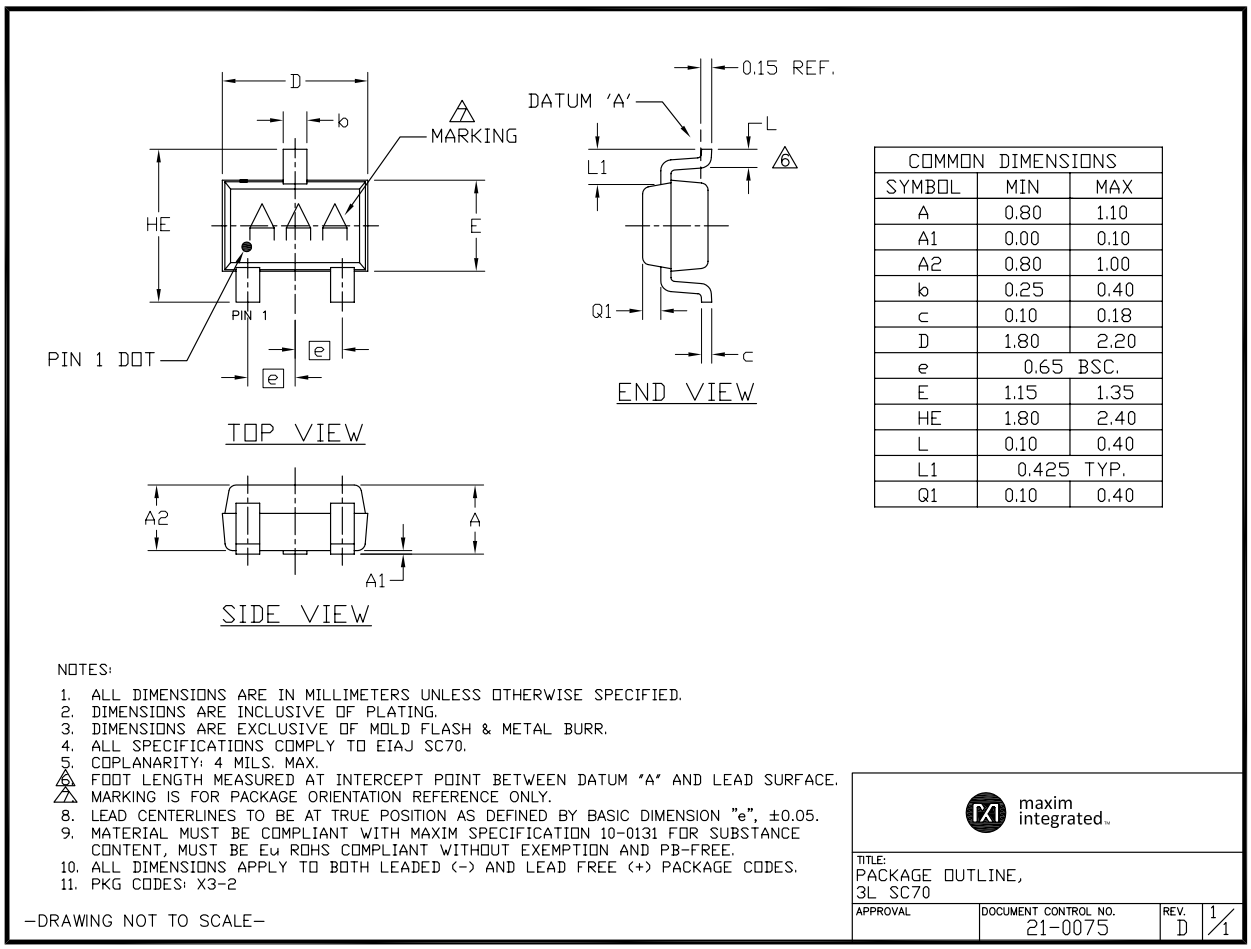
Selector Guide (continued)

Table 3. Standard Versions (continued)

DEVICE	TOP MARK
MAX6835VXSD3	AFF
MAX6835HXSD0	AFG
MAX6835HXSD3	AFH
MAX6835FXSD0	AFI
MAX6835FXSD3	AFJ
MAX6836VXSD0	AFK
MAX6836VXSD3	AFL
MAX6836HXSD0	AFM
MAX6836HXSD3	AFN
MAX6836FXSD0	AFO
MAX6836FXSD3	AFP
MAX6837VXSD0	AFQ
MAX6837VXSD3	AFR
MAX6837HXSD0	AFS
MAX6837HXSD3	AFT
MAX6837FXSD0	AFU
MAX6837FXSD3	AFC
MAX6838XSD0	AFW
MAX6838XSD3	AFV
MAX6839XSD0	AFX
MAX6839XSD3	AEZ
MAX6840XSD0	AFY
MAX6840XSD3	AFZ

Package Information

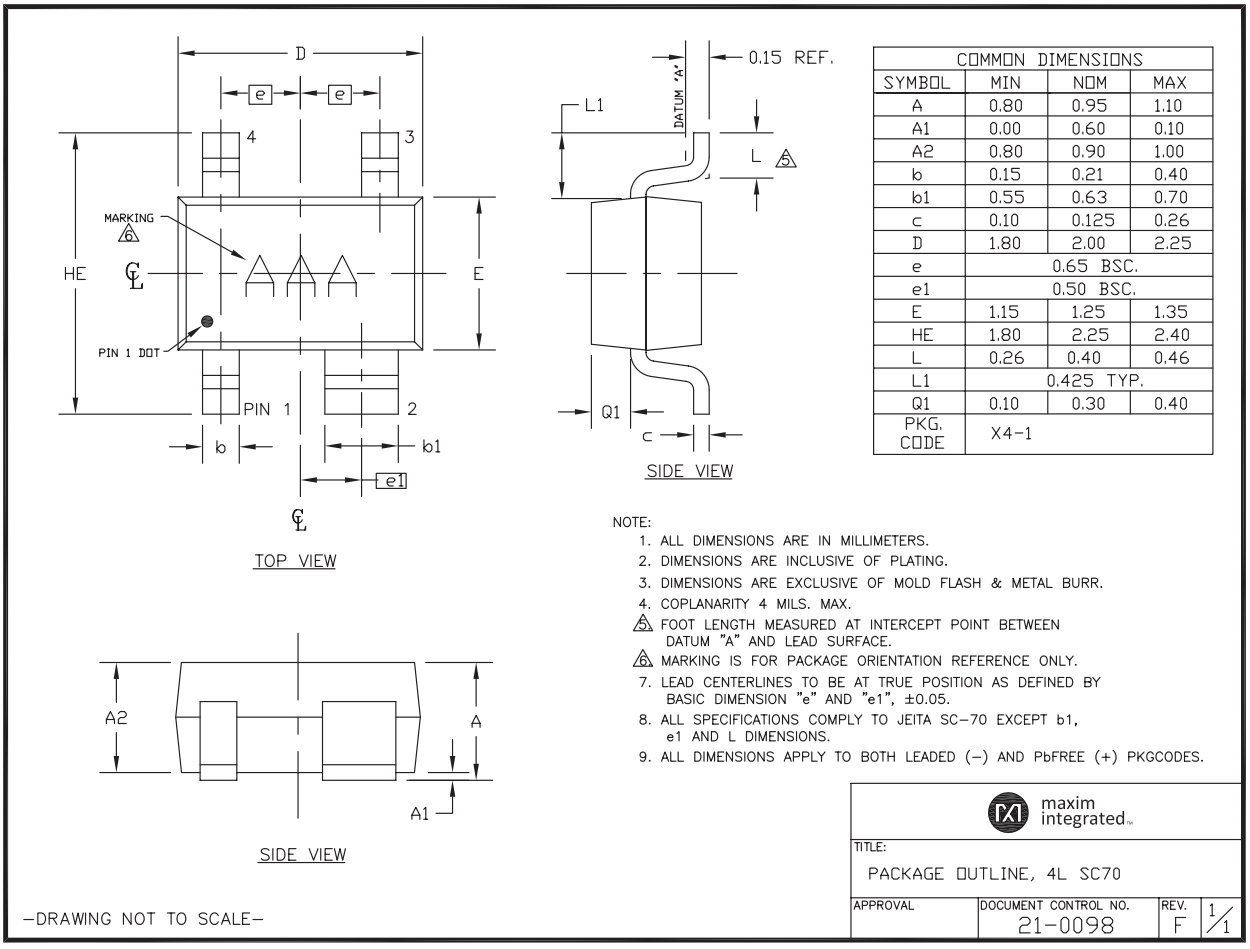
For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.25	0.40
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.40
L1	0.425 TYP.	
Q1	0.10	0.40

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.60	0.10
A2	0.80	0.90	1.00
b	0.15	0.21	0.40
b1	0.55	0.63	0.70
c	0.10	0.125	0.26
D	1.80	2.00	2.25
e	0.65 BSC.		
e1	0.50 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.25	2.40
L	0.26	0.40	0.46
L1	0.425 TYP.		
Q1	0.10	0.30	0.40
PKG. CODE	X4-1		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e" AND "e1", ±0.05.
8. ALL SPECIFICATIONS COMPLY TO JEITA SC-70 EXCEPT b1, e1 AND L DIMENSIONS.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKGCODES.

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