0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+, IN_ .....-0.3V to +4V
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current (COM_, NO_, NC_).....±100mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms 10% duty cycle).....±200mA
Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 9.1W/°C above +70°C) 727mW
16-Pin QFN (derate 16.9W/°C above +70°C) 1349mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, $V_{IH\_}$ = +1.4V, $V_{IL\_}$ = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance (Note 4)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.6	0.9	Ω
			T_{MIN} to T_{MAX}			1	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.03	0.12	Ω
			T_{MIN} to T_{MAX}			0.15	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = 100mA, $V_{NO\_}$ or $V_{NC\_}$ = 1V, 1.5V, 2V	+25°C		0.04	0.1	Ω
			T_{MIN} to T_{MAX}			0.12	
NO_ or NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	
COM_ Off-Leakage Current (Note 7)	$I_{COM\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 3.6V, 0.3V	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.6V, $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.6V, or floating	+25°C	-2.5	0.002	+2.5	nA
			T_{MIN} to T_{MAX}	-5		+5	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, $V_{IH\_}$ = +1.4V, $V_{IL\_}$ = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1		+25°C		6	30	ns
				T_{MIN} to T_{MAX}			30	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1		+25°C		10	25	ns
				T_{MIN} to T_{MAX}			25	
Break-Before-Make (Note 8) (MAX4753 Only)	t_{BBM}	$V_{NO\_}$ and $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF, Figure 1		+25°C		7		ns
				T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 2		+25°C		21		pC
NO_ or NC_ Off-Capacitance	C_{OFF}	f = 1MHz, Figure 3		+25°C		31		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	f = 1MHz, Figure 3		+25°C		30		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, Figure 3		+25°C		75		pF
Off-Isolation (Note 9)	V_{ISO}	R_L = 50Ω, C_L = 5pF, Figure 4	f = 10MHz	+25°C		-51		dB
			f = 1MHz	+25°C		-65		
Crosstalk		R_L = 50Ω, C_L = 5pF, Figure 4	f = 10MHz	+25°C		-70		dB
			f = 1MHz	+25°C		-80		
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $V_{COM\_}$ = $2V_{P-P}$, R_L = 32Ω		+25°C		0.031		%
DIGITAL I/O								
Input Logic High	$V_{IH\_}$			T_{MIN} to T_{MAX}	1.4			V
Input Logic Low	$V_{IL\_}$			T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or V+		T_{MIN} to T_{MAX}	-1	0.0005	+1	µA
POWER SUPPLY								
Power-Supply Range	V+				+1.6		+3.6	V
Positive Supply Current	I+	V+ = 3.6V, $V_{IN\_}$ = 0 or V+					1	µA

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +1.8V Supply

(V+ = +1.8V, V_{IH} = +1V, V_{IL} = +0.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

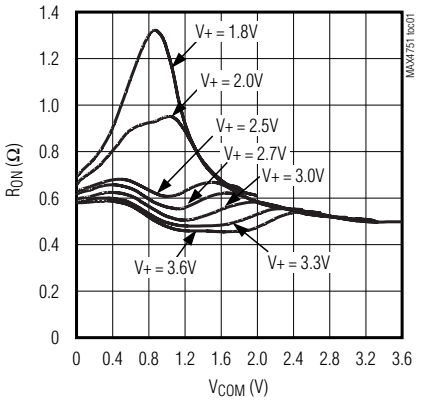
PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance (Note 4)	R_{ON}	V+ = 1.8V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0.9V	+25°C		1.4	2.5	Ω
			T_{MIN} to T_{MAX}			3	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 1.8V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0.9V	+25°C		0.05	0.25	Ω
			T_{MIN} to T_{MAX}			0.25	
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.0V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		25	35	ns
			T_{MIN} to T_{MAX}			35	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1.0V, R_L = 50Ω, C_L = 35pF, Figure 1	+25°C		20	25	ns
			T_{MIN} to T_{MAX}			30	
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 2	+25°C		8		pC
DIGITAL I/O							
Input Logic High	$V_{IH\_}$		T_{MIN} to T_{MAX}	1.0			V
Input Logic Low	$V_{IL\_}$		T_{MIN} to T_{MAX}			0.4	V
Input Leakage Current	$I_{IN\_}$	$V_{IN\_}$ = 0 or V+	T_{MIN} to T_{MAX}	-1	0.0005	+1	µA
POWER SUPPLY							
Power-Supply Range	V+			+1.6		+3.6	V
Positive Supply Current	I+	$V_{IN\_}$ = 0 or V+				1	µA

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Parts are tested at +85°C and guaranteed by design and correlation over the full temperature range.
Note 4: R_{ON} and ΔR_{ON} matching specifications for QFN-packaged parts are guaranteed by design.
Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
Note 7: Leakage parameters are 100% tested at the maximum-rated hot operating temperature and guaranteed by correlation at T_A = +25°C.
Note 8: Guaranteed by design, not production tested.
Note 9: Off-Isolation = $20\log_{10}[V_{COM} / (V_{NC}$ or $V_{NO})]$, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

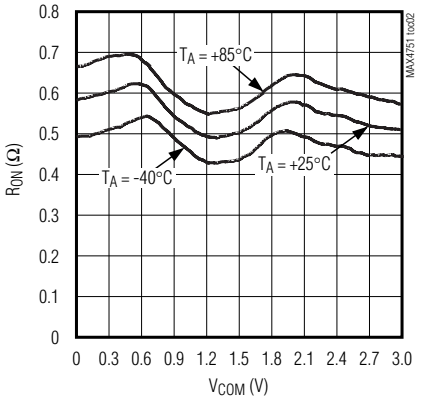
Typical Operating Characteristics

(V+ = +3V and T_A = +25°C, unless otherwise noted.)

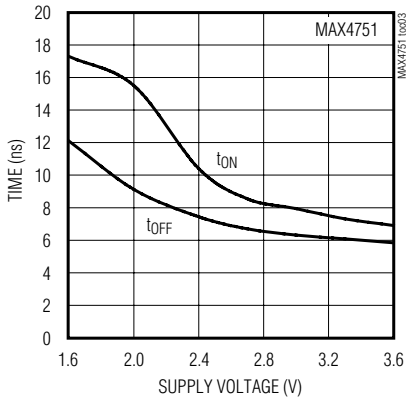
ON-RESISTANCE vs. V_{COM}



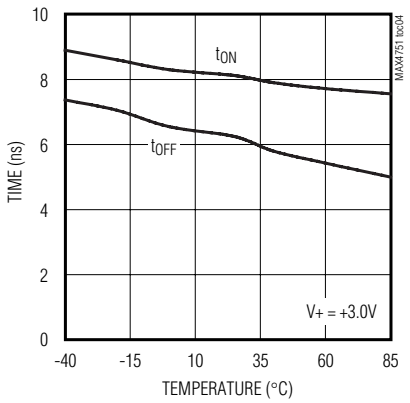
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



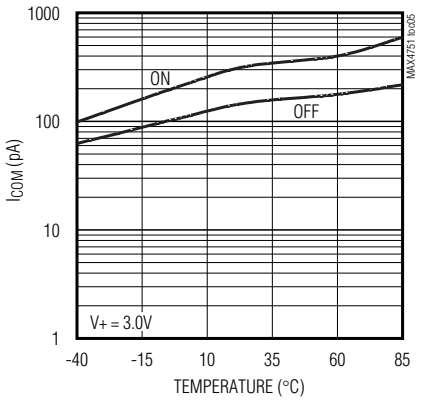
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



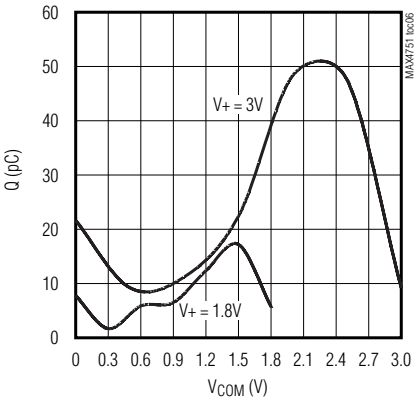
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



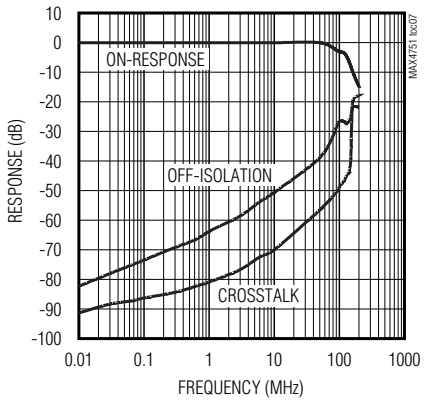
LEAKAGE CURRENT vs. TEMPERATURE



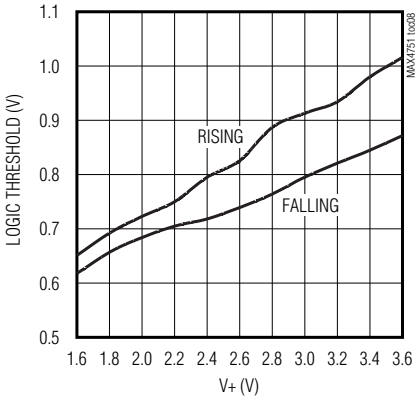
CHARGE INJECTION vs. V_{COM}



FREQUENCY RESPONSE



LOGIC THRESHOLD vs. SUPPLY VOLTAGE

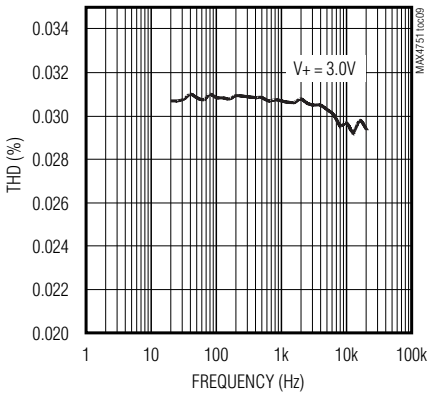


0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

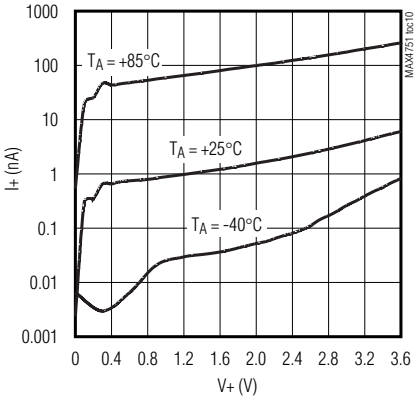
Typical Operating Characteristics (continued)

(V+ = +3V and T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



Pin Description

PIN						NAME	FUNCTION
MAX4751		MAX4752		MAX4753			
TSSOP	QFN	TSSOP	QFN	TSSOP	QFN		
1, 3, 8, 11	15, 1, 7, 11	—	—	—	—	NO1, NO2, NO3, NO4	Switch Normally Open Terminals
—	—	1, 3, 8, 11	15, 1, 7, 11	—	—	NC1, NC2, NC3, NC4	Switch Normally Closed Terminals
—	—	—	—	3, 11	1, 11	NC2, NC4	Switch Normally Closed Terminals
—	—	—	—	1, 8	15, 7	NO1, NO3	Switch Normally Open Terminals
2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	2, 4, 9, 10	16, 2, 8, 9	COM1, COM2, COM3, COM4	Switch Common Terminals
7	6	7	6	7	6	GND	Ground
13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	13, 5, 6, 12	13, 4, 5, 12	IN1, IN2, IN3, IN4	Logic Control Inputs
14	14	14	14	14	14	V+	Positive Supply Voltage
—	3, 10	—	3, 10	—	3, 10	N.C.	No Connection. Not internally connected.

Test Circuits/Timing Diagrams

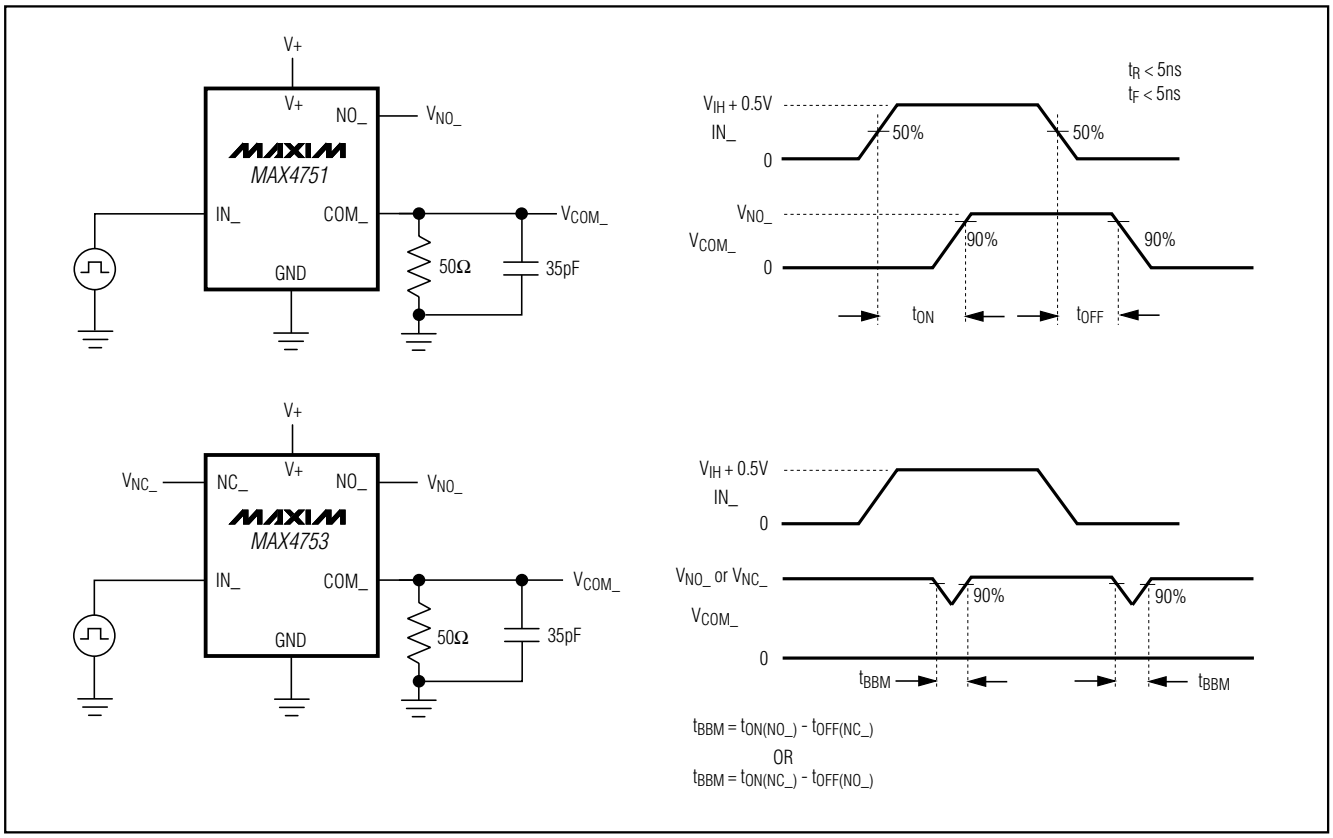


Figure1. Switching Times

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

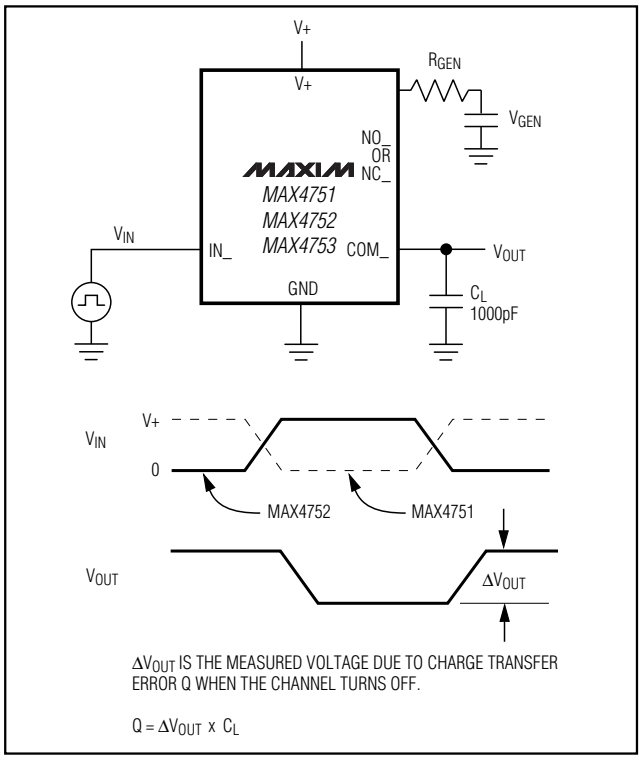


Figure 2. Charge Injection

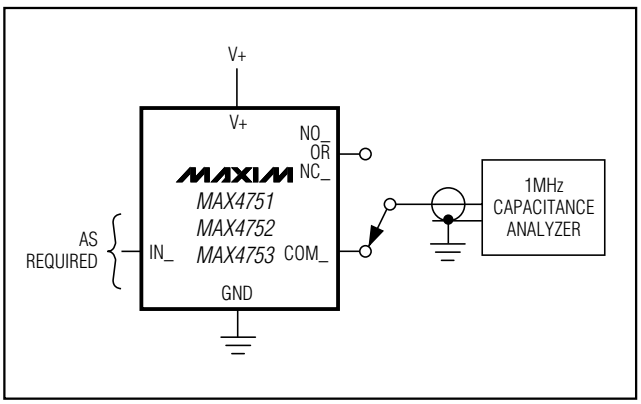


Figure 3. NO_, NC_, and COM_ Capacitance

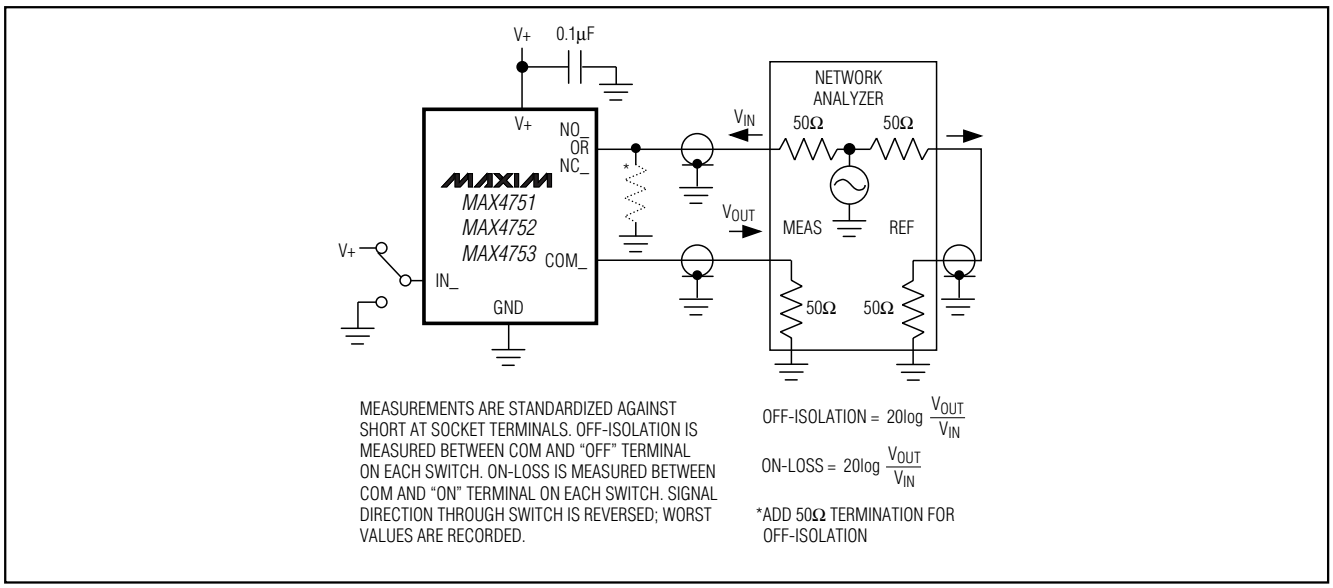


Figure 4. Off-Isolation, On-Loss, and Crosstalk

Detailed Description

The MAX4751/MAX4752/MAX4753 are low 0.9Ω max (at V+ = 3V) on-resistance, low-voltage quad analog switches that operate from a +1.6V to +3.6V single supply. CMOS construction allows switching analog signals that are within the supply voltage range (GND to V+).

When powered from a +3V supply, the 0.9Ω (max) R_{ON} allows high continuous currents to be switched in a variety of applications.

Applications Information

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, followed by NO_, NC_, or COM_. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 5). Adding these diodes reduces the analog signal by one diode drop below V+ and one diode drop above GND, but does not affect the low switch resistance and low leakage characteristics of the device. Device operation is unchanged, and the difference between V+ and GND should not exceed 4V.

Power-supply bypassing is needed to improve noise margin and to prevent switching noise propagation from the V+ supply to other components. A 0.1µF capacitor, connected from V+ to GND, is adequate for most applications.

Logic Inputs

The MAX4751/MAX4752/MAX4753 logic inputs can be driven up to +3.6V regardless of the supply voltage. For example, with a +1.8V supply, IN_ may be driven low to GND and high to +3.6V. Driving IN_ rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be used as either inputs or outputs.

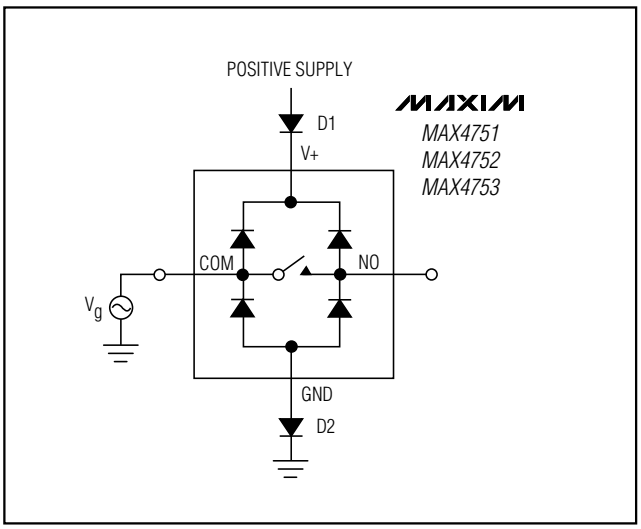


Figure 5. Overvoltage Protection Using Two External Blocking Diodes

Layout

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Chip Information

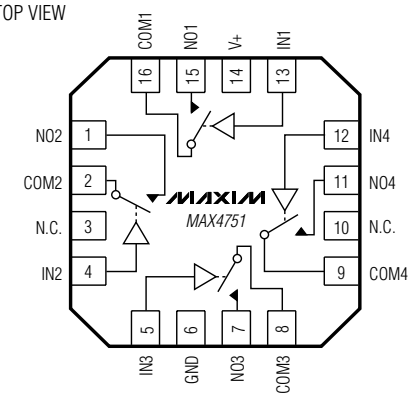
TRANSISTOR COUNT: 228

PROCESS: CMOS

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

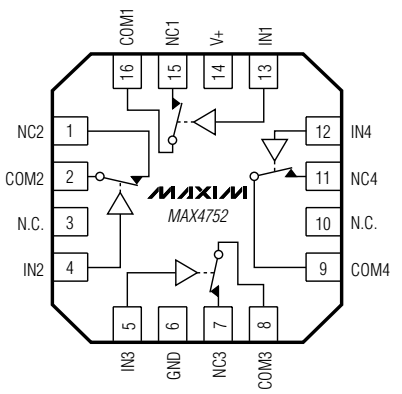
Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



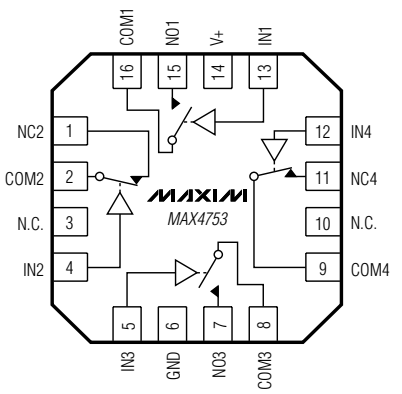
QFN

MAX4751	
INPUT	SWITCH STATE
LOW	OFF
HIGH	ON



QFN

MAX4752	
INPUT	SWITCH STATE
LOW	ON
HIGH	OFF



QFN

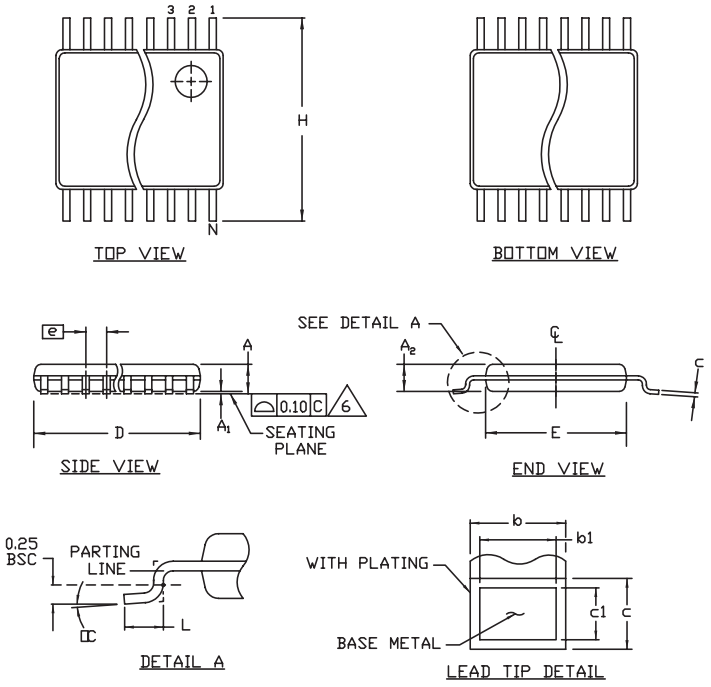
MAX4753		
INPUT	SWITCHES 1, 8	SWITCHES 2, 4
LOW	OFF	ON
HIGH	ON	OFF

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

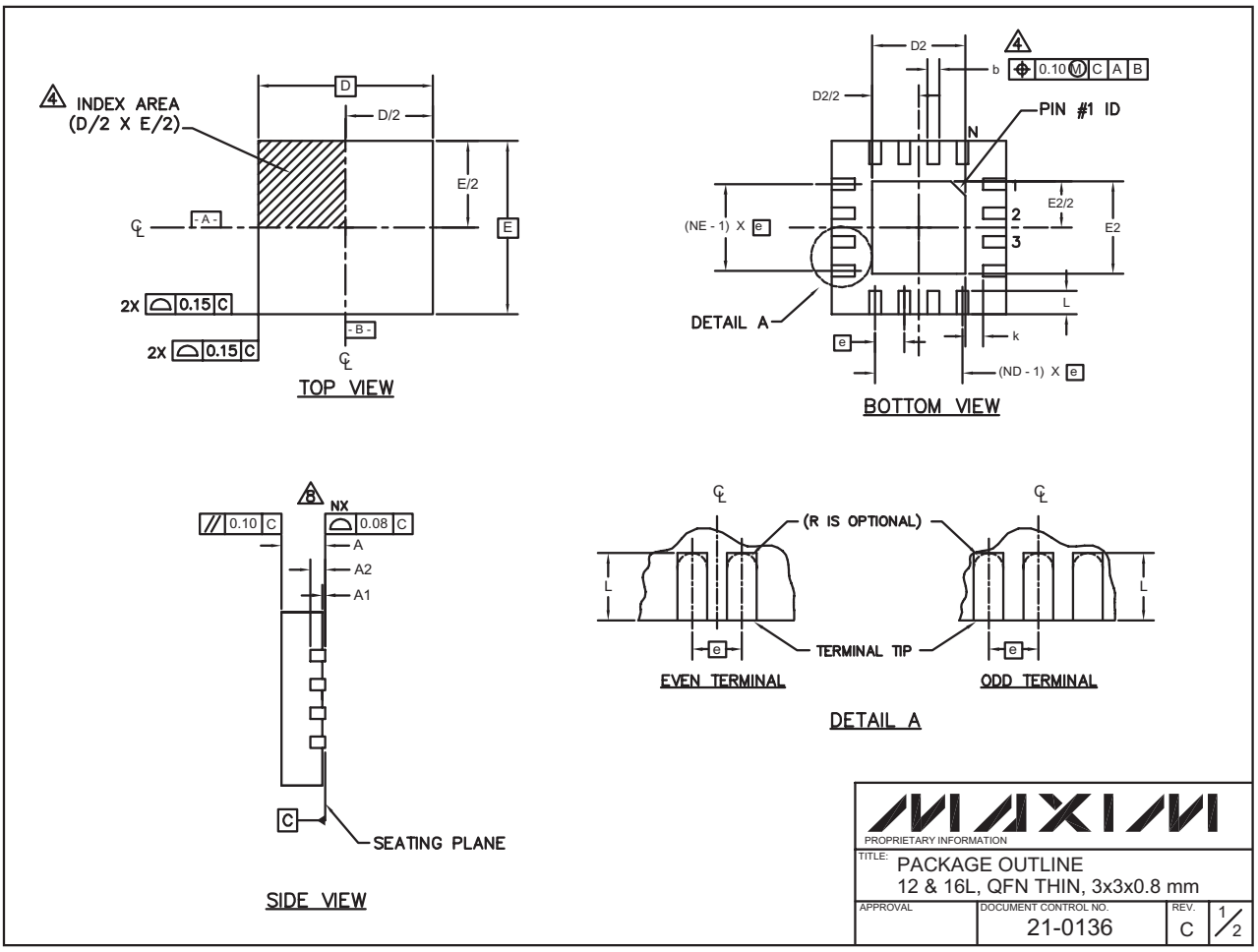
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1

0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



0.9Ω, Low-Voltage, Single-Supply Quad SPST Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12 & 16L, QFN THIN, 3x3x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	C	2/2