

# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V-)

V+ .....	-0.3V, +13V
Voltage into Any Terminal (Note 1) or $\pm 20\text{mA}$ (whichever occurs first) .....	-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal .....	$\pm 20\text{mA}$
Peak Current, NO, NC, or COM <sub>1</sub> (pulsed at 1ms, 10% duty cycle) .....	$\pm 30\text{mA}$
ESD per Method 3015.7 .....	>2000V
Continuous Power Dissipation (T <sub>A</sub> = +70°C) 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...	727mW
8-Pin SO (derate 5.88mW/°C above +70°C) .....	471mW

5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) .....	571mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) .....	640mW
Operating Temperature Ranges	
MAX4516C <sub>1</sub> /MAX4517 <sub>1</sub> .....	0°C to +70°C
MAX4516E <sub>1</sub> /MAX4517E <sub>1</sub> .....	-40°C to +85°C
MAX4516MJA/MAX4517MJA .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10sec) .....	+300°C

**Note 1:** Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS— $\pm 5\text{V}$ Supply

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V<sub>INH</sub> = 3.5V, V<sub>INL</sub> = 1.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH									
Analog Signal Range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>					V-		V+	V
COM to NO or NC On-Resistance	R <sub>ON</sub>	V+ = 5V, V- = -5V, V <sub>NO</sub> or V <sub>NC</sub> = 3V, I <sub>COM</sub> = 1mA	T <sub>A</sub> = +25°C		10		20	Ω	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			25			
COM to NO or NC On-Resistance Flatness	R <sub>FLAT(ON)</sub>	V+ = 5V, V- = -5V; V <sub>NO</sub> or V <sub>NC</sub> = 3V, 0V, -3V; I <sub>COM</sub> = 1mA	T <sub>A</sub> = +25°C		2		4	Ω	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			6			
NO or NC Off-Leakage Current (Note 3)	I <sub>NO(OFF)</sub> I <sub>NC(OFF)</sub>	V+ = 5.5V, V- = 5.5V, V <sub>COM</sub> = ±4.5V, V <sub>NO</sub> or V <sub>NC</sub> = ∓4.5V	T <sub>A</sub> = +25°C		-1	0.01	1	nA	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-20		20		
				M	-100		100		
COM Off-Leakage Current (Note 3)	I <sub>COM(OFF)</sub>	V+ = 5.5V, V- = -5.5V, V <sub>COM</sub> = ±4.5V, V <sub>NO</sub> or V <sub>NC</sub> = ∓4.5V	T <sub>A</sub> = +25°C		-1	0.01	1	nA	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-20		20		
				M	-100		100		
COM On-Leakage Current (Note 3)	I <sub>COM(ON)</sub>	V+ = 5.5V, V- = -5.5V, V <sub>COM</sub> = ±4.5V, V <sub>NO</sub> or V <sub>NC</sub> = ±4.5V	T <sub>A</sub> = +25°C		-2	0.01	2	nA	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	C, E	-40		40		
				M	-200		200		
DIGITAL I/O									
Input Logic High	V <sub>IH</sub>					V+ - 1.5V		V+	V
Input Logic Low	V <sub>IL</sub>					V-		V+ - 3.5V	V
Input Current Logic High or Low	I <sub>IH</sub> , I <sub>IL</sub>	V <sub>IN</sub> = V+, 0V				-0.5	0.03	0.5	μA

# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

MAX4516/MAX4517

## ELECTRICAL CHARACTERISTICS—±5V Supply (continued)

(V<sub>+</sub> = +4.5V to +5.5V, V<sub>-</sub> = -4.5V to -5.5V, V<sub>INH</sub> = 3.5V, V<sub>INL</sub> = 1.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t <sub>ON</sub>	Figure 1	T <sub>A</sub> = +25°C	40	100		ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		150		
Turn-Off Time	t <sub>OFF</sub>	Figure 1	T <sub>A</sub> = +25°C	30	75		ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		125		
Charge Injection (Note 4)	Q	C <sub>L</sub> = 1nF, V <sub>NO</sub> = 0V, R <sub>S</sub> = 0Ω, T <sub>A</sub> = +25°C, Figure 2		10	20		pC
Off Isolation	V <sub>ISO</sub>	R <sub>L</sub> = 50Ω, C <sub>L</sub> = 15pF, V <sub>NO</sub> = 1V <sub>RMS</sub> , f = 100kHz, T <sub>A</sub> = +25°C, Figure 3		-86			dB
NO or NC Off Capacitance	C <sub>NO(OFF)</sub> , C <sub>NO(ON)</sub>	f = 1MHz, T <sub>A</sub> = +25°C, Figure 4		9			pF
COM Off Capacitance	C <sub>COM(OFF)</sub>	f = 1MHz, T <sub>A</sub> = +25°C, Figure 4		9			pF
COM On Capacitance	C <sub>COM(ON)</sub>	f = 1MHz, T <sub>A</sub> = +25°C, Figure 4		22			pF
POWER SUPPLY							
Power-Supply Range				±1		±6	V
V+ Supply Current	I+	V <sub>IN</sub> = 0V or V+	T <sub>A</sub> = +25°C	40	125		μA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		200		
V- Supply Current	I-	V <sub>IN</sub> = 0V or V+	T <sub>A</sub> = +25°C	-125	-30		μA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	200			

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 3:** Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are guaranteed by correlation at +25°C.

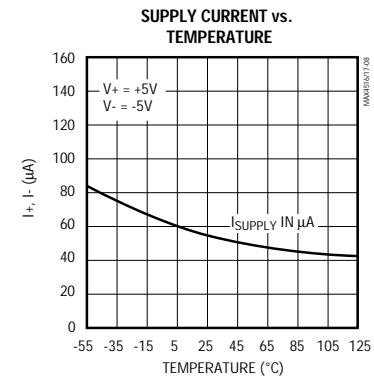
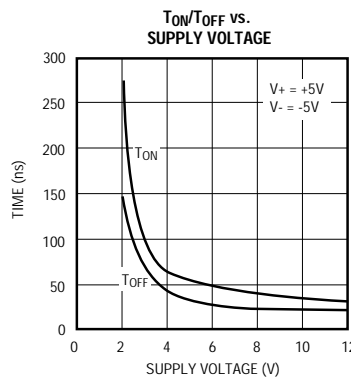
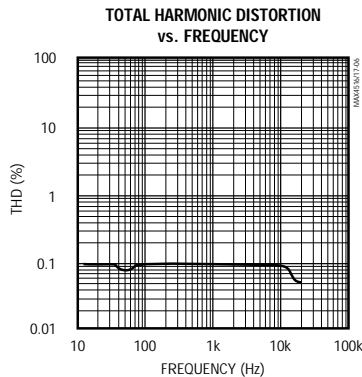
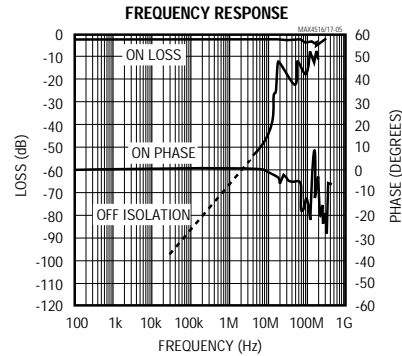
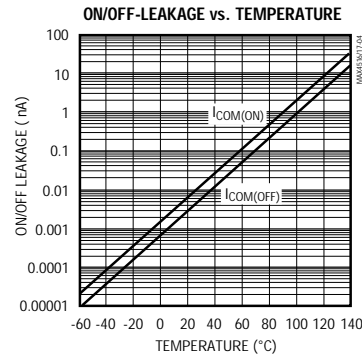
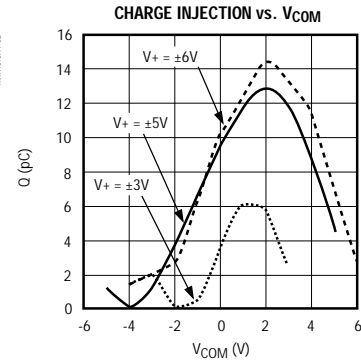
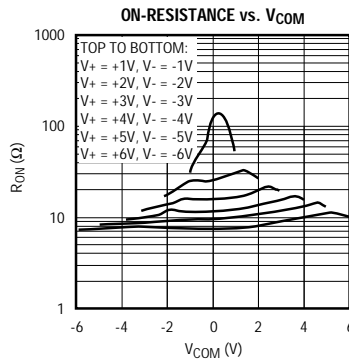
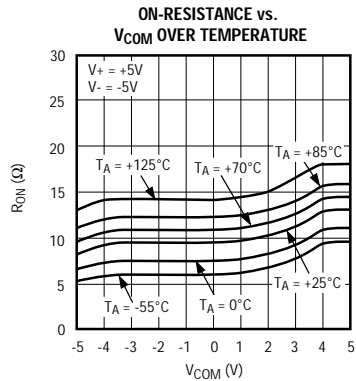
**Note 4:** Guaranteed, not production tested.

**Note 5:** SOT packaged parts are 100% tested at +25°C. Limits at maximum and minimum rated temperature are guaranteed by design and correlation limits at +25°C.

# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

## Typical Operating Characteristics

( $V_+ = +5V$ ,  $V_- = -5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

## Pin Description

PIN				NAME	FUNCTION
MAX4516		MAX4517			
DIP/SO	SOT23-5	DIP/SO	SOT23-5		
1	1	1	1	COM	Analog Switch Common Terminal
2, 3, 5	—	2, 3, 5	—	N.C.	No Connect (not internally connected)
4	5	4	5	V+	Positive Supply-Voltage Input (analog and digital)
6	4	6	4	IN	Digital Control Input
7	3	7	3	V-	Negative Supply-Voltage Input (analog and digital)
8	2	—	—	NO	Analog Switch (normally open)
—	—	8	2	NC	Analog Switch (normally closed)

**Note:** NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass equally well in both directions.

## Applications Information

### Power-Supply Considerations

The MAX4516/MAX4517 operate with power-supply voltages from  $\pm 1\text{V}$  to  $\pm 6\text{V}$ , but are tested and guaranteed only with  $\pm 5\text{V}$  supplies. Similarly, they will operate with a single  $+2\text{V}$  to  $+12\text{V}$  supply, but logic-level inputs can shift with higher voltages. The pin-compatible MAX4514/MAX4515 are recommended for use with a single supply.

The MAX4516/MAX4517 construction is typical of most CMOS analog switches, except that they have only two supply pins:  $V+$  and  $V-$ .  $V+$  and  $V-$  drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both  $V+$  and  $V-$ . One of these diodes conducts if any analog signal exceeds  $V+$  or  $V-$ .

Virtually all the analog leakage current comes from the ESD diodes to  $V+$  or  $V-$ . Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either  $V+$  or  $V-$  and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the  $V+$  and  $V-$  pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

There is no connection between the analog-signal paths and  $V+$  or  $V-$ .

$V+$  and  $V-$  also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched  $V+$  and  $V-$  signals to drive the analog signal gates.

### Logic-Level Thresholds

The logic-level thresholds are CMOS-compatible but **not TTL-compatible**. Since these parts have no ground pin, the logic-level threshold is referenced to  $V+$ . The threshold limits are  $V+ = -1.5\text{V}$  and  $V+ = -3.5\text{V}$  for  $V+$  levels between  $+6\text{V}$  and  $+3\text{V}$ . When  $V+ = +2\text{V}$ , the logic threshold is approximately  $0.6\text{V}$ .

**Do not connect the MAX4516/MAX4517's  $V+$  to  $+3\text{V}$  and then connect the logic-level pins to logic-level signals that operate from a  $+5\text{V}$  supply. TTL levels can exceed  $+3\text{V}$  and violate the absolute maximum ratings, damaging the part and/or external circuits.**

### High-Frequency Performance

In  $50\Omega$  systems, signal response is reasonably flat up to  $250\text{MHz}$  (see *Typical Operating Characteristics*). Above  $20\text{MHz}$ , the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on; it's in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At  $10\text{MHz}$ , off isolation is about  $-48\text{dB}$  in  $50\Omega$  systems, decreasing (approximately  $20\text{dB}$  per decade) as frequency increases. Higher circuit impedances also cause off isolation to decrease. Off isolation is about  $3\text{dB}$  above that of a bare IC socket, and is due entirely to capacitive coupling.

MAX4516/MAX4517

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## Test Circuits/Timing Diagrams

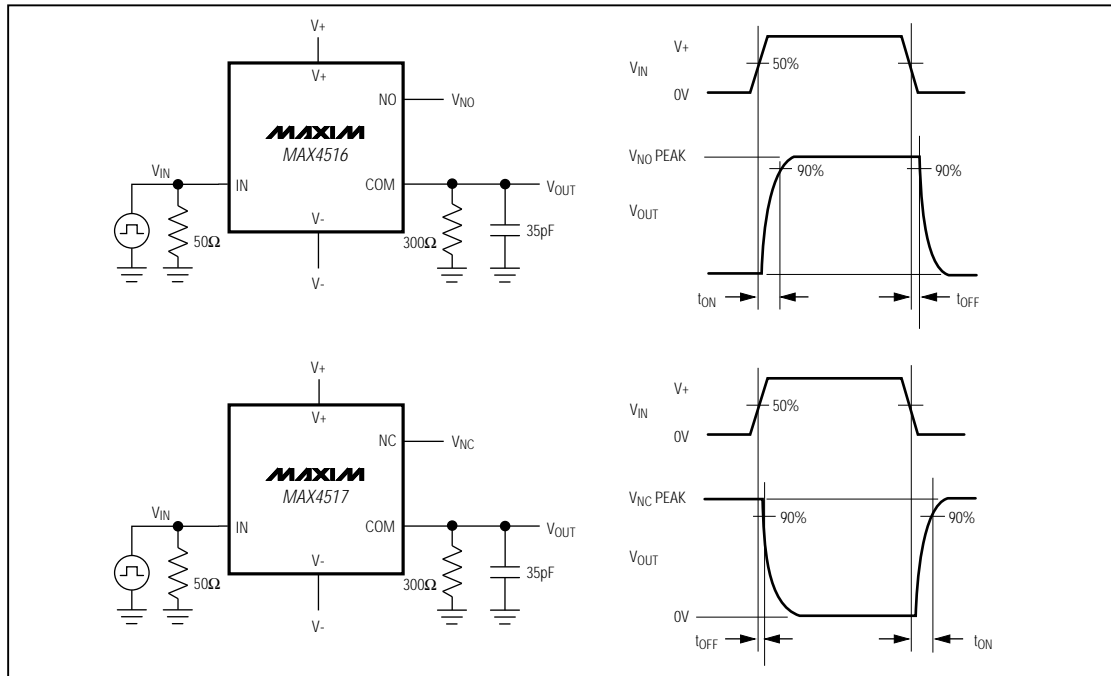


Figure 1. Switching Times

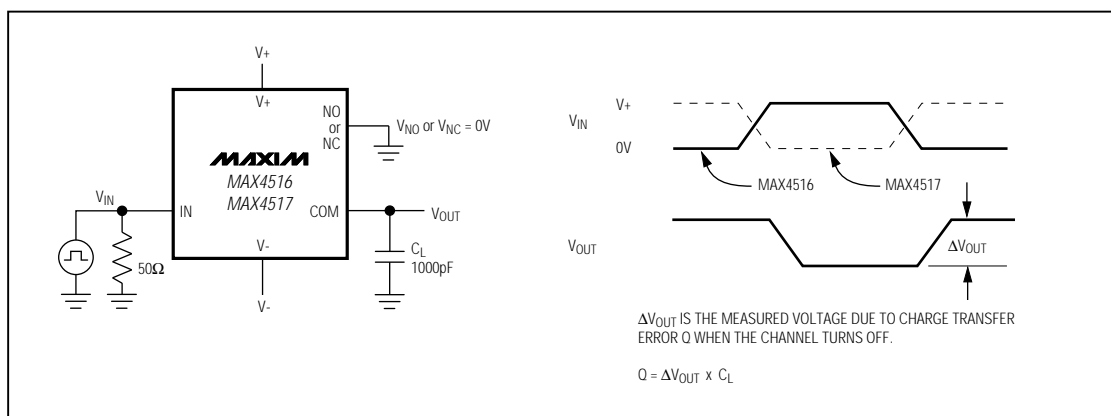


Figure 2. Charge Injection

# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

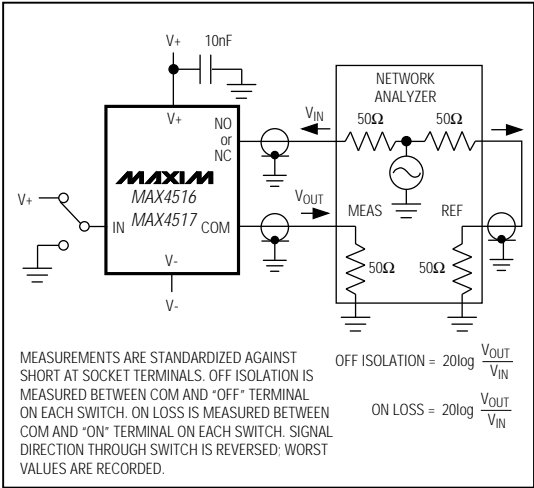


Figure 3. Off Isolation, On Loss, and Crosstalk

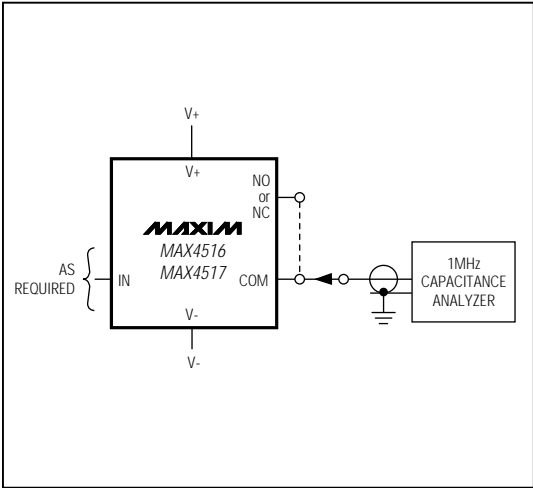


Figure 4. NO, NC, and COM Capacitance

MAX4516/MAX4517

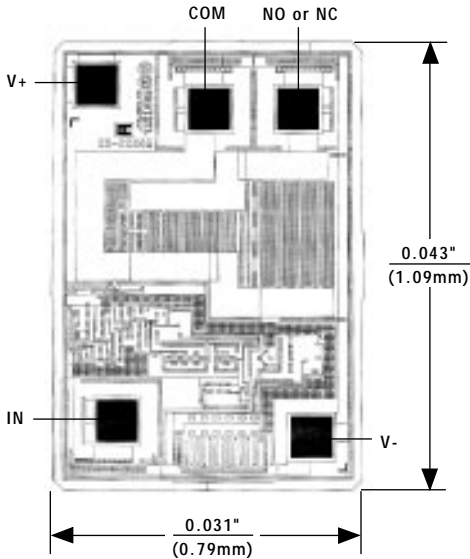
## Chip Topography

### Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4516EPA	-40°C to +85°C	8 Plastic DIP
MAX4516ESA	-40°C to +85°C	8 SO
MAX4516EUK	-40°C to +85°C	5 SOT23-5
MAX4516MJA	-55°C to +125°C	8 Cerdip**
<b>MAX4517CPA</b>	0°C to +70°C	8 Plastic DIP
MAX4517CSA	0°C to +70°C	8 SO
MAX4517CUK	0°C to +70°C	5 SOT23-5
MAX4517C/D	0°C to +70°C	Dice*
MAX4517EPA	-40°C to +85°C	8 Plastic DIP
MAX4517ESA	-40°C to +85°C	8 SO
MAX4517EUK	-40°C to +85°C	5 SOT23-5
MAX4517MJA	-55°C to +125°C	8 Cerdip**

\*Contact factory for dice specifications.

\*\*Contact factory for availability.

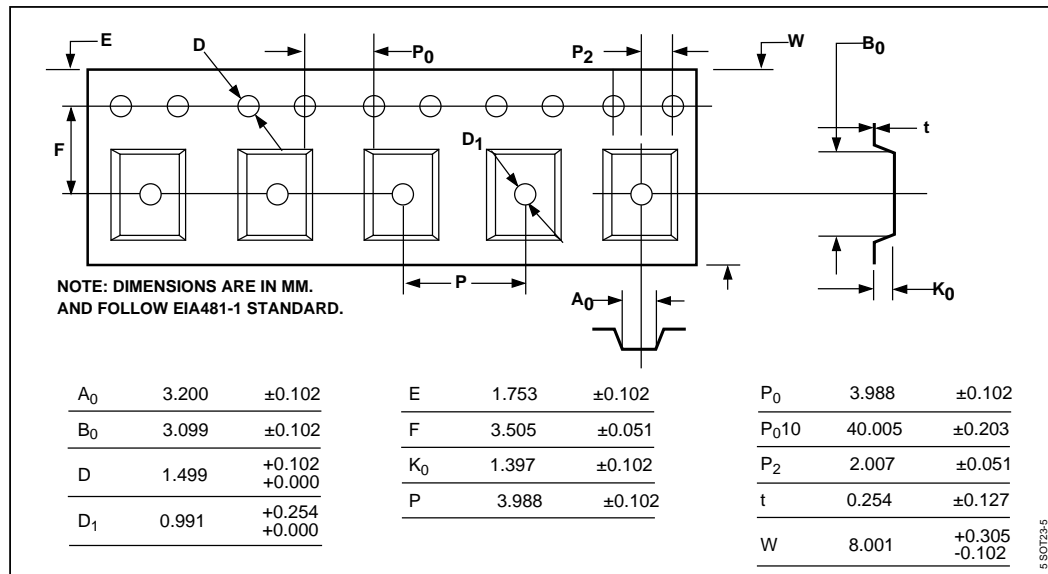


TRANSISTOR COUNT: 36  
SUBSTRATE IS INTERNALLY CONNECTED TO V+

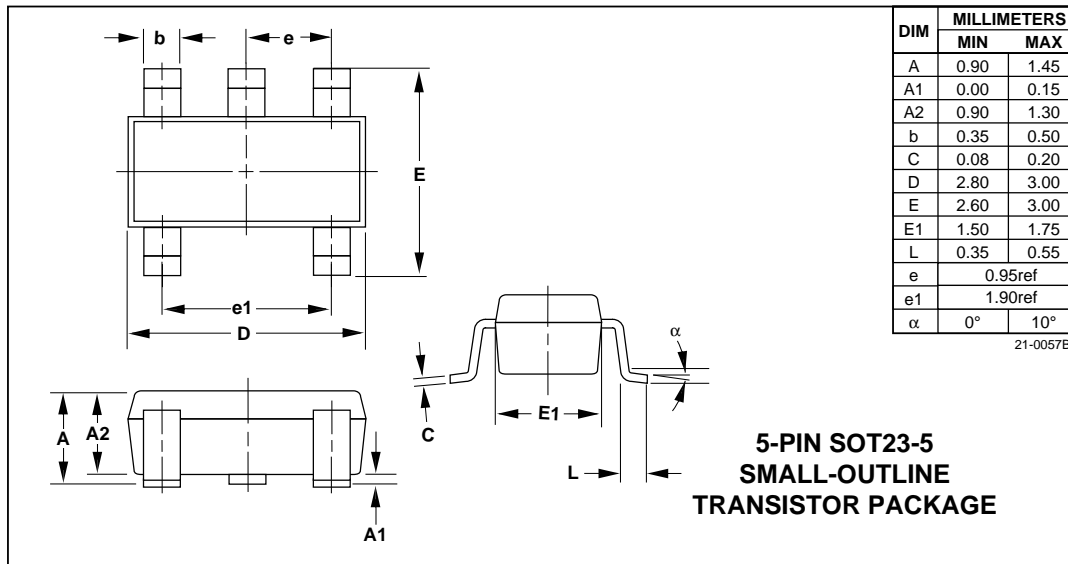
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# Dual-Supply, Low-On-Resistance, SPST, CMOS Analog Switches

## Tape-and-Reel Information



## Package Information



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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