## Absolute Maximum Ratings

Supply Voltage ($V_{DD}$ to $V_{SS}$) ..... 11V
IN+, IN-, OUT Voltage ..... ($V_{DD}$ + 0.3V) to ($V_{SS}$ - 0.3V)
Short-Circuit Duration (to either rail) ..... Continuous
Continuous Power Dissipation ($T_A$ = +70°C)
5-Pin SOT23 (derate 3.9mW/°C above +70°C) ..... 312mW
8-Pin SO (derate 7.4mW/°C above +70°C) ..... 588mW
8-Pin UCSP (derate 4.7mW/°C above +70°C) ..... 379mW
8-Pin µMAX (derate 4.8mW/°C above +70°C) ..... 387mW
14-Pin SO (derate 12.3mW/°C above +70°C) ..... 987mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow, UCSP) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics: 3V Operation

($V_{DD}$ = 3V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ = $V_{DD}$/2, $R_L$ connected to $V_{DD}$/2, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | Inferred from PSRR test | | 2.5 | | 10.0 | V |
| Supply Current (Per Amplifier) | $I_{DD}$ | | | | 25 | 40 | µA |
| Input Bias Current (Note 2) | $I_B$ | | | | 1.0 | 100 | pA |
| Input Offset Voltage | $V_{OS}$ | MAX4162 | $T_A$ = +25°C | | ±0.5 | ±3 | mV |
| | | | $T_A$ = -40°C to +85°C | | | ±4 | |
| | | MAX4163 | $T_A$ = +25°C | | ±0.5 | ±4 | |
| | | | $T_A$ = -40°C to +85°C | | | ±5 | |
| | | MAX4164 | $T_A$ = +25°C | | ±0.5 | ±5 | |
| | | | $T_A$ = -40°C to +85°C | | | ±6 | |
| Input Offset Voltage Tempco | $TCV_{OS}$ | | | | 2 | | µV/°C |
| Differential Input Resistance | $R_{IN}$ | | | | >10 | | TΩ |
| Input Common-Mode Voltage Range | $V_{CM}$ | Inferred from CMRR test | | $V_{SS}$ - 0.25 | | $V_{DD}$ + 0.25 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ($V_{SS}$ - 0.25V) to ($V_{DD}$ + 0.25V) | | 70 | 100 | | dB |
| Large-Signal Voltage Gain | $A_V$ | $R_L$ = 10kΩ | | 85 | 120 | | dB |
| Output Voltage Swing | $V_{OUT}$ | $R_L$ = 10kΩ | $V_{DD}$ - $V_{OH}$ | | 30 | 180 | mV |
| | | | $V_{OL}$ - $V_{SS}$ | | 30 | 180 | |
| | | $R_L$ = 100kΩ | $V_{DD}$ - $V_{OH}$ | | 3 | 25 | |
| | | | $V_{OL}$ - $V_{SS}$ | | 3 | 25 | |
| Output Short-Circuit Current | $I_{SC}$ | To either supply rail | | | 15 | | mA |
| Closed-Loop Output Resistance | $R_{OUT}$ | $A_V$ = 1V/V | | | 0.1 | | Ω |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 2.5V to 10V | | 80 | 110 | | dB |
| Gain-Bandwidth Product | GBWP | | | | 200 | | kHz |
| Phase Margin | ϕM | | | | 60 | | ° |
| Gain Margin | GM | | | | 12 | | dB |
| Total Harmonic Distortion | THD | f = 1kHz, $V_{OUT}$ = $2V_{P-P}$, $R_L$ = 100kΩ, $A_V$ = 1V/V | | | 0.02 | | % |
| Slew Rate | SR | | | | 115 | | V/ms |
| Settling Time to 0.1% | | $V_{OUT}$ = 1V to 2V step | | | 50 | | µs |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 0 to 3V step, $V_{IN}$ = $V_{DD}$/2, $A_V$ = 1V/V | | | 20 | | µs |



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## Electrical Characteristics: 3V Operation (continued)

($V_{DD}$ = 3V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ = $V_{DD}$/2, $R_L$ connected to $V_{DD}$/2, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Voltage-Noise Density | $e_n$ | f = 1kHz | | 80 | | nV/√Hz |
| Differential Input Capacitance | | | | 0.7 | | pF |
| Input Common-Mode Capacitance | | | | 1.5 | | pF |
| Internal Charge-Pump Frequency | | | | 700 | | kHz |
| Charge-Pump Output Feedthrough | | | | 100 | | $\mu V_{P-P}$ |

## Electrical Characteristics: 5V Operation

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ = $V_{DD}$/2, $R_L$ connected to $V_{DD}$/2, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | Inferred from PSRR test | | 4.5 | | 10.0 | V |
| Supply Current (Per Amplifier) | $I_{DD}$ | | | | 25 | 45 | µA |
| Input Bias Current (Note 2) | $I_B$ | | | | 1.0 | 100 | pA |
| Input Offset Voltage | $V_{OS}$ | MAX4162 | $T_A$ = +25°C | | ±0.5 | ±3 | mV |
| | | | $T_A$ = -40°C to +85°C | | | ±4 | |
| | | MAX4163 | $T_A$ = +25°C | | ±0.5 | ±4 | |
| | | | $T_A$ = -40°C to +85°C | | | ±5 | |
| | | MAX4164 | $T_A$ = +25°C | | ±0.5 | ±5 | |
| | | | $T_A$ = -40°C to +85°C | | | ±6 | |
| Input Offset Voltage Tempco | | | | | 2 | | µV/°C |
| Differential Input Resistance | | | | | >10 | | TΩ |
| Input Common-Mode Voltage Range | $V_{CM}$ | Inferred from CMRR test | | $V_{SS}$ - 0.25 | | $V_{DD}$ + 0.25 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = ($V_{SS}$ - 0.25V) to ($V_{DD}$ + 0.25V) | | 70 | 100 | | dB |
| Large-Signal Voltage Gain | $A_V$ | $R_L$ = 10kΩ | | 85 | 120 | | dB |
| Output Voltage Swing | $V_{OUT}$ | $R_L$ = 10kΩ | $V_{DD}$ - $V_{OH}$ | | 50 | 300 | mV |
| | | | $V_{OL}$ - $V_{SS}$ | | 50 | 300 | |
| | | $R_L$ = 100kΩ | $V_{DD}$ - $V_{OH}$ | | 5 | 40 | |
| | | | $V_{OL}$ - $V_{SS}$ | | 5 | 40 | |
| Output Short-Circuit Current | $I_{SC}$ | To either supply rail | | | 15 | | mA |
| Closed-Loop Output Resistance | $R_{OUT}$ | $A_V$ = 1V/V | | | 0.1 | | Ω |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 4.5V to 10V | | 80 | 110 | | dB |
| Gain-Bandwidth Product | GBWP | | | | 200 | | kHz |
| Phase Margin | ϕM | | | | 60 | | ° |
| Gain Margin | GM | | | | 12 | | dB |



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## Electrical Characteristics: 5V Operation (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $V_{OUT}$ = $V_{DD}$/2, $R_L$ connected to $V_{DD}$/2, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

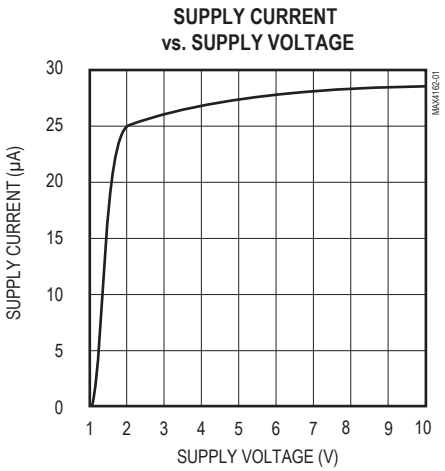
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | THD | f = 1kHz, $V_{OUT}$ = $2V_{P-P}$, $R_L$ = 100kΩ, $A_V$ = 1V/V | | 0.02 | | % |
| Slew Rate | SR | | | 115 | | V/ms |
| Settling Time to 0.1% | | $V_{OUT}$ = 1V to 2V step | | 70 | | µs |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 0 to 3V step, $V_{IN}$ = $V_{DD}$/2, $A_V$ = 1V/V | | 40 | | µs |
| Input Voltage-Noise Density | $e_n$ | f = 1kHz | | 80 | | $nV/\sqrt{Hz}$ |
| Differential Input Capacitance | | | | 0.7 | | pF |
| Input Common-Mode Capacitance | | | | 1.5 | | pF |
| Internal Charge-Pump Frequency | | | | 700 | | kHz |
| Charge-Pump Output Feedthrough | | | | 100 | | $µV_{P-P}$ |

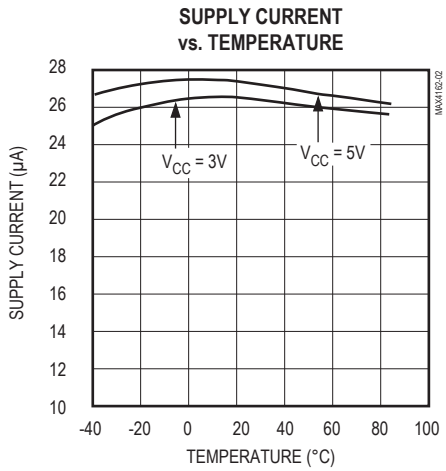
**Note 1:** All device specifications are 100% tested at $T_A$ = +25°C. Limits over the extended temperature range are guaranteed by design, not production tested.

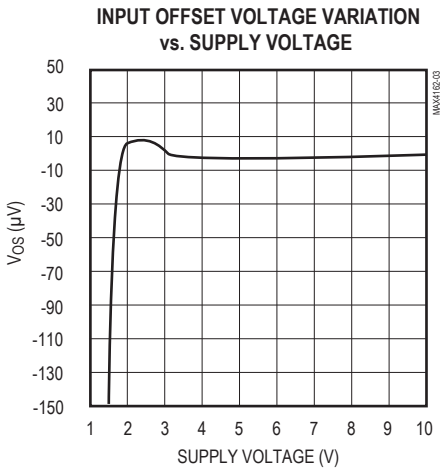
**Note 2:** Input bias current guaranteed by design, not production tested.

## Typical Operating Characteristics

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)



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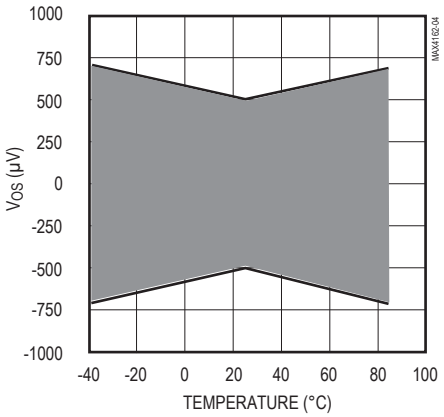
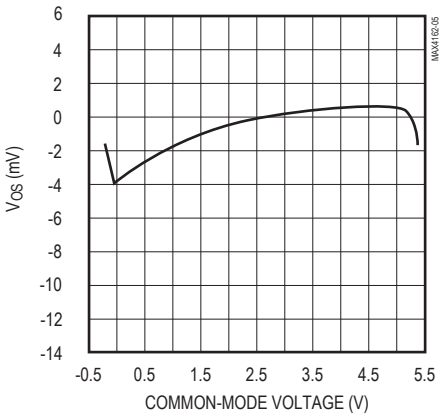
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)

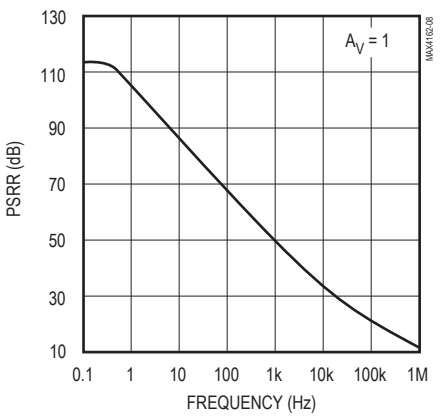
**INPUT OFFSET VOLTAGE vs. TEMPERATURE**



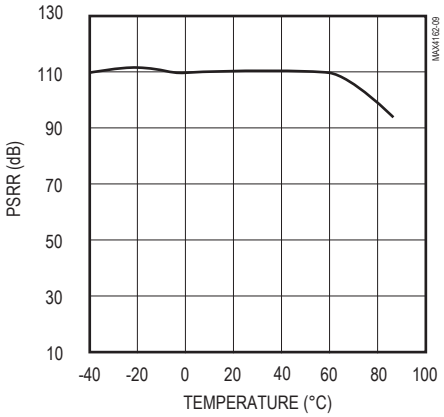

**INPUT OFFSET VOLTAGE VARIATION vs. COMMON-MODE VOLTAGE**



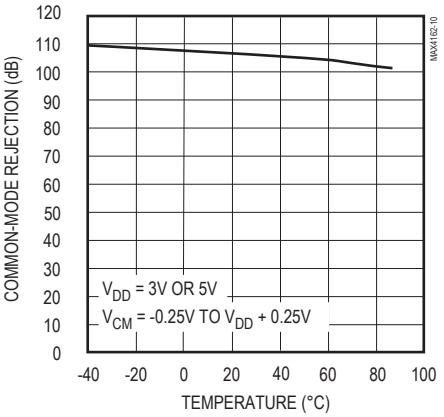

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



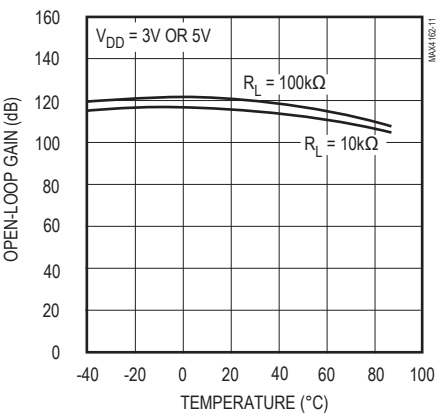

**POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE**



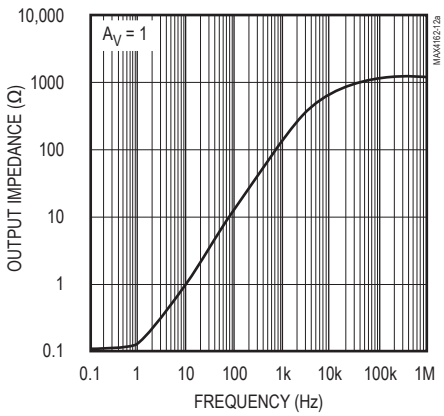

**COMMON-MODE REJECTION vs. TEMPERATURE**



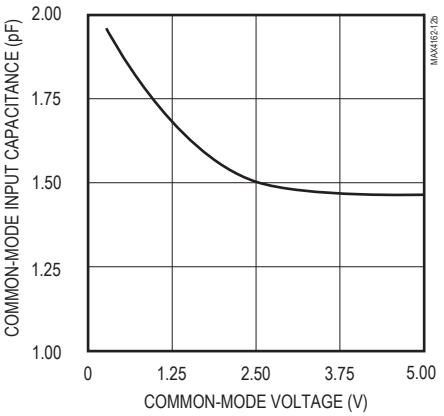

**OPEN-LOOP GAIN vs. TEMPERATURE**



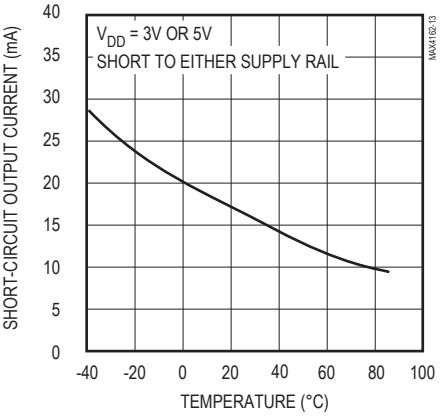

**OUTPUT IMPEDANCE vs. FREQUENCY**




**COMMON-MODE INPUT CAPACITANCE vs. COMMON-MODE VOLTAGE**




**SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE**



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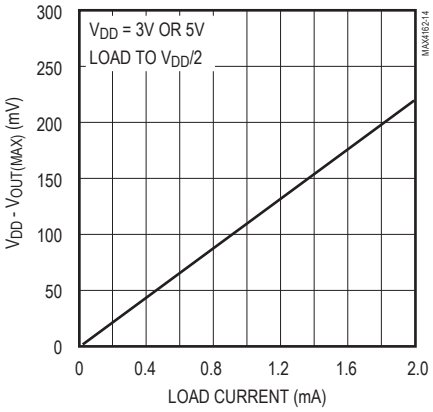
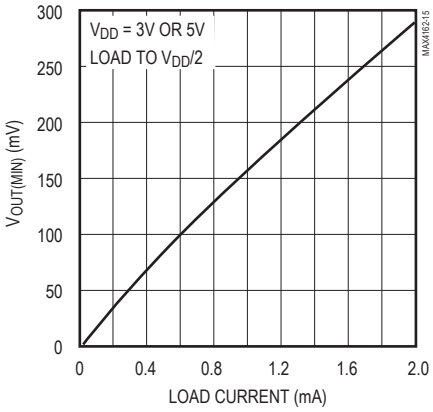
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)

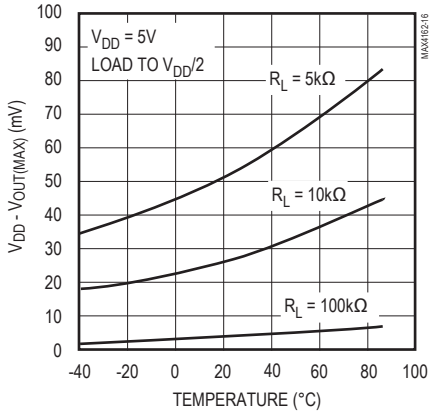
**MAXIMUM OUTPUT VOLTAGE vs. LOAD CURRENT**



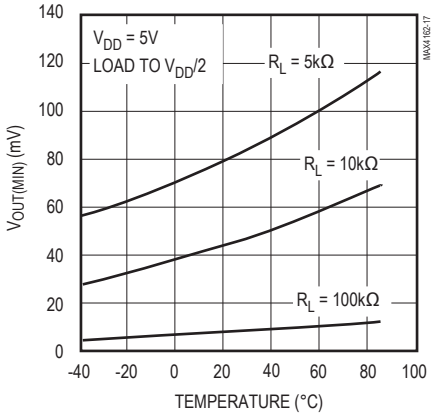

**MINIMUM OUTPUT VOLTAGE vs. LOAD CURRENT**



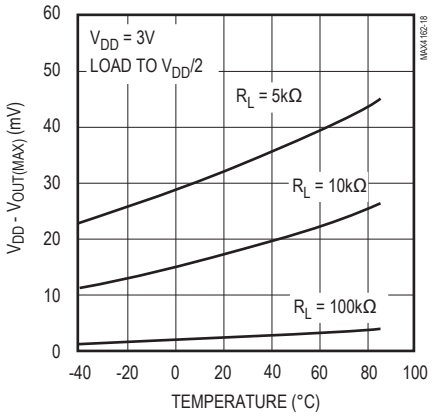

**MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE ($V_{DD}$ = 5V)**



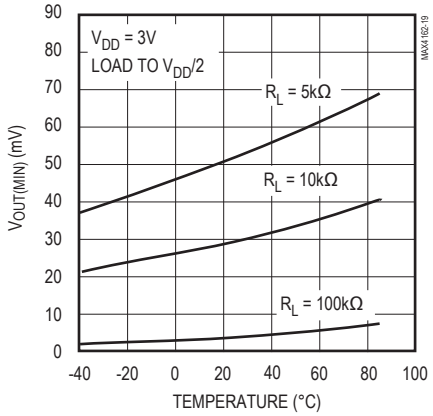

**MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE ($V_{DD}$ = 5V)**



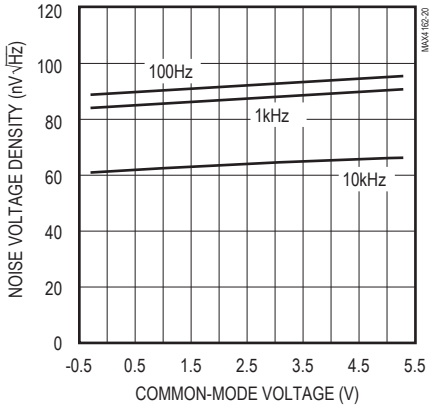

**MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE ($V_{DD}$ = 3V)**



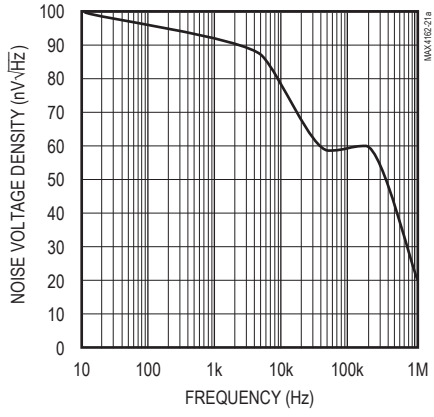

**MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE ($V_{DD}$ = 3V)**



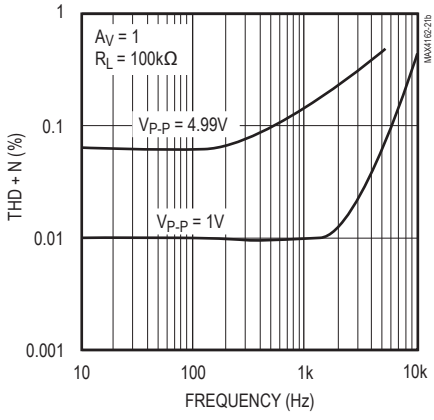

**NOISE VOLTAGE DENSITY vs. COMMON-MODE VOLTAGE**




**NOISE VOLTAGE DENSITY vs. FREQUENCY**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



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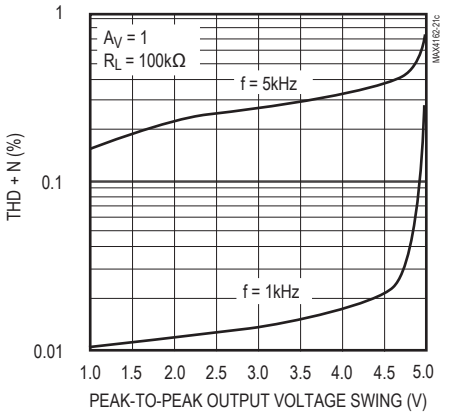
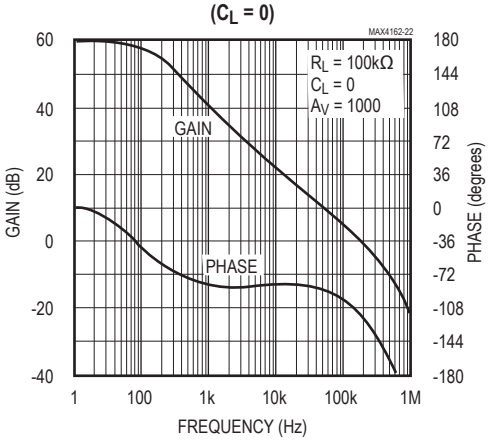
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)

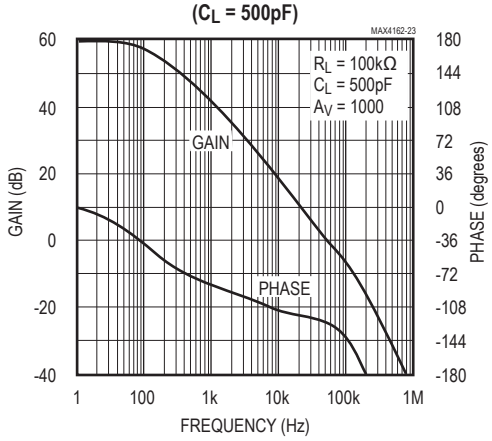
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING**



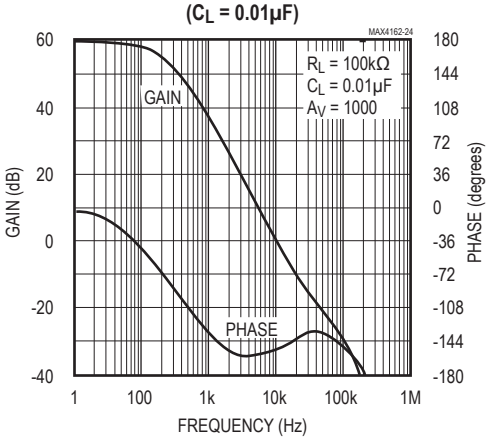

**GAIN AND PHASE vs. FREQUENCY ($C_L$ = 0)**



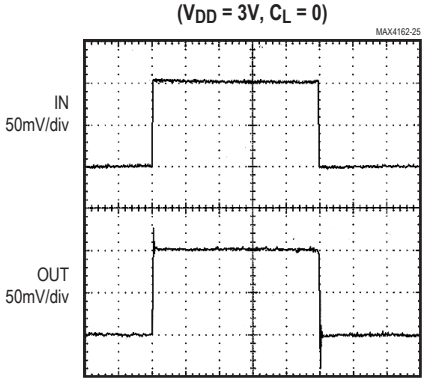

**GAIN AND PHASE vs. FREQUENCY ($C_L$ = 500pF)**




**GAIN AND PHASE vs. FREQUENCY ($C_L$ = 0.01µF)**

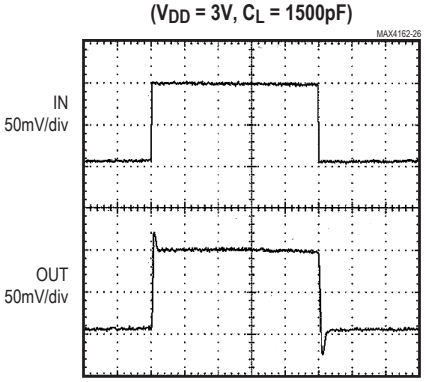



**NONINVERTING SMALL-SIGNAL PULSE RESPONSE ($V_{DD}$ = 3V, $C_L$ = 0)**




$V_{DD}$ = 3V, $V_{IN}$ = 100mV, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 0

**NONINVERTING SMALL-SIGNAL PULSE RESPONSE ($V_{DD}$ = 3V, $C_L$ = 1500pF)**




$V_{DD}$ = 3V, $V_{IN}$ = 100mV, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 1500pF



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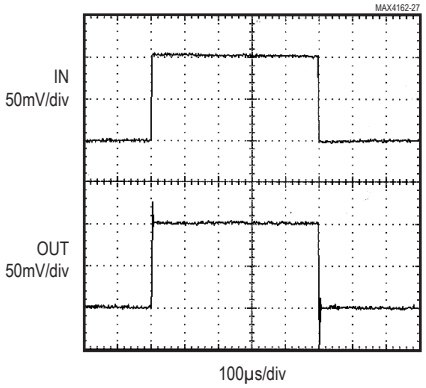
## Typical Operating Characteristics (continued)

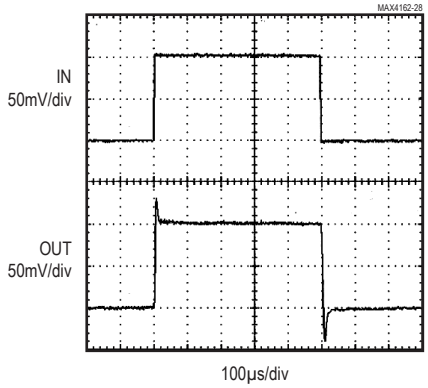
($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)

**NONINVERTING SMALL-SIGNAL PULSE RESPONSE ($V_{DD}$ = 5V, $C_L$ = 0)**



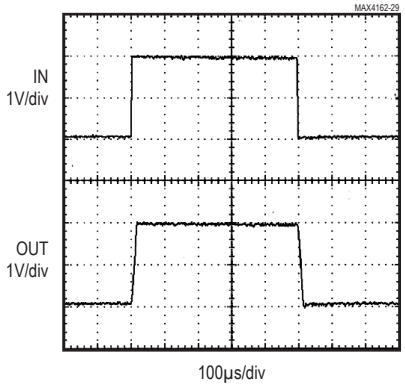

$V_{DD}$ = 5V, $V_{IN}$ = 100mV, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 0

**NONINVERTING SMALL-SIGNAL PULSE RESPONSE ($V_{DD}$ = 5V, $C_L$ = 1500pF)**



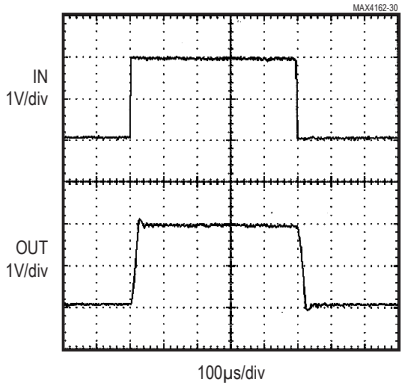

$V_{DD}$ = 5V, $V_{IN}$ = 100mV, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 1500pF

**NONINVERTING LARGE-SIGNAL PULSE RESPONSE ($V_{DD}$ = 3V, $C_L$ = 0)**



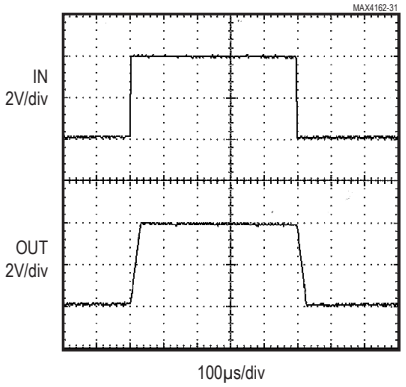

$V_{DD}$ = 3V, $V_{IN}$ = 2V, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 0

**NONINVERTING LARGE-SIGNAL PULSE RESPONSE ($V_{DD}$ = 3V, $C_L$ = 1500pF)**




$V_{DD}$ = 3V, $V_{IN}$ = 2V, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 1500pF

**NONINVERTING LARGE-SIGNAL PULSE RESPONSE ($V_{DD}$ = 5V, $C_L$ = 0)**




$V_{DD}$ = 5V, $V_{IN}$ = 4V, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 0



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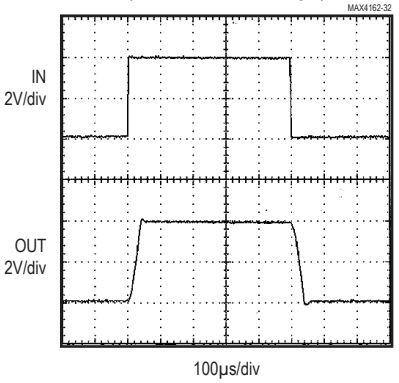
## Typical Operating Characteristics (continued)

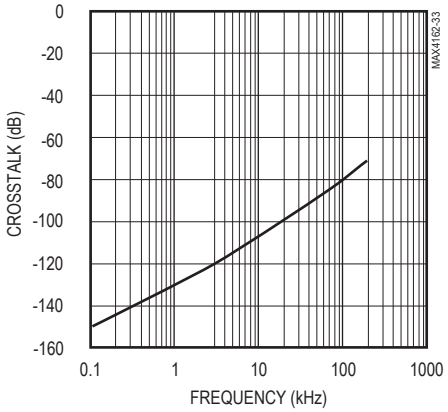
($V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{DD}$/2, $T_A$ = +25°C, unless otherwise noted.)

**NONINVERTING LARGE-SIGNAL PULSE RESPONSE ($V_{DD}$ = 5V, $C_L$ = 1500pF)**




$V_{DD}$ = 5V, $V_{IN}$ = 4V, $R_L$ = 100kΩ to $V_{DD}$/2, $C_L$ = 1500pF

**MAX4163/MAX4164 CROSSTALK vs. FREQUENCY**




## Pin Description

| PIN | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|
| MAX4162 | | MAX4163 | | MAX4164 | | |
| SO | SOT23 | SO/µMAX | UCSP | SO | | |
| 1, 5, 8 | – | – | – | – | N.C. | No Connection. Not internally connected. |
| 2 | 4 | – | – | – | IN- | Amplifier Inverting Input |
| 3 | 3 | – | – | – | IN+ | Amplifier Noninverting Input |
| 4 | 2 | 4 | C2 | 11 | $V_{SS}$ | Negative Power Supply |
| 6 | 1 | – | – | – | OUT | Amplifier Output |
| 7 | 5 | 8 | A2 | 4 | $V_{DD}$ | Positive Power Supply |
| – | – | 1 | A1 | 1 | OUTA | Amplifier A Output |
| – | – | 2 | B1 | 2 | INA- | Amplifier A Inverting Input |
| – | – | 3 | C1 | 3 | INA+ | Amplifier A Noninverting Input |
| – | – | 5 | C3 | 5 | INB+ | Amplifier B Noninverting Input |
| – | – | 6 | B3 | 6 | INB- | Amplifier B Inverting |
| – | – | 7 | A3 | 7 | OUTB | Amplifier B Output |
| – | – | – | – | 8 | OUTC | Amplifier C Output |
| – | – | – | – | 9 | INC- | Amplifier C Inverting Input |
| – | – | – | – | 10 | INC+ | Amplifier C Noninverting Input |
| – | – | – | – | 12 | IND+ | Amplifier D Noninverting Input |
| – | – | – | – | 13 | IND- | Amplifier D Inverting Input |
| – | – | – | – | 14 | OUTD | Amplifier D Output |



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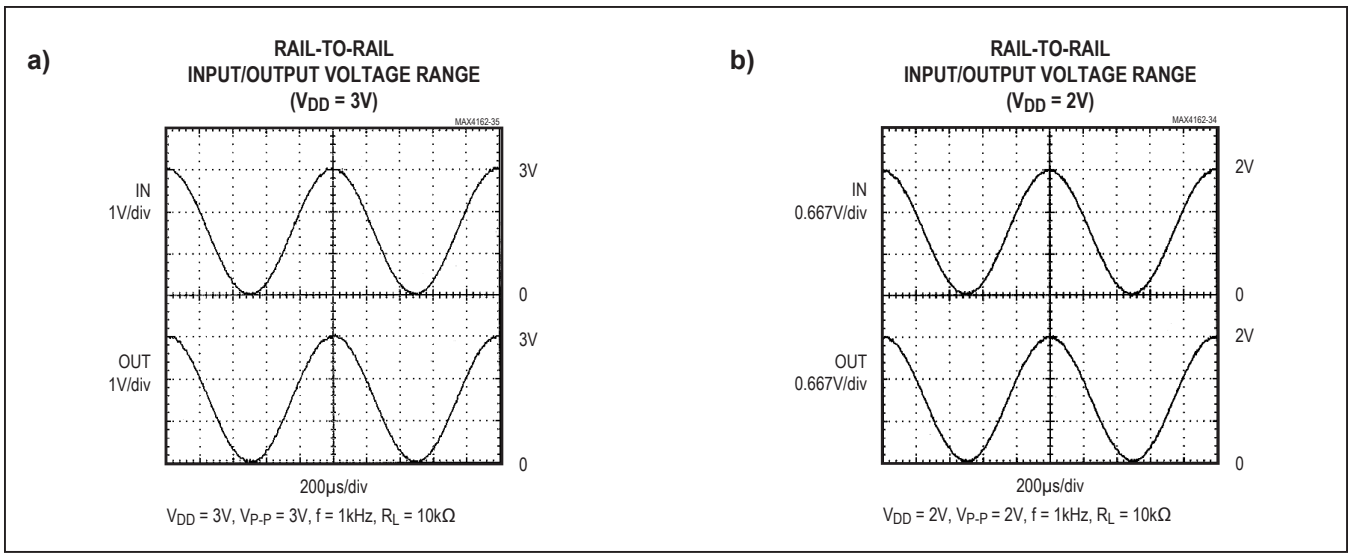
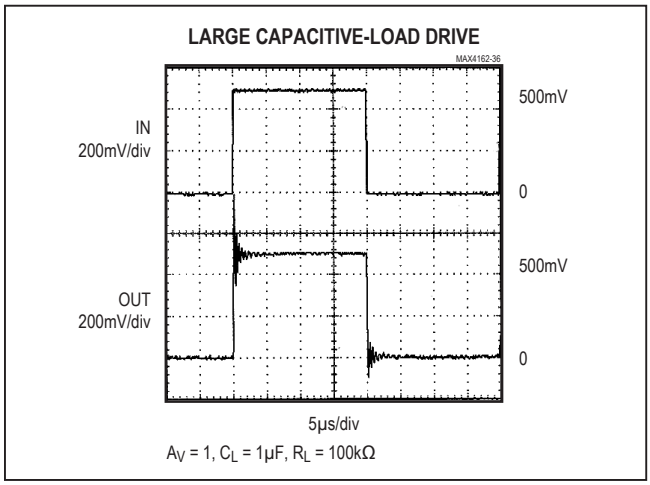



*Figure 1. Rail-to-Rail I/O: a) $V_{DD}$ = 3V; b) $V_{DD}$ = 2V*




*Insert caption here and position to the layout.*

## Applications Information

### Rail-to-Rail Inputs and Outputs

The MAX4162/MAX4163/MAX4164 input common-mode range extends 250mV beyond each of the supply rails, providing a substantial increase in dynamic range over other op amps (even many of those referred to as rail-to-rail). Although the minimum operating voltage is specified at 2.5V, the devices typically provide full rail-to-rail operation below 2.0V (Figure 1). These amplifiers do not suffer from midswing common-mode-rejection degradation or cross-over nonlinearity often encountered in other rail-to-rail op amps. Extremely low, 1.0pA input bias current makes these devices ideal for applications such as pH probes, electrometers, and ionization detectors. They are also protected against phase reversal (inferred from CMRR test) and latchup for input signals extending beyond the supply rails. The output stage achieves a lower output impedance than traditional rail-to-rail output stages, providing an output voltage range that typically swings within 150mV of the supply rails for 1mA loads. This architecture also maintains high open-loop gain and output swing while driving substantial loads.

### Output Loading and Stability

These devices drive 1mA loads to within 150mV of the supply rails while consuming only 25µA of quiescent current. Internal compensation allows these amplifiers to remain unity-gain stable while driving any capacitive load (Figure 2).

### Internal Charge Pump

An internal charge pump provides two internal supplies typically 2V beyond each rail. These internal rails allow the MAX4162/MAX4163/MAX4164 to achieve true rail-to-rail inputs and outputs, while providing excellent common-mode rejection, power-supply rejection ratios, and gain linearity.

These charge pumps require no external components, and in most applications are entirely transparent to the user. Two characteristics may be visible to the user, depending on the application:



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1) The on-board charge pumps generate a small amount of 700kHz switching noise at the op amp's output. The amplitude of this noise is typically 100μ$V_{P-P}$. The noise is **not** referred to the input, and is independent of amplifier gain. The charge-pump switching frequency is well beyond the amplifier's 200kHz bandwidth, and is therefore unnoticeable in most applications.
2) The charge pumps typically require up to 20μs on power-up to fully energize the internal supply rails (Figure 3).

### Power Supplies and Layout

The MAX4162/MAX4163/MAX4164 are guaranteed to operate from a single 2.5V to 10.0V power supply, but full rail-to-rail operation typically extends below 2V. For single-supply operation, bypass the power supply with a 1μF capacitor in parallel with a 0.1μF ceramic capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace and external component lead lengths, and place external components close to the op amp's pins.

### UCSP Package Consideration

For general UCSP package information and PC layout considerations, please refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale-Package).

## UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP. Performance through operating life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered.

Table 1 shows the testing done to characterize the UCSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in the table. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at **www.maximintegrated.com**.

## Table 1. Reliability Test Data

| TEST | CONDITIONS | DURATION | NO. OF FAILURES PER SAMPLE SIZE |
|---|---|---|---|
| Temperature Cycle | -35°C to +85°C, -40°C to +100°C | 150 cycles, 900 cycles | 0/10, 0/200 |
| Operating Life | $T_A$ = +70°C | 240h | 0/10 |
| Moisture Resistance | -20°C to +60°C, 90% RH | 240h | 0/10 |
| Low-Temperature Storage | -20°C | 240h | 0/10 |
| Low-Temperature Operational | -10°C | 24h | 0/10 |
| Solderability | 8h steam age | — | 0/15 |
| ESD | ±2000V, Human Body Model | — | 0/5 |
| High-Temperature Operating Life | $T_J$ = +150°C | 168h | 0/45 |



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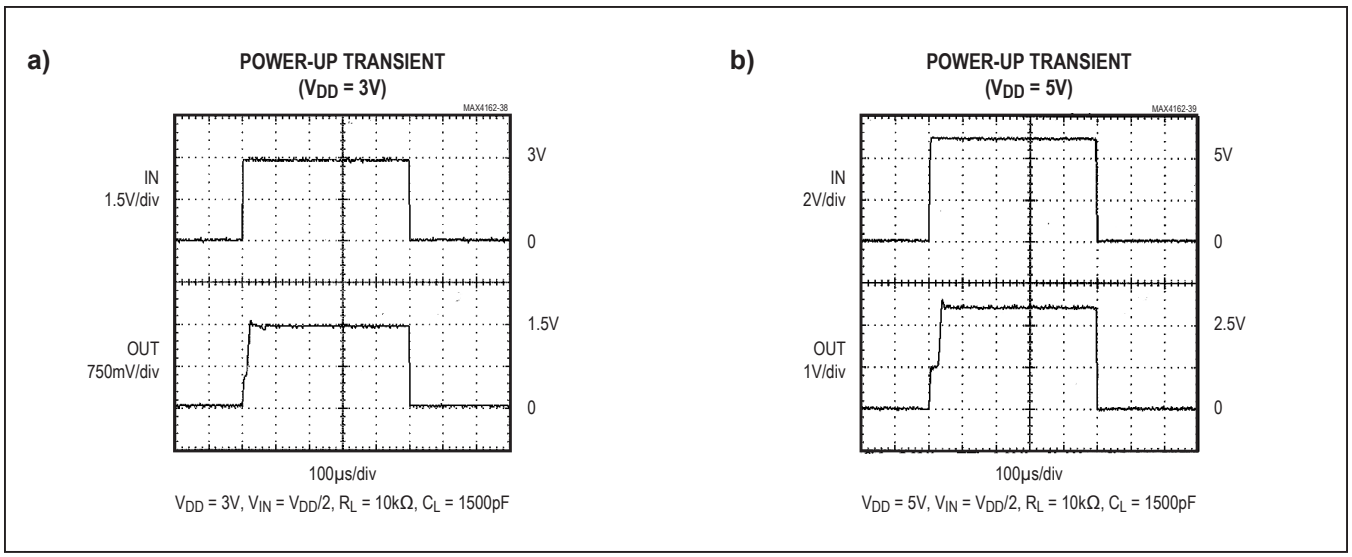
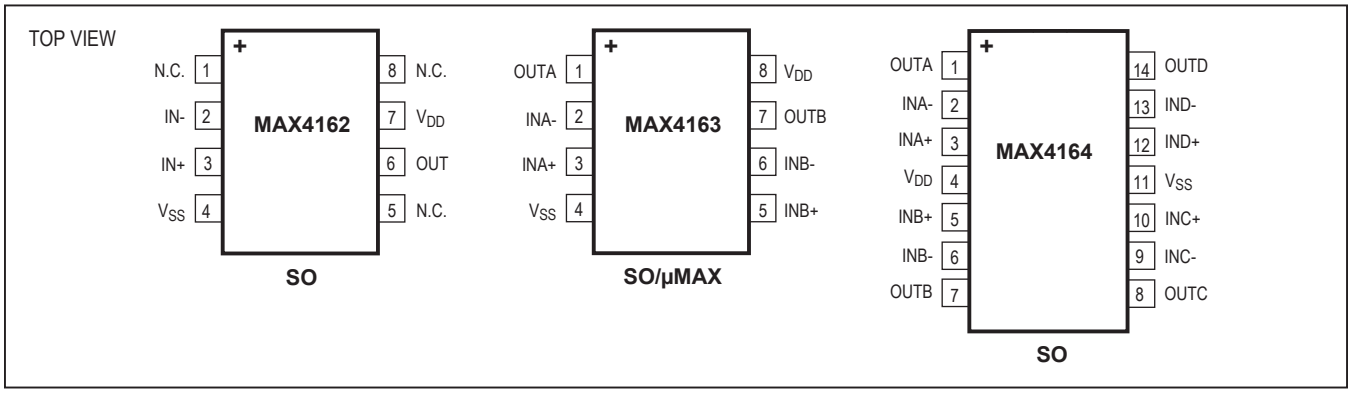



*Figure 3. Power-Up Transient: a) $V_{DD}$ = 3V; b) $V_{DD}$ = 5V*

## Pin Configurations (continued)




## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 8 SO | S8-2, S8-4 | 21-0041 |
| 5 SOT23 | U5-1 | 21-0057 |
| 8 UCSP | B9-5 | 21-0093 |
| 8 µMAX | U8-1 | 21-0036 |
| 14 SO | S14M-5 | 21-0041 |



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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 2 | 5/09 | Changed operating supply voltage from 2.7V to 2.5V | 1, 2, 3, 10, 11 |
| 3 | 1/10 | Updated PSRR condition for 5V operation, added lead-free designation to *Ordering Information*, and added UCSP soldering temperature | 1–9, 12 |
| 4 | 8/19 | Updated *Pin Configurations* | 1 |

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