

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+-0.3V, 44V

GND-0.3V, 25V

Digital Inputs, NO, COM (Note 1).....(V- - 2V) to (V+ + 2V) or
30mA (whichever occurs first)

Continuous Current (any terminal)30mA

Peak Current, NO or COM

(pulsed at 1ms, 10% duty cycle max)100mA

Continuous Power Dissipation (TA = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C)842mW

Narrow SO (derate 8.70mW/°C above +70°C)696mW

16-Pin TQFN (derate 21.3mW/°C above +70°C)1702mW

CERDIP (derate 10.00mW/°C above +70°C)800mW

Operating Temperature Ranges

MAX33_C_0°C to +70°C

MAX33_E_-40°C to +85°C

MAX33_MJE-55°C to +125°C

Storage Temperature Range-65°C to +150°C

Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on NO, COM, EN, A0, A1, or A2 exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, VAH = +2.4V, VAL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS	
SWITCH									
Analog Signal Range	V _{NO} , V _{COM}	(Note 3)			-15		15	V	
On-Resistance	R _{ON}	I _{NO} = 0.2mA, V _{COM} = ±10V	T _A = +25°C		220		400	Ω	
			T _A = T _{MIN} to T _{MAX}			500			
On-Resistance Matching Between Channels	ΔR _{ON}	I _{NO} = 0.2mA, V _{COM} = ±10V (Note 4)	T _A = +25°C		4		10	Ω	
			T _A = T _{MIN} to T _{MAX}			15			
NO-Off Leakage Current (Note 5)	I _{NO(OFF)}	V _{COM} = ∓10V, V _{NO} = ±10V, V _{EN} = 0V	T _A = +25°C		-0.02	0.001	0.02	nA	
			T _A = T _{MIN} to T _{MAX}	C, E	-1.25		1.25		
				M	-20		20		
COM-Off Leakage Current (Note 5)	I _{COM(OFF)}	V _{NO} = ±10V, V _{COM} = ∓10V, V _{EN} = 0V	MAX338	T _A = +25°C		-0.05	0.005	0.05	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-3.25		3.25	
					M	-40		40	
		V _{NO} = ∓10V, V _{COM} = ±10V, V _{EN} = 0V	MAX339	T _A = +25°C		-0.05	0.005	0.05	
				T _A = T _{MIN} to T _{MAX}	C, E	-1.65		1.65	
					M	-20		20	
COM-On Leakage Current (Note 5)	I _{COM(ON)}	V _{COM} = ±10V, V _{NO} = ±10V, sequence each switch on	MAX338	T _A = +25°C		-0.05	0.006	0.05	nA
				T _A = T _{MIN} to T _{MAX}	C, E	-3.25		3.25	
					M	-40		40	
		MAX339	T _A = +25°C		-0.05	0.008	0.05		
			T _A = T _{MIN} to T _{MAX}	C, E	-1.65		1.65		
				M	-20		20		

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

MAX338/MAX339

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I _{AH}	V _A = 2.4V or 15V		-1.0	0.001	1.0	μA
Input Current with Input Voltage Low	I _{AL}	V _{EN} = 0V or 2.4V, V _A = 0V		-1.0		1.0	μA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	V _{EN} = V _A = 0V	T _A = +25°C	50	100	μA	
			T _A = T _{MIN} to T _{MAX}	150			
		V _{EN} = 2.4V, V _{A(ALL)} = 2.4V	T _A = +25°C	290	500	μA	
			T _A = T _{MIN} to T _{MAX}	600			
Negative Supply Current	I-	V _{EN} = 0V or 2.4V, V _{A(ALL)} = 0V, 2.4V or 5V	T _A = +25°C	-1	1	μA	
			T _A = T _{MIN} to T _{MAX}	-10	10		
DYNAMIC							
Transistion Time	t _{TRANS}	Figure 2		T _A = +25°C	200	500	ns
Break-Before-Make Interval	t _{OPEN}	Figure 4		T _A = +25°C	10	140	ns
Enable Turn-On Time	t _{ON(EN)}	Figure 3		T _A = +25°C	160	500	ns
				T _A = T _{MIN} to T _{MAX}	750		
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3		T _A = +25°C	100	500	ns
				T _A = T _{MIN} to T _{MAX}	750		
Charge Injection (Note 3)	Q	C _L = 100pF, V _{NO} = 0V, R _S = 0Ω, Figure 6		T _A = +25°C	1.5	5	pC
Off Isolation (Note 6)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz		T _A = +25°C	-75		dB
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{P-P} , R _L = 1kΩ, Figure 7		T _A = +25°C	-92		dB
Logic Input Capacitance	C _{IN}	f = 1MHz		T _A = +25°C	2		pF
NO-Off Capacitance	C _{NO(OFF)}	f = 1MHz, V _{EN} = V _{NO} = 0V, Figure 8		T _A = +25°C	3		pF
COM-Off Capacitance	C _{COM(OFF)}	f = 1MHz, V _{EN} = 0.8V, V _{COM} = 0V, Figure 8	MAX338	T _A = +25°C	11	pF	
			MAX339		6		
COM-On Capacitance	C _{COM(ON)}	f = 1MHz, V _{EN} = 2.4V, V _{COM} = 0V, Figure 8	MAX338	T _A = +25°C	16	pF	
			MAX339		9		

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V₊ = +12V, V₋ = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V _{NO} , V _{COM}	(Note 3)		0		12	V
On-Resistance	R _{ON}	I _{NO} = 0.2mA V _{COM} = 3V or 10V	T _A = +25°C		460	650	Ω
DYNAMIC							
Transition Time (Note 3)	t _{TRANS}	V _{NO1} = 8V, V _{NO8} = 0V, V _{IN} = 2.4V, Figure 1	T _A = +25°C		210	500	ns
Enable Turn-On Time (Note 3)	t _{ON(EN)}	V _{INH} = 2.4V, V _{INL} = 0V, V _{NO1} = 5V, Figure 3	T _A = +25°C		280	500	ns
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}	V _{INH} = 2.4V, V _{INL} = 0V, V _{NO1} = 5V, Figure 3	T _A = +25°C		110	500	ns
Charge Injection (Note 3)	Q	C _L = 100pF, V _{NO} = 0V, R _S = 0Ω	T _A = +25°C		1.8	5	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

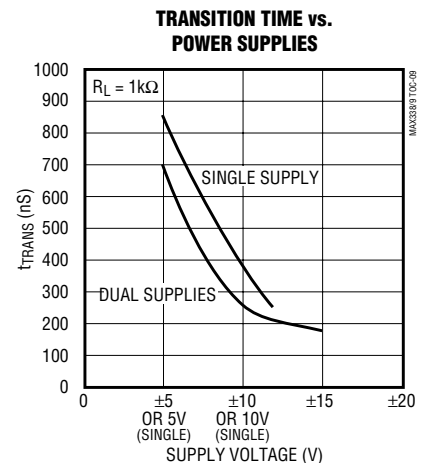
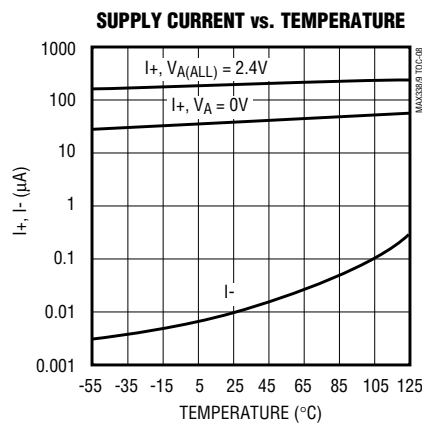
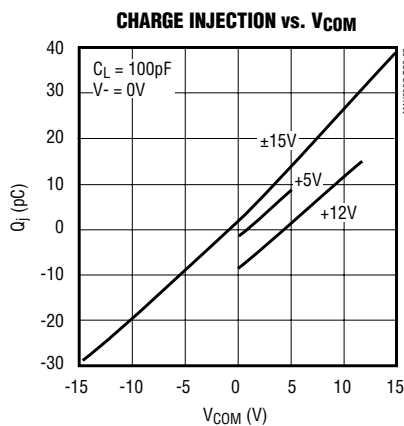
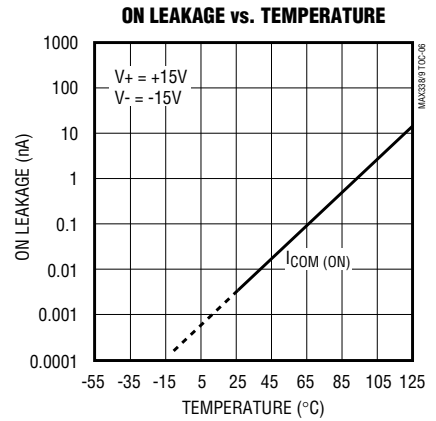
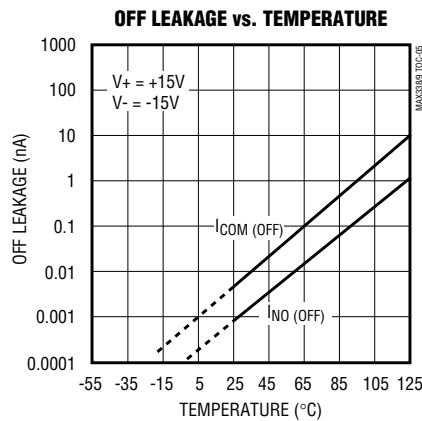
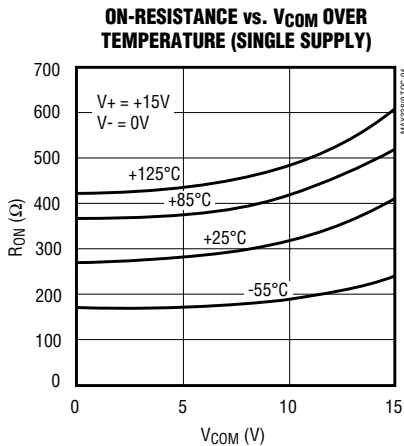
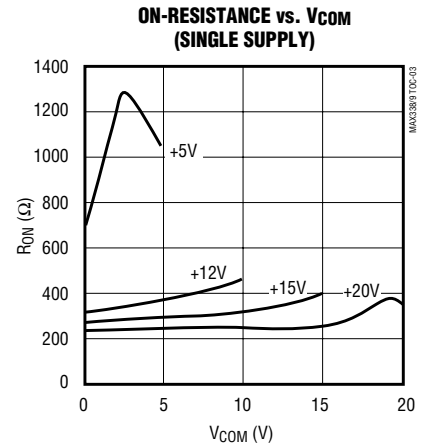
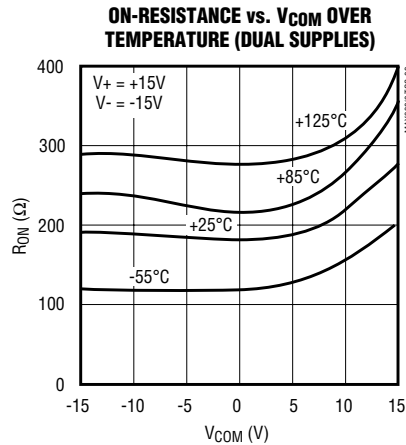
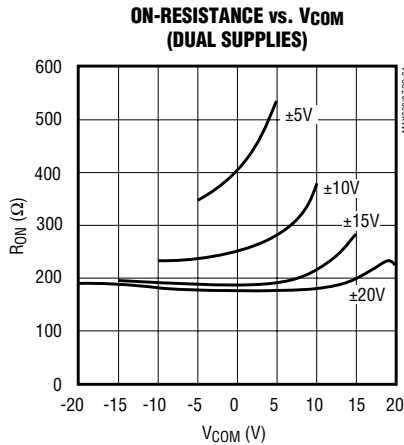
Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = 20log V_{COM}/V_{NO}, where V_{COM} = output and V_{NO} = input to off switch.

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX338/MAX339



8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Description

PIN				NAME	FUNCTION
MAX338		MAX339			
DIP/SO	THIN QFN	DIP/SO	THIN QFN		
1, 15, 16,	15, 14, 13	—	—	A0, A2, A1	Address Inputs
—	—	1, 16	15, 14	A0, A1	Address Inputs
2	16	2	16	EN	Enable
3	1	3	1	V-	Negative-Supply Voltage Input
4–7	2–5	—	—	NO1–NO14	Analog Inputs—Bidirectional
—	—	4–7	2–5	NO1A–NO4A	Analog Inputs—Bidirectional
8	6	—	—	COM	Analog Output—Bidirectional
—	—	8, 9	6, 7	COMA, COMB	Analog Outputs—Bidirectional
9–12	7–10	—	—	NO8–NO5	Analog Inputs—Bidirectional
—	—	10–3	8–11	NO4B–NO1B	Analog Inputs—Bidirectional
13	11	14	12	V+	Positive-Supply Voltage Input
14	12	15	13	GND	Ground
—	EP	—	EP	Exposed Pad	Exposed Pad. Connect to V+.

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than $\pm 15\text{V}$ will reduce the analog signal range. The MAX338/MAX339 switches operate with $\pm 4.5\text{V}$ to $\pm 20\text{V}$ bipolar supplies or with a $+4.5\text{V}$ to $+30\text{V}$ single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies such as $+24\text{V}$ and -5V . The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs NO and COM. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 44V.

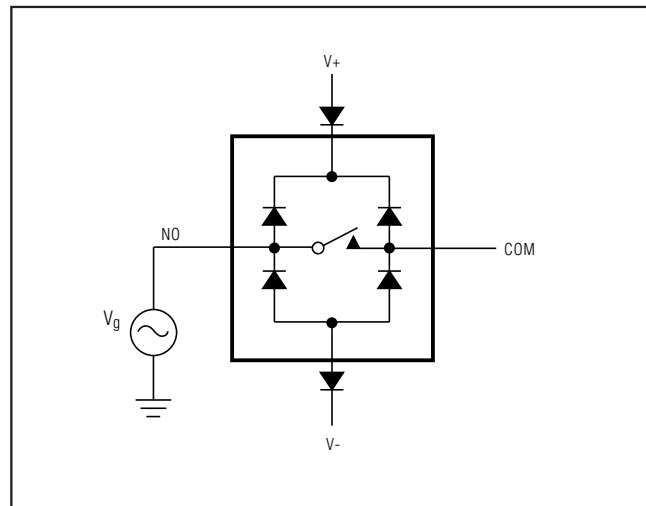


Figure 1. Overvoltage Protection Using External Blocking Diodes

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Test Circuits/Timing Diagrams

MAX338/MAX339

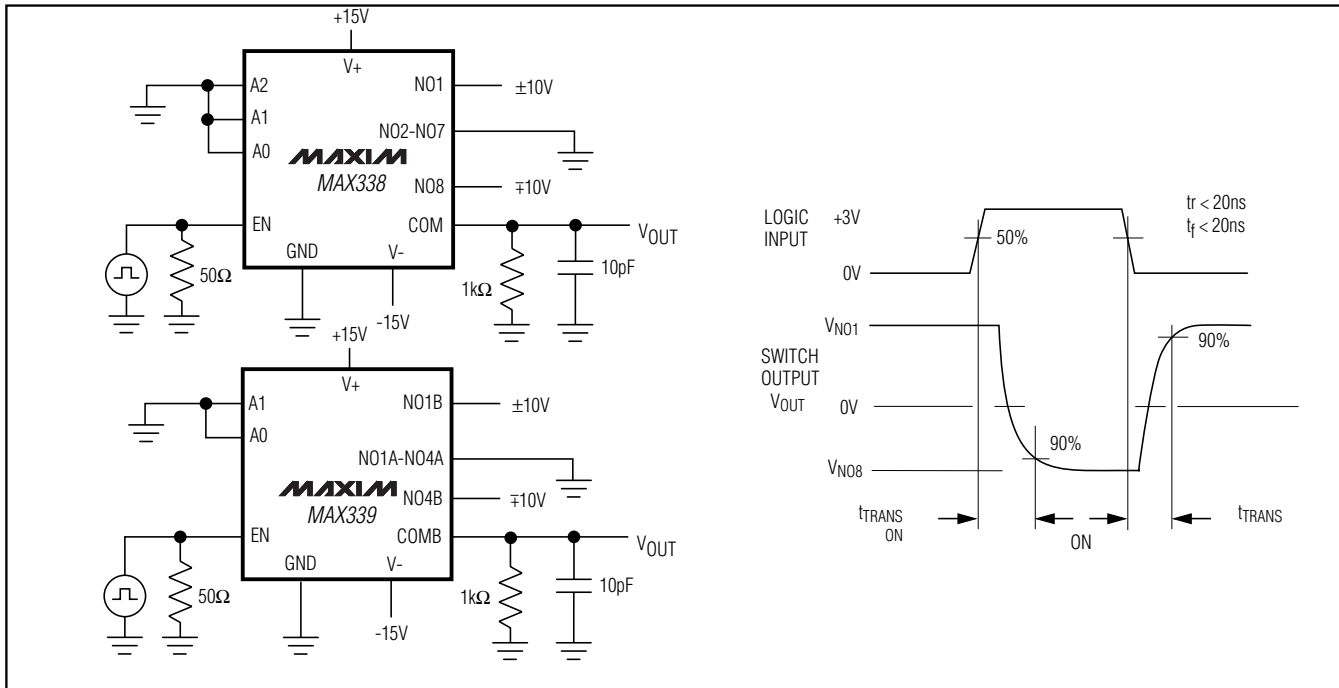


Figure 2. Transition Time

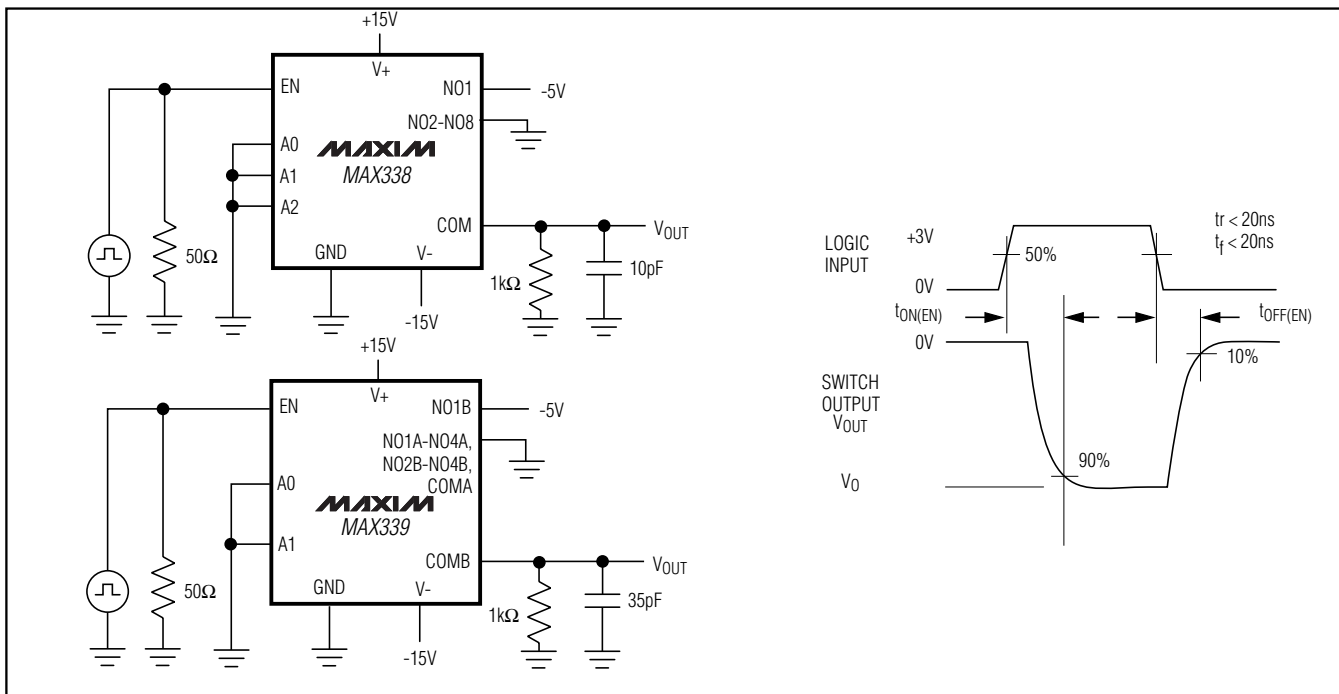


Figure 3. Enable Switching Time

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Test Circuits/Timing Diagrams (continued)

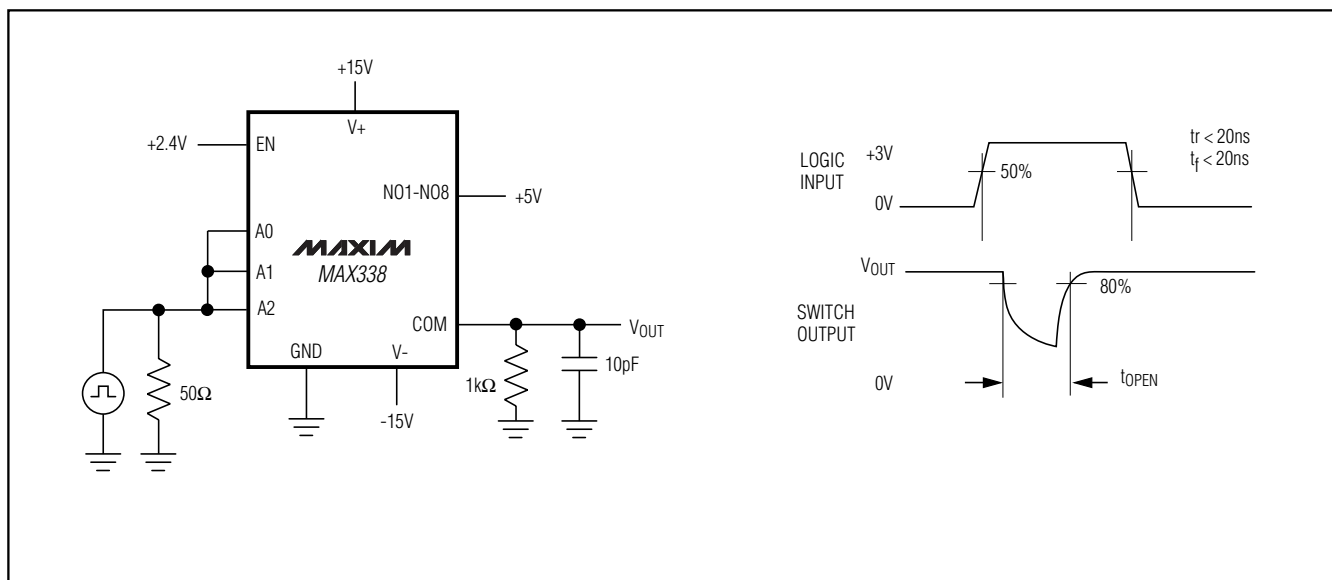


Figure 4. Break-Before-Make Interval

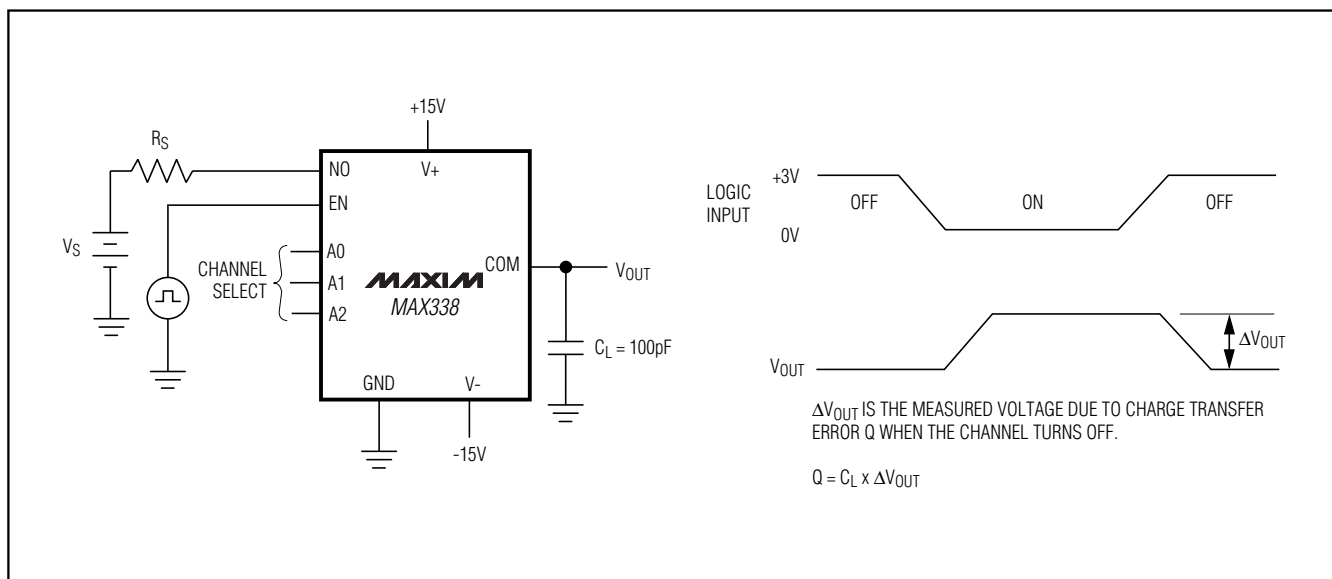


Figure 5. Charge Injection

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Test Circuits/Timing Diagrams (continued)

MAX338/MAX339

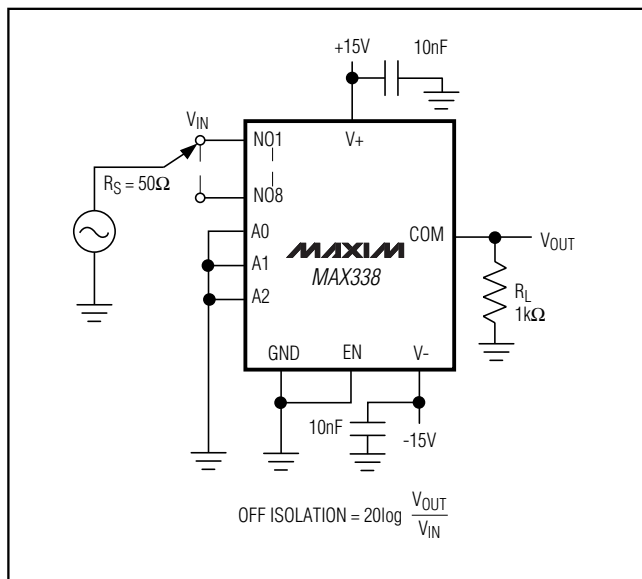


Figure 6. Off-Isolation

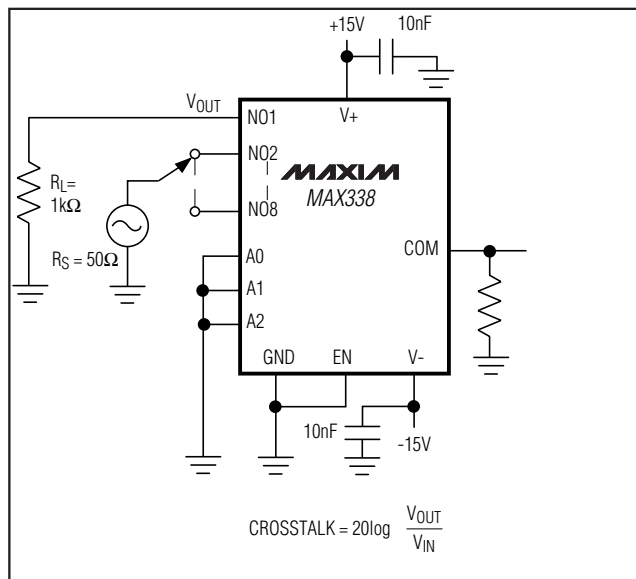


Figure 7. Crosstalk

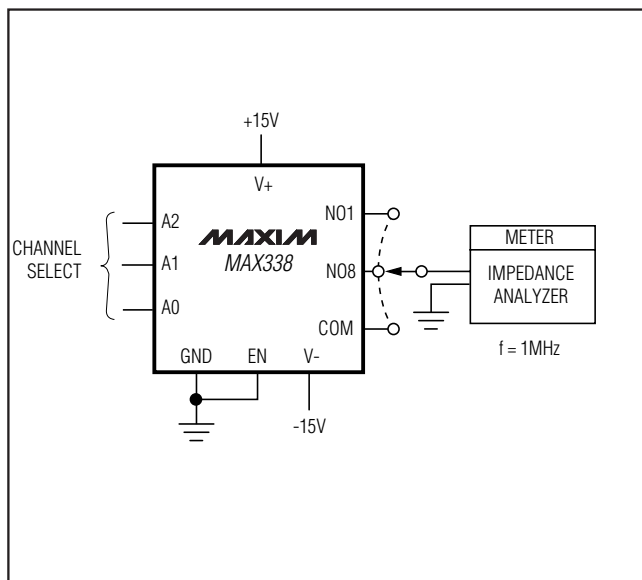
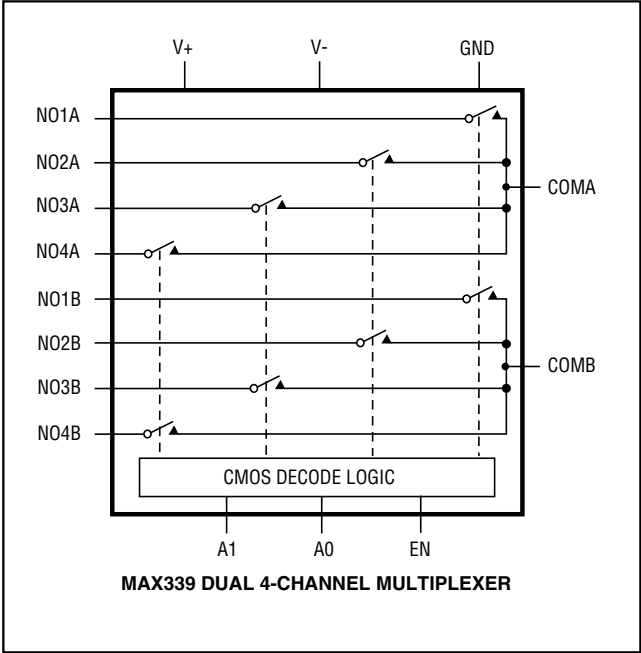
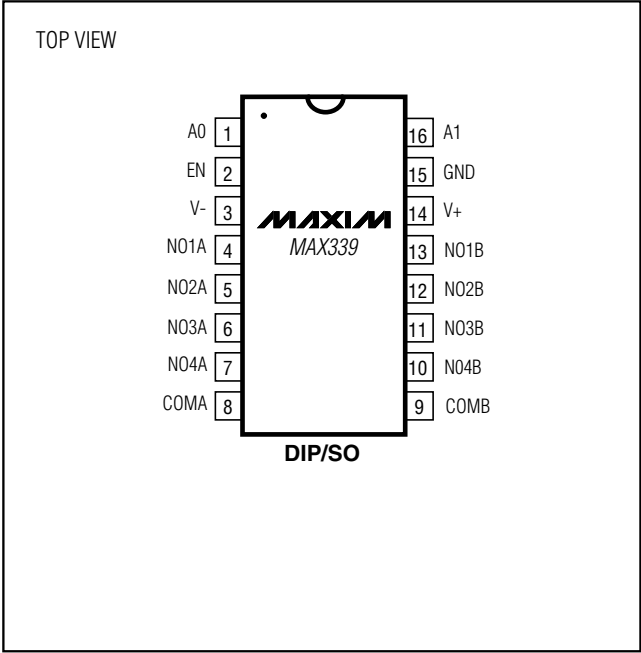


Figure 8. NO/COM Capacitance

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Pin Configurations/Functional Diagrams/Truth Tables (continued)



A2	A1	A0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAX338

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

MAX339

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

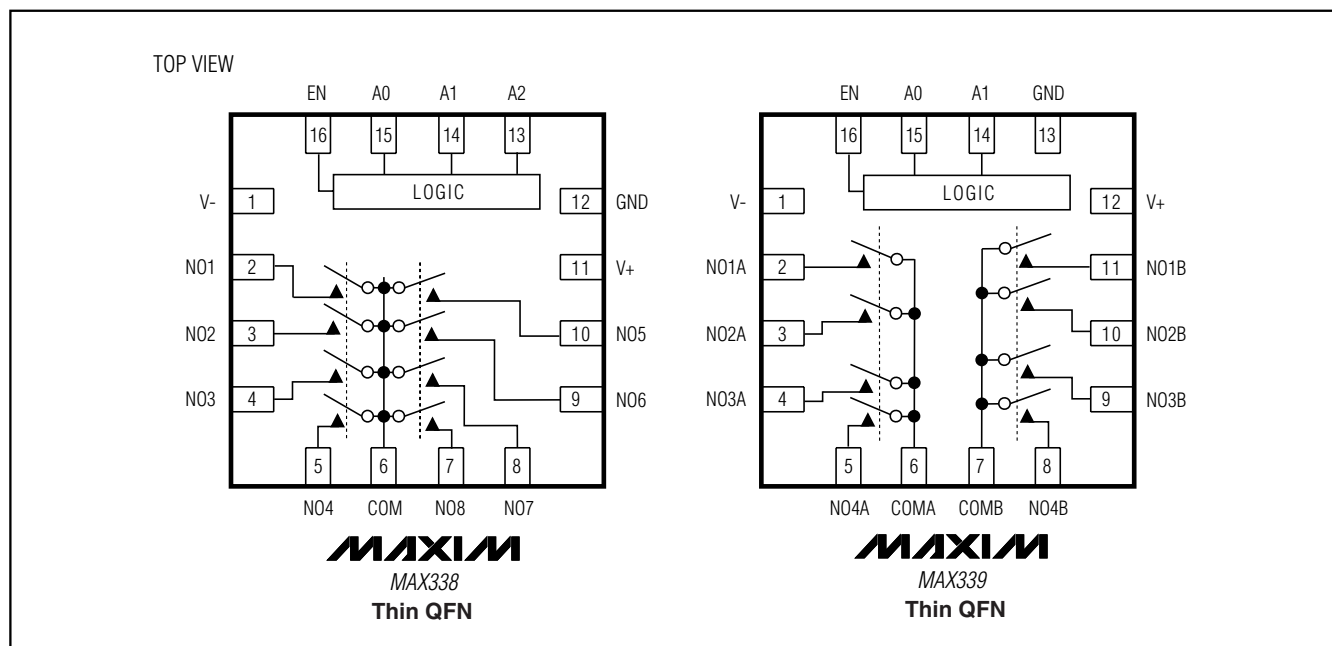
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX339CPE	0°C to +70°C	16 Plastic DIP
MAX339CSE	0°C to +70°C	16 Narrow SO
MAX339C/D	0°C to +70°C	Dice*
MAX339ETE	-40°C to +85°C	16 Thin QFN (5mm x 5mm)
MAX339EPE	-40°C to +85°C	16 Plastic DIP
MAX339ESE	-40°C to +85°C	16 Narrow SO
MAX339EJE	-40°C to +85°C	16 CERDIP
MAX339MJE	-55°C to +125°C	16 CERDIP**

*Contact factory for dice specifications.

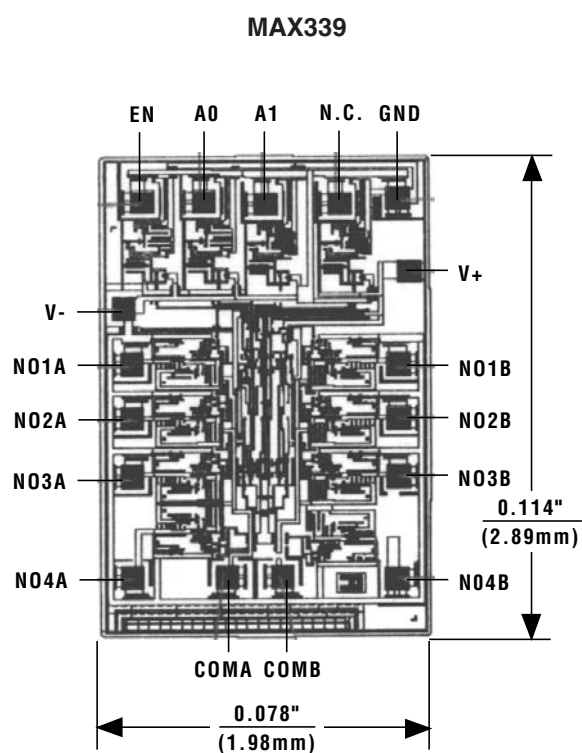
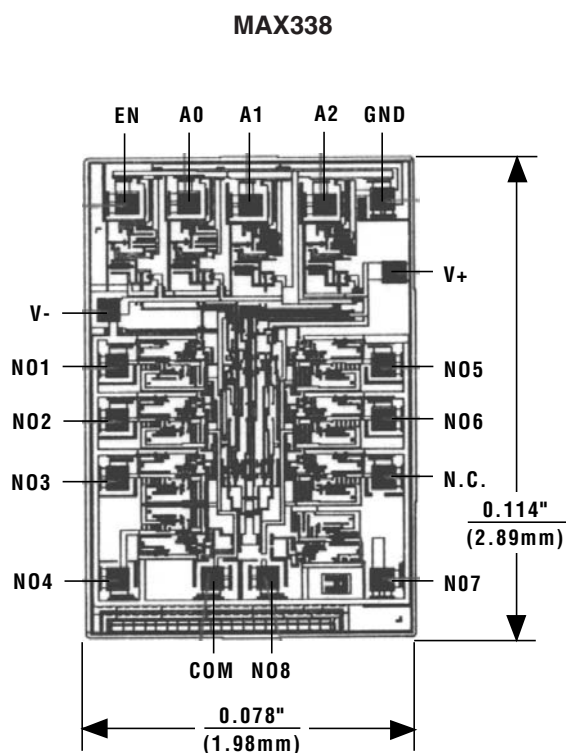
**Contact factory for availability.

Pin Configurations/Functional Diagrams/Truth Tables (continued)



8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Chip Topographies



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 224

SUBSTRATE IS INTERNALLY CONNECTED TO V+

Note: On Thin QFN packages connect exposed pad to V+.

TRANSISTOR COUNT: 224

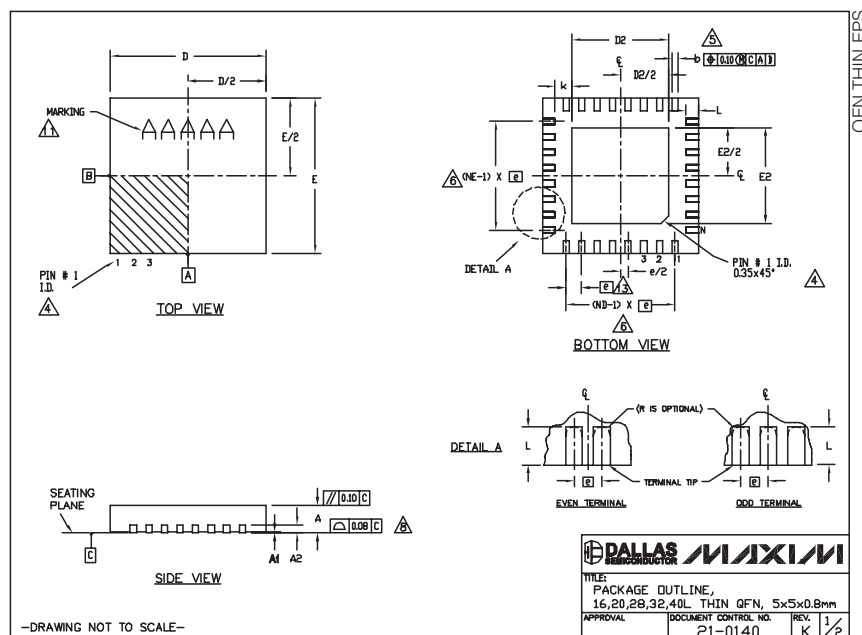
SUBSTRATE IS INTERNALLY CONNECTED TO V+

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX338/MAX339



COMMON DIMENSIONS												
PKG	16L	20L	28L	32L	40L	5x5	5x5	5x5	5x5	5x5	5x5	5x5
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20	REF.	0.20	0.20	REF.	0.20	0.20	REF.	0.20	0.20	REF.	0.20
b	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80	BSC.	0.65	BSC.	0.50	BSC.	0.50	BSC.	0.40	BSC.	0.40	BSC.
k	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16	20	28	32	40							
ND	4	5	7	8	10							
NE	4	5	7	8	10							
JEDEC	WHHB	WHHC	WHHD-1	WHHD-2	-----							

EXPOSED PAD VARIATIONS						
PKG CODES	DE			EE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055N-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-9	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2055-3, T2055-6, T4055-1 AND T4055-2.
- VARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.
	21-0140	K

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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