Low-Noise, 14V Input, 1A, PWM Step-Down Converters

ABSOLUTE MAXIMUM RATINGS

AIN to AGND .....-0.3 to +15V
IN to PGND .....-0.3V to (V_{AIN} + 0.3V)
LX to PGND .....-0.5V to (V_{IN} + 0.3V)
PGND to AGND .....±0.3V
$\overline{SHDN}$ to AGND .....-0.3V to (V_{AIN} + 0.3V)
ILIM/SS, FB, CC, BOOT, REF to AGND ....-0.3V to (V_{CVL} + 0.3V)
CVH to IN.....-6V to +0.3V
CVL, $\overline{STBY}$, SYNC/PWM to AGND.....-0.3V to +6V
Reference Current .....±1mA
CVL Current .....-1mA to +10mA
LX Peak Current (Internally Limited) 2.3A
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = 6V, $\overline{STBY}$ = SYNC/PWM = CVL, V_{BOOT} = V_{OUT}, FB = AGND, circuit of Figure 1, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range				2.7		14	V
Feedback Voltage	V_{FB}	V_{FB} = V_{OUT}, I_{LOAD} = 0 to 1A		1.238	1.251	1.264	V
Output Voltage (3.3V Mode)	V_{OUT}	FB = AGND, I_{LOAD} = 0 to 1A		3.296	3.333	3.368	V
Output Load Regulation		V_{FB} = V_{OUT}, I_{LOAD} = 0 to 1A			0.01		%
Output Current Capability		V_{IN} = 5V to 14V		1			A
Output Adjust Range		BOOT = AGND (Note 1)		V_{REF}		V_{IN}	V
FB Input Current	I_{FB}	V_{FB} = 1.4V		-50		50	nA
On-Resistance, P-Channel		High-side switch, I_{LX} = 1A	V_{IN} = 6V		0.24	0.5	Ω
			V_{IN} = 2.7V		0.34	0.8	
On-Resistance, N-Channel		Low-side switch, V_{IN} = 2.7V, I_{LX} = 200mA			3	8	Ω
Current Limit in PWM Mode	I_{LIM}			1.2	1.75	2.3	A
Pulse-Skipping Current Threshold		SYNC/PWM = low		285	380	475	mA
Current Limit in Low-Power Mode	I_{LIMLP}	$\overline{STBY}$ = low		285	380	475	mA
Current Limit, N-Channel		SYNC/PWM = high		0.15	0.4	0.9	A
Zero Crossing Threshold		SYNC/PWM = low	MAX1684	-10	50	100	mA
			MAX1685	20	80	130	
Quiescent Power Consumption		PWM mode, SYNC/PWM = high, V_{BOOT} = 3.3V (Note 2)	MAX1684		13	33	mW
			MAX1685		25	65	
		Normal mode, SYNC/PWM = low, V_{BOOT} = 3.3V (Note 2)			0.9	2	
		Low-power mode, $\overline{STBY}$ = low, V_{BOOT} = 3.3V (Note 2)			0.14	0.27	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = $V_{\overline{SHDN}}$ = 6V, $\overline{STBY}$ = SYNC/PWM = CVL, V_{BOOT} = V_{OUT}, FB = AGND, circuit of Figure 1, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current in Dropout		$\overline{STBY}$ = low, V_{IN} = 2.7V			230	430	µA
Shutdown Supply Current		$\overline{SHDN}$ = low			2	6	µA
LX Leakage Current	I_{LX}	V_{IN} = 14V, V_{LX} = 0 or 14V, $\overline{SHDN}$ = low				20	µA
Oscillator Frequency	f_{OSC}	MAX1684		260	300	340	kHz
		MAX1685		520	600	680	
SYNC Capture Range		MAX1684		180		350	kHz
		MAX1685		360		700	
Maximum Duty Cycle				100			%
Constant-Frequency Minimum Duty Cycle		(Note 3)	MAX1684		10		%
			MAX1685		20		
Reference Output Voltage	V_{REF}	I_{REF} = 0		1.238	1.251	1.264	V
Reference Load Regulation		-1µA < I_{REF} < 50µA			4	15	mV
Reference Supply Regulation		2.7V < V_{BOOT} < 5.5V			0.2	5	mV
CVL Regulator Output Voltage		V_{IN} = 3V to 14V, BOOT = AGND, I_{CVL} = 0 to 5mA		2.7	3.0	3.15	V
CVL Dropout Voltage		BOOT = AGND, I_{CVL} = 5mA				120	mV
CVL Undervoltage Lockout Threshold		BOOT = AGND, CVL falling edge, typical hysteresis is 40mV		2.35	2.5	2.6	V
CVH with Respect to V_{IN}		I_{CVH} = -1mA		-5.0	-4.6	-4.1	V
BOOT Switchover Threshold		BOOT falling edge, typical hysteresis is 0.1V		2.35	2.5	2.65	V
Thermal Shutdown Threshold		Typical hysteresis is +10°C (Note 4)			160		°C
ILIM/SS Source Current		$V_{ILIM/SS}$ = 1.4V		3.3	4	4.65	µA
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, $\overline{STBY}$, SYNC/PWM		2			V
Logic Input Low Voltage	V_{IL}					0.7	V
Logic Input Current		$\overline{SHDN}$, $\overline{STBY}$, SYNC/PWM		-1		1	µA
SYNC/PWM Pulse Width		High or low period		500			ns

Low-Noise, 14V Input, 1A, PWM Step-Down Converters

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = 6V, $\overline{STBY}$ = SYNC/PWM = CVL, V_{BOOT} = V_{OUT}, FB = AGND, circuit of Figure 1, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Voltage Range			2.7	14	V
Output Feedback Voltage	V_{FB}	V_{FB} = V_{OUT}, I_{LOAD} = 0 to 1A	1.233	1.269	V
Output Voltage (3.3V Mode)	V_{OUT}	FB = AGND, I_{LOAD} = 0 to 1A	3.280	3.382	V
Output Current Capability		V_{IN} = 6V to 14V	1		A
Output Adjust Range		BOOT = AGND (Note 1)	V_{REF}	V_{IN}	V
FB Input Current	I_{FB}	V_{FB} = 1.4V	-50	50	nA
Current Limit in PWM Mode	I_{LIM}		1.2	2.3	A
Current Limit in Low-Power Mode	I_{LIMLP}	$\overline{STBY}$ = low	285	475	mA
Quiescent Power Consumption		Normal mode, SYNC/PWM = low, V_{BOOT} = 3.3V (Note 2)		2	mW
		Low-power mode, $\overline{STBY}$ = low, V_{BOOT} = 3.3V (Note 2)		0.27	
Shutdown Supply Current		$\overline{SHDN}$ = low		6	µA
Oscillator Frequency	f_{OSC}	MAX1684	240	350	kHz
		MAX1685	480	700	
Reference Output Voltage		I_{REF} = 0	1.232	1.268	V
CVL Regulator Output Voltage		V_{IN} = 3V to 14V, BOOT = AGND, I_{CVL} = 0 to 5mA	2.7	3.15	V
CVL Undervoltage Lockout Threshold		BOOT = AGND, CVL falling edge, typical hysteresis is 40mV	2.4	2.6	V
CVH with Respect to V_{IN}		I_{CVH} = -1mA	-5.0	-4.1	V
BOOT Switchover Threshold		BOOT falling edge, typical hysteresis is 0.1V	2.35	2.65	V
ILIM/SS Source Current		$V_{ILIM/SS}$ = 1.4V	3.1	4.7	µA
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, $\overline{STBY}$, SYNC/PWM	2		V
Logic Input Low Voltage	V_{IL}			0.7	

Note 1: The output adjust range with BOOT connected to V_{OUT} is V_{REF} to 5.5V. Connect BOOT to AGND for V_{OUT} > 5.5V.

Note 2: The quiescent power-consumption specifications include chip supply and gate-drive loss only. Divide these values by V_{IN} (6V) to obtain quiescent currents. In normal and low-power modes, chip supply current dominates and quiescent power is proportional to V_{BOOT} (BOOT connected to OUT). In PWM mode, gate-drive loss dominates and quiescent power is proportional to V_{IN} × (V_{IN} - V_{CVH}). In addition, IR losses in power switches and external components typically increase PWM quiescent power consumption by 5mW to 10mW. Note that if the device is not bootstrapped, additional power is dissipated in the CVL linear regulator.

Note 3: When the duty factor (V_{OUT} / V_{IN}) is less than this value, the switching frequency decreases in PWM mode to maintain regulation.

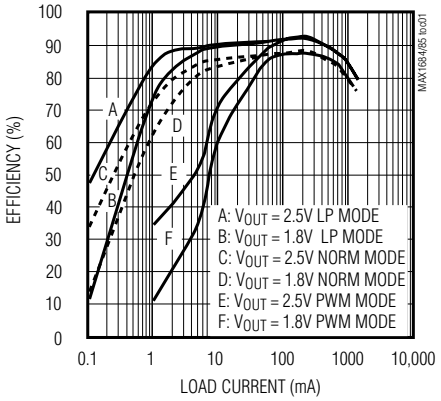
Note 4: Thermal shutdown is disabled in low-power mode ($\overline{STBY}$ = low) to reduce power consumption.

Note 5: Specifications to -40°C are guaranteed by design, not production tested.

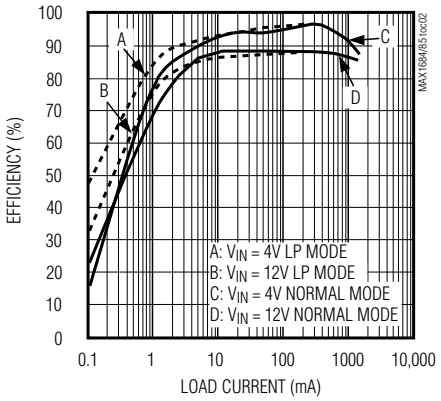
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

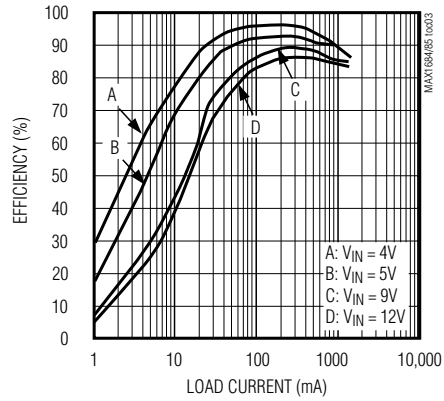
MAX1684
EFFICIENCY vs. LOAD CURRENT
(V_{IN} = 3.3V, V_{OUT} = 1.8V, 2.5V)



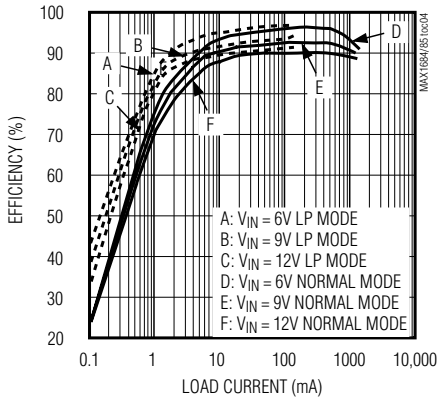
MAX1684
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



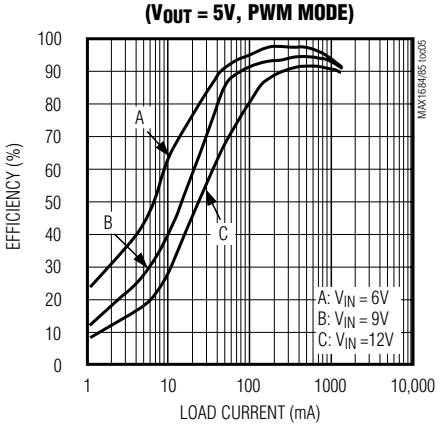
MAX1684
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V, PWM MODE)



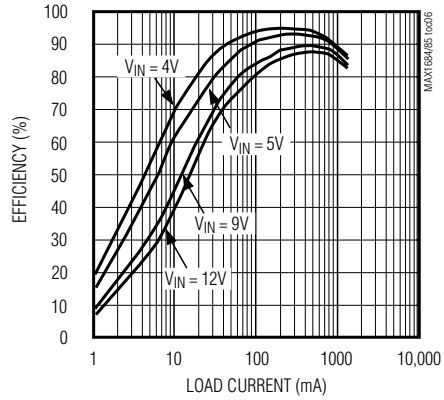
MAX1684
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V)



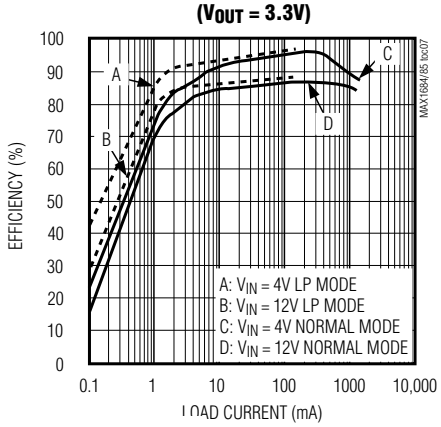
MAX1684
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V, PWM MODE)



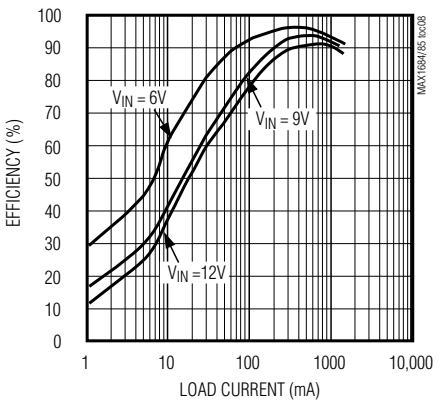
MAX1685
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V, PWM MODE)



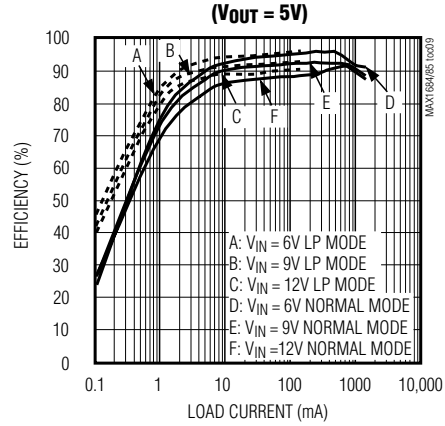
MAX1685
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 3.3V)



MAX1685
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V PWM MODE)



MAX1685
EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 5V)

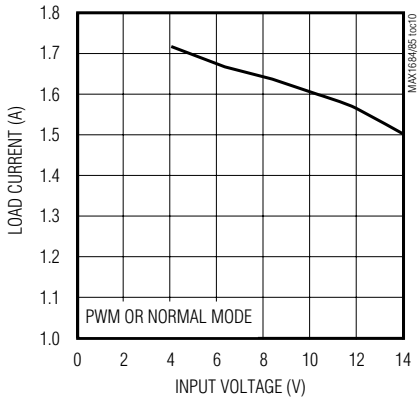


Low-Noise, 14V Input, 1A, PWM Step-Down Converters

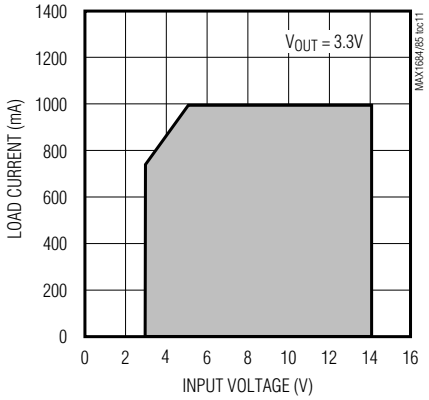
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

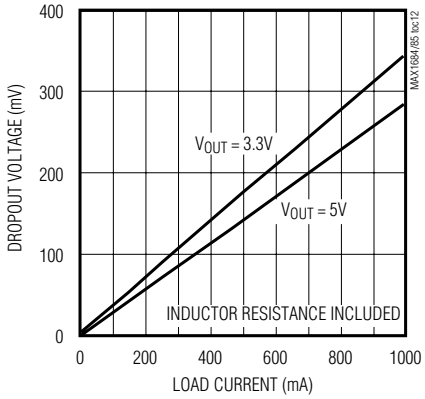
MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE



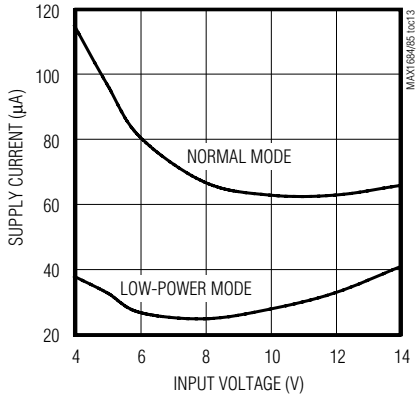
SAFE OPERATING AREA



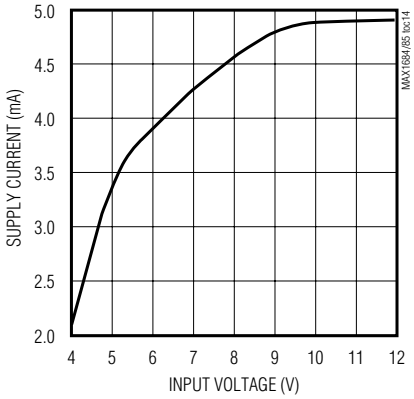
DROPOUT VOLTAGE vs. LOAD CURRENT



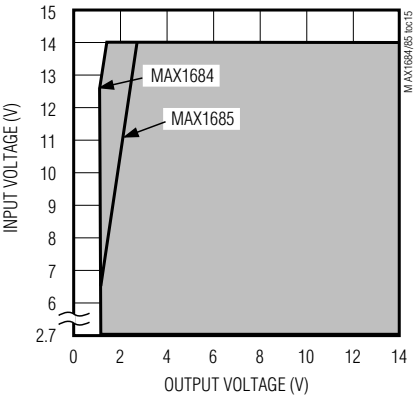
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



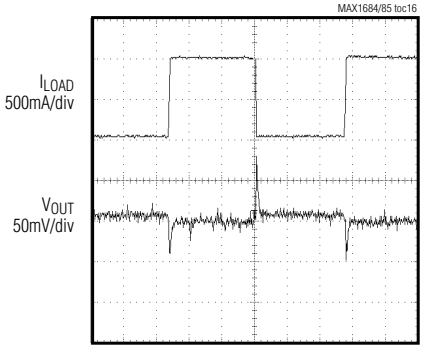
MAX1684 NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (V_{OUT} = 3.3V, PWM MODE)



PWM FIXED-FREQUENCY OPERATION AREA

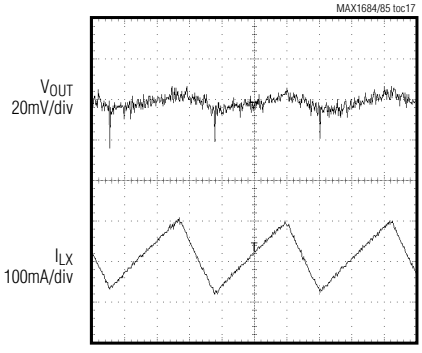


LOAD-TRANSIENT RESPONSE



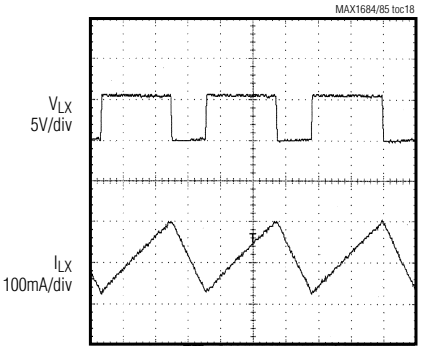
MAX1684, I_{LOAD} = 0.1mA TO 1A, V_{OUT} = 3.3V, V_{IN} = 5V, SYNC/PWM = 3.3V

SWITCHING WAVEFORM



MAX1684, I_{LOAD} = 100mA, V_{OUT} = 3.3V, V_{IN} = 5V, SYNC/PWM = 3.3V

SWITCHING WAVEFORM

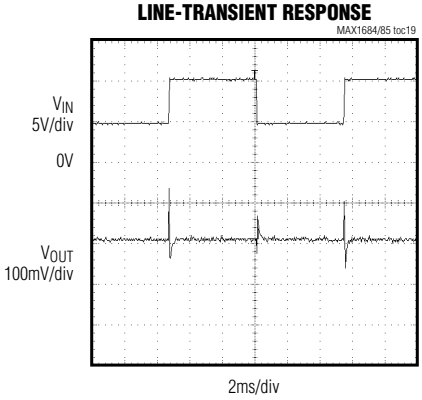


MAX1684, I_{LOAD} = 100mA, V_{OUT} = 3.3V, V_{IN} = 5V, SYNC/PWM = 3.3V

Typical Operating Characteristics (continued)

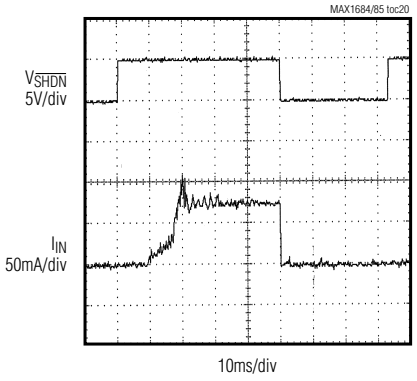
(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LINE-TRANSIENT RESPONSE



MAX1684, I_{LOAD} = 100mA, V_{IN} = 5V TO 10V, SYNC/PWM = 3.3V

STARTUP CURRENT



MAX1684, I_{LOAD} = 100mA, V_{OUT} = 3.3V, V_{IN} = 5V, $C_{ILIM/SS}$ = 0.1µF, SYNC/PWM = 3.3V

Pin Description

PIN	NAME	FUNCTION
1	CVH	High-Side MOSFET Gate Bias. Bias voltage for P-channel switch. Bypass to IN with a 0.1µF capacitor.
2	AIN	Analog Supply Voltage Input. Connect to IN with a 0.2in metal trace. Bypass to PGND with a 0.1µF capacitor.
3	IN	Supply Voltage Input
4	CVL	Logic Supply Voltage Output and IC Logic Supply. Sources 5mA for external loads. Bypass to AGND with 1µF capacitor.
5	AGND	Analog Ground
6	REF	Reference Output. 1.25V reference output supplies 10µA for external loads. Bypass to AGND with 0.1µF capacitor.
7	FB	Dual-Mode Feedback Input. Connect FB to V_{OUT} for 1.25V output. Connect to an external resistor divider to adjust the output voltage. Connect to AGND to set output voltage to 3.3V.
8	CC	Integrator Capacitor Connection. Connect a 0.01µF capacitor to AGND.
9	SYNC/PWM	SYNC/PWM Input: For synchronized-PWM operation, drive with TTL level, 50% square wave. Connect to CVL for PWM mode. Connect to AGND for normal mode.
10	ILIM/SS	Current-Limit Adjust/Soft-Start Input. See the *Current Limit and Soft-Start* section.
11	$\overline{STBY}$	Standby Control Input. Connect to CVL for normal operation. Connect to AGND for low-power mode (Table 1). This pin overrides SYNC/PWM setting.
12	BOOT	Bootstrap Input. Connection for the bootstrap switch and internal feedback path. Connect BOOT to V_{OUT} for V_{OUT} < 5.5V. Connect BOOT to AGND for V_{OUT} > 5.5V.
13, 14	LX	Inductor Connection. Drain for internal P-channel MOSFETs. Connect inductor from LX to OUT.
15	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to ground for shutdown. $\overline{SHDN}$ can withstand the input voltage.
16	PGND	Power Ground

Low-Noise, 14V Input, 1A, PWM Step-Down Converters

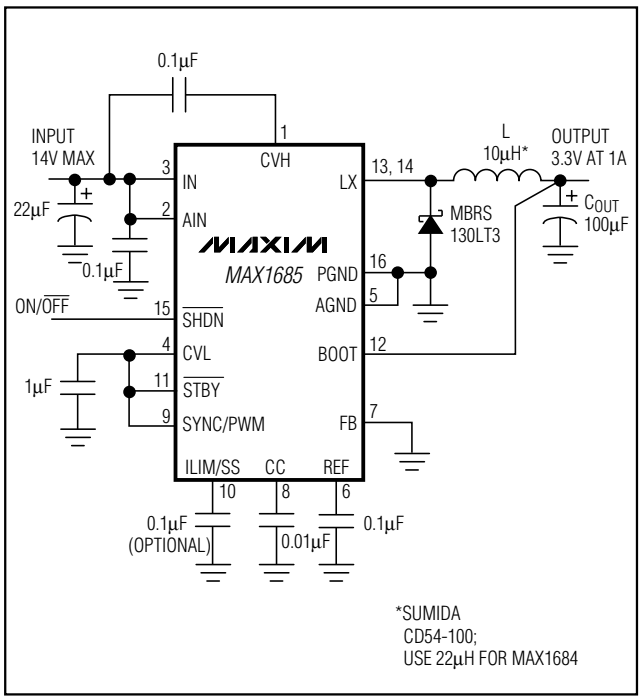


Figure 1. Standard Application Circuit

Detailed Description

The MAX1684/MAX1685 step-down, PWM DC-DC converters provide an adjustable output from 1.25V to the input voltage. They accept inputs from 2.7V to 14V and deliver up to 1.6A. An internal MOSFET and synchronous rectifier reduce PC board area while maintaining high efficiency. Operation with up to 100% duty cycle minimizes dropout voltage. Fixed-frequency PWM operation reduces interference in sensitive communications and data-acquisition applications. A SYNC input allows synchronization to an external clock. The MAX1684/MAX1685 can operate in five modes. Setting the devices to operate in the appropriate mode for the intended application (Table 1) achieves highest efficiency.

PWM Control

The MAX1684/MAX1685 use an oscillator-triggered minimum/maximum on-time current-mode control scheme (Figure 2). The minimum on-time is typically 220ns unless the regulator is in dropout. The maximum on-time is 2 / f_{OSC}, allowing operation to 100% duty cycle. Current-mode feedback provides cycle-by-cycle current limiting for superior load- and line-transient response.

At each falling edge of the internal oscillator, the internal P-channel MOSFET (main switch) turns on. This allows current to ramp up through the inductor to the load and stores energy in a magnetic field. The switch remains on until either the current-limit comparator trips, the maximum on-time expires, or the PWM comparator signals that the output is in regulation. When the switch turns off during the second half of each cycle, the inductor's magnetic field collapses, releasing the stored energy and forcing current through the output diode to the output filter capacitor and load. The output filter capacitor stores charge when the inductor current is high and releases it when the inductor current is low, smoothing the voltage across the load.

During normal operation, the MAX1684/MAX1685 regulate the output voltage by switching at a constant frequency and modulating the power transferred to the load on each cycle using the PWM comparator. A multi-input comparator sums three weighted differential signals (the output voltage with respect to the reference, the main switch current sense, and the slope-compensation ramp) and changes states when a threshold is reached. It modulates output power by adjusting the

Table 1. Operating Modes

MODE	SYNC/PWM	$\overline{\text{STBY}}$	$\overline{\text{SHDN}}$	FUNCTION	TYPICAL OUTPUT CAPABILITY (A)
PWM	H	H	H	Fixed-frequency PWM	1.6
Sync PWM	Clocked	H	H	Fixed-input clock-frequency PWM	1.6
Normal	L	H	H	PFM at light loads (<150mA); fixed-frequency PWM at heavy loads (>150mA)	1.6
Low Power	X	L	H	Low-power or standby mode	160m
Shutdown	X	X	L	Circuit disabled	0

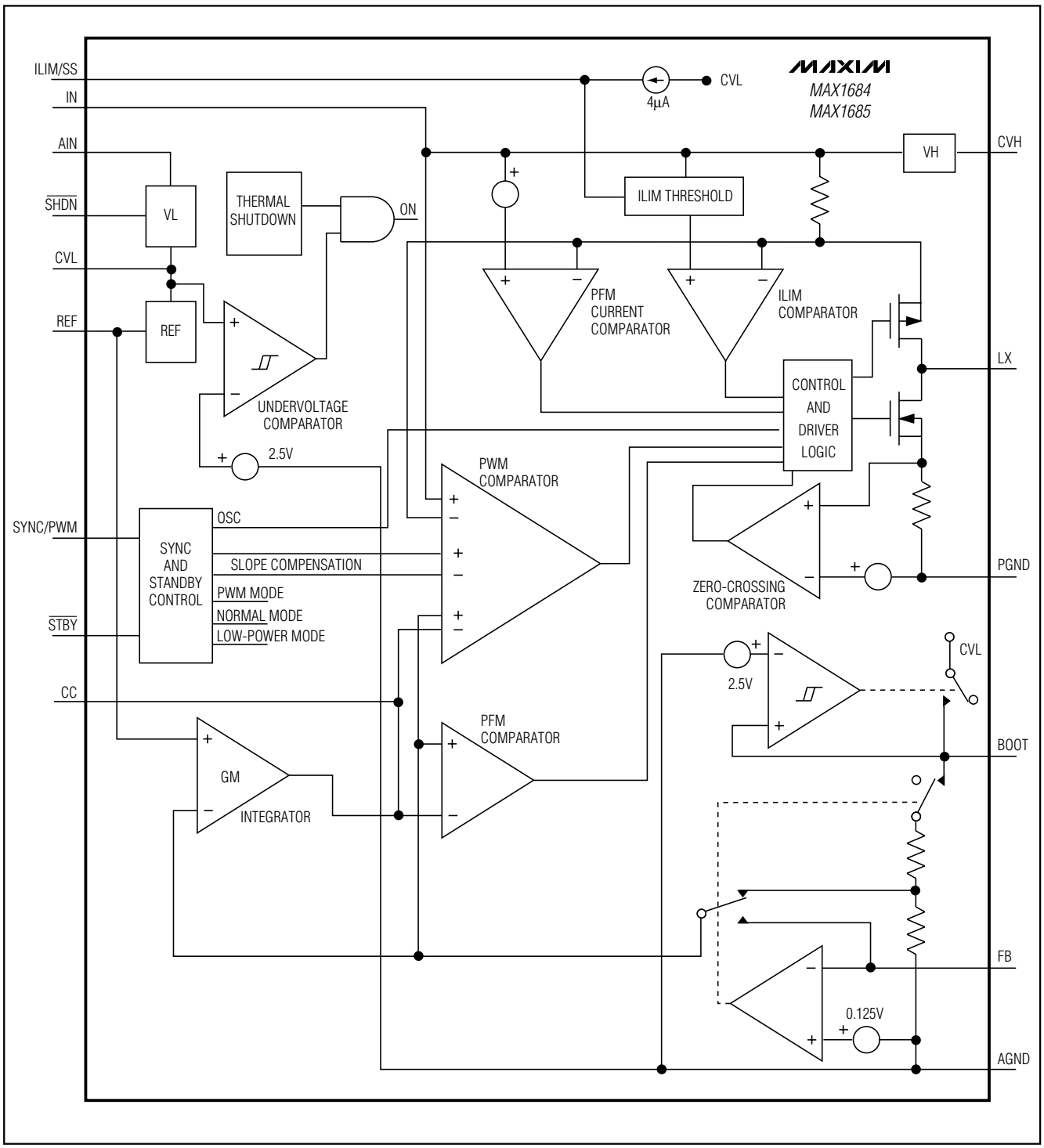


Figure 2. Functional Diagram

Low-Noise, 14V Input, 1A, PWM Step-Down Converters

inductor peak current during the first half of each cycle, based on the output error voltage. The MAX1684/MAX1685s' loop gain is relatively low to enable the use of a small, low-value output filter capacitor. The 1.4% transient load regulation from 0 to 1A is compensated by an integrator circuit that lowers DC load regulation to 0.01% typical. Slope compensation accounts for the inductor-current waveform's down slope during the second half of each cycle, and eliminates the inductor-current staircasing characteristic of current-mode controllers at high duty cycles.

PFM Control

In low-power mode, the MAX1684/MAX1685 switch only as needed to service the load. This reduces the switching frequency and associated losses in the P-channel switch, the synchronous rectifier, and the external inductor. During this PFM operation, a switching cycle initiates when the PFM comparator senses that the output voltage has dropped too low. The P-channel MOSFET switch turns on and conducts current to the output-filter capacitor and load. The MAX1684/MAX1685 then wait until the PFM comparator senses a low-output voltage again.

In normal mode at light load (<150mA), the device also operates in PFM. The PFM current comparator controls both entry into PWM mode and the peak switch current during PFM operation. Consequently, some jitter is normal during transition from PFM to PWM with loads around 150mA, and it has no adverse impact on regulation.

100% Duty-Cycle Operation

As the input voltage drops, the duty cycle increases until the P-channel MOSFET turns on continuously, achieving 100% duty cycle. Dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal switch and inductor, approximately 0.35V (I_{OUT} = 1A).

Very Low Duty-Cycle Operation

Because of the P-channel minimum on-time and dead-time (duration when both switches are off), the MAX1684/MAX1685s' switching frequency must decrease in PWM or normal mode to maintain regulation at a very low duty cycle. The total P-channel on-time and dead-time is 290ns typical. As a result, the MAX1684/MAX1685 maintain fixed-frequency regulation at no load for V_{IN} up to $10V_{OUT}$ and $5V_{OUT}$, respectively (see PWM Fixed-Frequency Operation Area graph in the *Typical Operating Characteristics*).

For higher V_{IN} at no load, the frequency decreases based on the following equation:

$$f = V_{OUT} / (V_{IN} \times 290ns)$$

At medium- to full-load current (>100mA), V_{IN} can increase slightly higher before the frequency decreases.

Synchronous Rectification

Although the primary rectifier is an external Schottky diode, a small internal N-channel synchronous rectifier allows PWM operation at light loads. During the second half of each cycle, when the inductor current ramps below the zero-crossing threshold or when the oscillator period ends, the synchronous rectifier turns off. This keeps excess current from flowing backward through the inductor. Choose an appropriate inductor to limit the PWM ripple current through the N-channel FET to $400mA_{P-P}$.

Current Limit and Soft-Start

The voltage at ILIM/SS sets the PWM current limit (I_{LIM} = 1.75A) and the low-power current limit (I_{LIMLP} = 380mA). The PWM current limit applies when the device is in PWM mode, in synchronized PWM mode, or delivering a heavy load in normal mode (Table 1). The I_{LIMLP} limit applies when the device is in low-power mode. An internal 4µA current source pulls ILIM/SS up to CVL. To use the maximum current-limit thresholds, leave ILIM/SS unconnected or connect it to a soft-start capacitor. Connect an external resistor from ILIM/SS to AGND to adjust the current-limit thresholds.

The PWM current-limit threshold is ($I_{LIM} \times R_{ILIM/SS} \times 4\mu A$) / V_{REF} and is adjustable from 0.5A to 1.75A.

The low-power current-limit threshold is equal to ($I_{LIMLP} \times R_{ILIM/SS} \times 4\mu A$) / V_{REF} and is adjustable from 110mA to 380mA.

For example, when $R_{ILIM/SS}$ is 156kΩ, the PWM current limit threshold is 0.88A and the low-power current limit threshold is 0.19A.

Connect a low-value capacitor from ILIM/SS to AGND to achieve soft-start, limiting inrush current. ILIM/SS internally shorts to AGND in shutdown to discharge the soft-start capacitor. Do not connect ILIM/SS to REF or CVL. Determine the soft-start duration by:

$$t_{SOFT-START} = C_{ILIM/SS}(1.25V / 4\mu A)$$

where $t_{SOFT-START}$ is the time from SHDN going high to the regulator being able to supply full load current. For example, a 0.1µF capacitor yields 31ms of soft-start.

The output current capability for each mode is determined by the following equations:

$I_{OUTMAX} = I_{LIM} - 0.5 \times I_{RIPPLE}$ (for PWM and normal modes)

$I_{OUTMAX} = 0.5 \times I_{LIMLP}$ (for low-power mode)

where:

I_{RIPPLE} = ripple current = $(V_{IN} - V_{OUT}) \times V_{OUT} / (V_{IN} \times f_{OSC} \times L)$

I_{LIM} = current limit in PWM mode

I_{LIMLP} = current limit in low-power mode

Internal Low-Voltage Regulators and Bootstrap (BOOT)

The MAX1684/MAX1685 have two internal regulators (VH and VL) that generate low-voltage supplies for internal circuitry (see the *Functional Diagram*). The VH regulator generates -4.6V with respect to IN to supply the P-channel switch and driver. Bypass CVH to IN with a 0.1µF capacitor. The VL regulator generates a 3V output at CVL to supply internal low-voltage blocks, as well as the N-channel switch and driver. Bypass CVL to AGND with a 1µF capacitor.

To reduce the quiescent current in low-power and normal modes, connect BOOT to OUT. After startup, when V_{BOOT} exceeds 2.6V, the internal bootstrap switch connects CVL to BOOT. This bootstrap mechanism causes the internal circuitry to be supplied from the output and thereby reduces the input quiescent current by a factor of V_{OUT} / V_{IN}. Do not connect BOOT to OUT if the output voltage exceeds 5.5V. Instead, connect BOOT to AGND to keep CVL regulated at 3V.

CVL has a 5mA capability to supply external logic circuitry and is disabled in shutdown mode.

Applications Information

Output Voltage Selection

Connect FB to AGND to select the internal 3.3V output mode. Connect BOOT to OUT in this configuration.

To select an output voltage between 1.25V and V_{IN}, connect FB to a resistor voltage-divider between the output and AGND (Figure 3). Select R2 in the 20kΩ to 100kΩ range. Calculate R1 as follows:

$$R1 = R2 [(V_{OUT} / V_{FB}) - 1]$$

where V_{FB} = 1.25V.

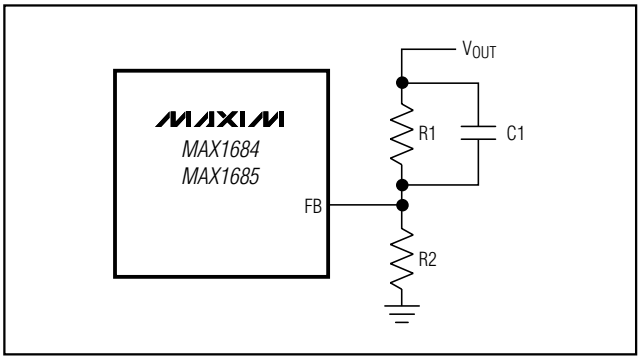


Figure 3. Setting Output Voltage

Connect a small capacitor across R1 to compensate for stray capacitance at the FB pin:

$$C1 = \frac{5 (10^{-7})}{R_2}$$

where: R2 = 100kΩ, use 4.7pF.

Inductor Selection

The MAX1684/MAX1685s' high switching frequency allows the use of small surface-mount inductors. Table 2 shows a selection of suitable inductors for different output voltage ranges. Calculate the minimum inductor by:

$$L = 0.9(V_{OUT} - 0.3V) / (I_{RIPPLE\ MAX} \times f_{OSC})$$

where:

$I_{RIPPLE\ MAX}$ = should be less than or equal to 400mA

f_{OSC} = 300kHz (MAX1684) or 600kHz (MAX1685)

Capacitor Selection

Select input and output filter capacitors to service inductor currents while minimizing voltage ripple. The input filter capacitor reduces peak currents and noise at the voltage source. The MAX1684/MAX1685s' loop gain is relatively low to enable the use of small, low-value output filter capacitors. Higher capacitor values provide improved output ripple and transient response.

Low-ESR capacitors are recommended. Capacitor ESR is a major contributor to output ripple (usually more than 60%). Avoid ordinary aluminum electrolytic capacitors, as they typically have high ESR. Low-ESR aluminum electrolytic capacitors are acceptable and relatively inexpensive. Low-ESR tantalum capacitors are better and provide a compact solution for space-constrained surface-mount designs. Do not exceed the ripple-current ratings of tantalum capacitors. Ceramic capacitors offer the lowest ESR overall. Sanyo OS-CON

Low-Noise, 14V Input, 1A, PWM Step-Down Converters

capacitors have the lowest ESR of the high-value electrolytic types. Use ceramic and OS-CON capacitors for very compact, high-reliability, or wide-temperature applications, where expense is justified. When using very low ESR capacitors, such as ceramic or OS-CON, check for stability while examining load-transient response, and increase the output compensation capacitor if needed. Table 3 lists suppliers for the various components used with the MAX1684/MAX1685.

Ensure that the minimum capacitance value and maximum ESR values are met:

$$C_{OUT} > I_{OUT\ MAX} / (V_{OUT} \times \text{AC Load Reg} \times f_{OSC})$$

$$R_{ESR} < 2 \times \text{AC Load Reg} \times V_{OUT}/I_{OUT\ MAX}$$

where $I_{OUT\ MAX}$ = 1A, AC Load Reg ≅ 1.4%, and f_{OSC} = 300kHz (MAX1684) or 600kHz (MAX1685).

Output Diode Selection

Use a 1A external Schottky diode (MBRS130LT3 or equivalent) for the output rectifier to pass inductor current during the start of the second half of each cycle. This diode operates before the internal N-channel MOSFET completely turns on and during high-current operation. Use a Schottky diode to avoid forward biasing the internal body diode of the N-channel MOSFET.

Table 2. Inductor and Minimum Output Capacitor Selection

V_{OUT} (V)	MAX1684 (300kHz)		MAX1685 (600kHz)	
	L (µH)	MIN C_{OUT} (µF)	L (µH)	MIN C_{OUT} (µF)
1.25 to 2.7	22	220	10	100
2.7 to 4	22	100	10	47
4 to 6	47	68	22	33
6 to 14	68	47	33	22

Table 3. Component Suppliers

SUPPLIER	PHONE	FAX
CAPACITORS		
AVX	803-946-0690	803-626-3123
Matsuo	714-969-2591	714-960-6492
Sanyo	619-661-6835	619-661-1055
Sprague	603-224-1961	603-224-1430
INDUCTORS		
Coilcraft	847-639-6400	847-639-1469
Murata-Erie	814-237-1431	814-238-0490
Sumida	847-956-0666	847-956-0702
TDK	847-390-4373	847-390-4428
DIODES		
Motorola	602-303-5454	602-994-6430

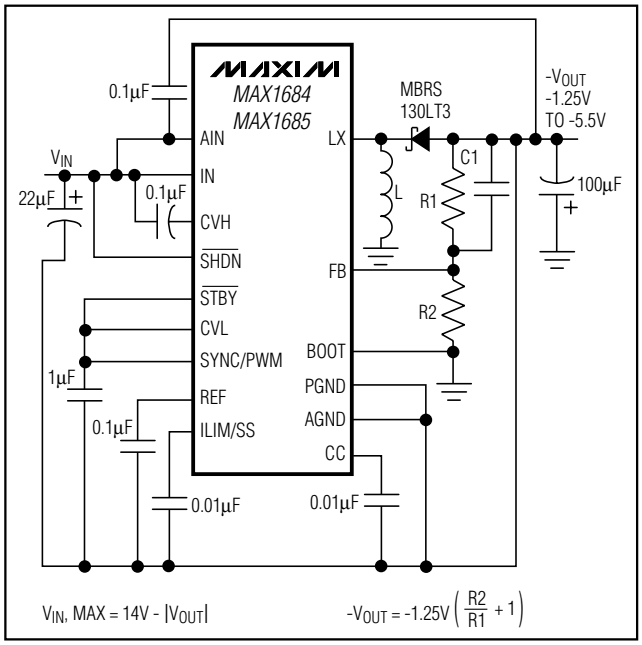


Figure 4. Inverting Output

Inverting Output

Interchanging the ground and V_{OUT} connections yields a negative voltage supply (Figure 4). The component selections are the same as for a positive voltage converter. The absolute maximum ratings limit the output voltage range to -1.25V to -5.5V and the maximum input voltage range to 14V - $|V_{OUT}|$.

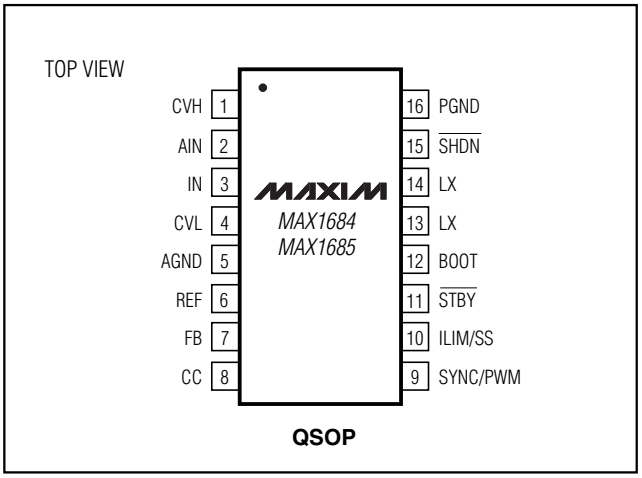
PC Board Layout

High switching frequencies and large peak currents make PC board layout a very important part of design. Poor design can result in excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which result in instability or regulation errors. Power components such as the MAX1684/MAX1685 inductor, input filter capacitor, and output filter capacitor should be placed as close together as possible, and their traces kept short, direct, and wide, Connect their ground nodes in a star-ground configuration. Keep the extra copper on the board and integrate into ground as a pseudo-ground plane.

When using external feedback, the feedback network should be close to FB, within 0.2 inch (5mm), and the output voltage feedback should be tapped as close to the output capacitor as possible. Keep noisy traces, such as those from LX, away from the voltage feedback network. Separate the noisy traces by grounded copper. Place the small bypass capacitors within 0.2 inch (5mm) of their respective inputs. The MAX1684 evaluation kit manual illustrates an example PC board layout, routing, and pseudo-ground plane.

Connect AIN to IN with a short (0.2 inch) metal trace or a 1Ω resistor and bypass AIN to PGND with a 0.1µF capacitor. This acts as a lowpass filter to reduce noise at AIN.

Pin Configuration



Chip Information

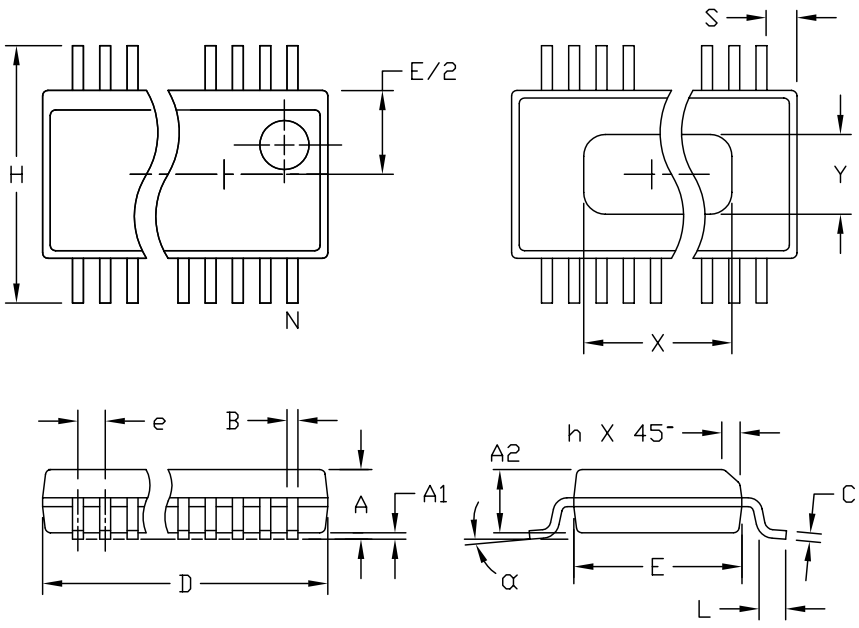
TRANSISTOR COUNT: 2061

Low-Noise, 14V Input, 1A, PWM Step-Down Converters

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1