2A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN to GND .....-0.3V to +6V
IN to V_{CC}.....±0.3V
GND to PGND.....±0.3V
All Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
LX Current (Note 1).....±3.75A
REF Short Circuit to GND Duration .....Continuous
ESD Protection.....±2kV

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 16.7mW/°C above +70°C;
part mounted on 1 in.^{2} of 1oz. copper).....1.2W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Preset Output Voltage	V_{OUT}	I_{LOAD} = 0 to 2A, V_{FB} = V_{OUT}	V_{IN} = V_{CC} = 4V to 5.5V, FBSEL = unconnected	3.300	3.333	3.366	V
			V_{IN} = V_{CC} = 3V to 5.5V, FBSEL = V_{CC}	2.500	2.525	2.550	
			V_{IN} = V_{CC} = 3V to 5.5V, FBSEL = REF	1.089	1.100	1.111	
Adjustable Output Voltage Range		V_{IN} = V_{CC} = 3V to 5.5V, I_{LOAD} = 0, FBSEL = GND or REF		V_{REF}		V_{IN}	V
AC Load Regulation Error		FBSEL = GND			1		%
		FBSEL = REF, V_{CC}, or unconnected			2		
DC Load Regulation Error		FBSEL = GND			0.2		%
		FBSEL = REF, V_{CC}, or unconnected			0.4		
Dropout Voltage	V_{DO}	V_{IN} = V_{CC} = 3V, I_{LOAD} = 1A, FBSEL = V_{CC}				200	mV
Reference Voltage	V_{REF}			1.089	1.100	1.111	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -1µA to +10µA			0.5	1	mV
PMOS Switch On-Resistance	$R_{ON, P}$	I_{LX} = 0.5A	V_{IN} = 4.5V		70	150	mΩ
			V_{IN} = 3V		100	200	
NMOS Switch On-Resistance	$R_{ON, N}$	I_{LX} = 0.5A	V_{IN} = 4.5V		70	150	mΩ
			V_{IN} = 3V		100	200	
Current-Limit Threshold	I_{LIMIT}			2.5	2.9	3.3	A
RMS LX Output Current						2.5	A
Idle Mode Current Threshold	I_{IM}			0.25	0.45	0.65	A
Switching Frequency	f	(Note 2)				350	kHz
No-Load Supply Current	I_{IN} + I_{CC}	V_{FB} = 1.2V			240	360	µA
Shutdown Supply Current	$I_{CC(SHDN)}$	$\overline{SHDN}$ = GND			<1	3	µA
PMOS Switch Off-Leakage Current	I_{IN}	$\overline{SHDN}$ = GND				15	µA
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			150		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling, hysteresis = 40mV	2.5	2.6	2.7	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V	0	80	200	nA
Off-Time Default Period	t_{OFF}	R_{TOFF} = 150kΩ	1.13	1.33	1.53	µs
		R_{TOFF} = 30.1kΩ	0.20	0.33		
		R_{TOFF} = 499kΩ		4.3	5.6	
Off-Time Start-Up Period	t_{OFF}	FB = GND		4 • t_{OFF}		µs
On-Time Period	t_{ON}		0.4			µs
SS Source Current	I_{SS}		3.5	5	6.5	µA
SS Sink Current	I_{SS}	V_{SS} = 1V	100			µA
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0 to V_{CC}	-0.5		0.5	µA
$\overline{SHDN}$ Input Low Threshold	V_{IL}				0.8	V
$\overline{SHDN}$ Input High Threshold	V_{IH}		2.0			V
FBSEL Input Current			-5		+5	µA
FBSEL Logic Thresholds		FBSEL = GND			0.2	V
		FBSEL = REF	0.9		1.3	
		FBSEL = unconnected	0.7 • V_{CC} - 0.2		0.7 • V_{CC} + 0.2	
		FBSEL = V_{CC}	V_{CC} - 0.2			
Maximum Output RMS Current					5.8	A_{RMS}

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{CC} = +3.3V, FBSEL = GND, **T_A = -40°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}			3.0		5.5	V
Preset Output Voltage	V_{OUT}	I_{LOAD} = 0 to 2A, V_{FB} = V_{OUT}	V_{IN} = V_{CC} = 4V to 5.5V, FBSEL = unconnected	3.276		3.390	V
			V_{IN} = 3V to 5.5V, FBSEL = V_{CC}	2.48		2.57	
			V_{IN} = 3V to 5.5V, FBSEL = REF	1.08		1.12	
Adjustable Output Voltage		V_{IN} = 3.0V to 5.5V, I_{LOAD} = 0, FBSEL = GND or REF		V_{REF}		V_{IN}	V
Reference Voltage	V_{REF}			1.08		1.12	V
PMOS Switch On-Resistance	$R_{ON, P}$	I_{LX} = 0.5A	V_{IN} = 4.5V			150	mΩ
			V_{IN} = 3V			200	
NMOS Switch On-Resistance	$R_{ON, N}$	I_{LX} = 0.5A	V_{IN} = 4.5V			150	mΩ
			V_{IN} = 3V			200	
Current-Limit Threshold	I_{LIMIT}			2.3		3.5	A
Idle Mode Current Threshold	I_{IM}			0.2		0.7	A
No-Load Supply Current	I_{IN} + I_{CC}	V_{FB} = 1.2V				360	µA
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V		0		250	nA
Off-Time Default Period	t_{OFF}	R_{TOFF} = 150kΩ		1.03		1.63	µs

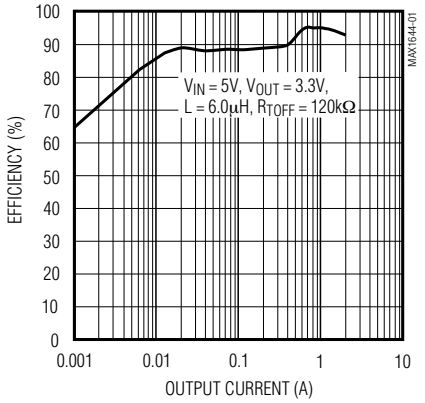
Note 2: Recommended operating frequency, not production tested.
Note 3: Specifications from 0°C to -40°C are guaranteed by design, not production tested.

2A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

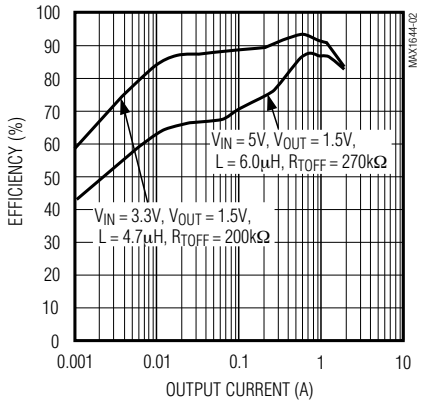
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

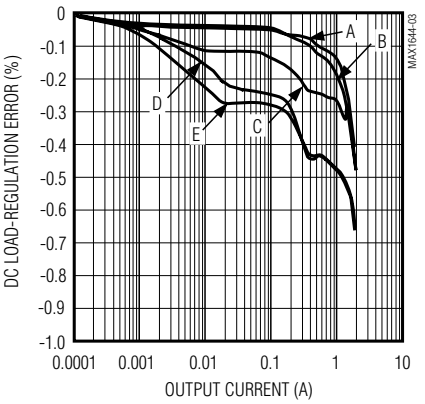
EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT

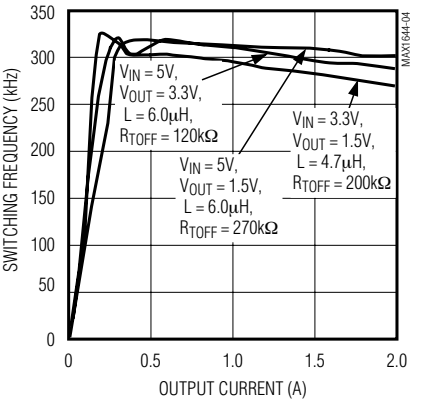


DC LOAD-REGULATION ERROR vs. OUTPUT CURRENT

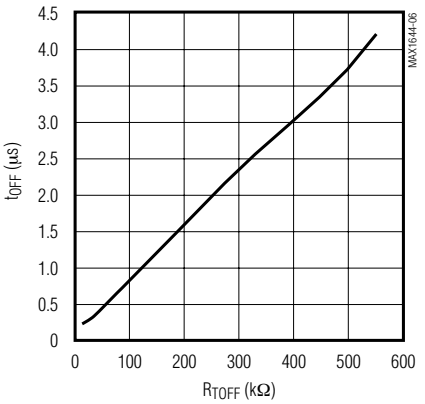


A: V_{IN} = 3.3V, V_{OUT} = 1.5V, L = 4.7µH, R_{TOFF} = 200kΩ, FBSEL = GND
B: V_{IN} = 3.3V, V_{OUT} = 1.5V, L = 4.7µH, R_{TOFF} = 200kΩ, FBSEL = REF
C: V_{IN} = 5V, V_{OUT} = 3.3V, L = 6.0µH, R_{TOFF} = 120kΩ, FBSEL = OPEN
D: V_{IN} = 5V, V_{OUT} = 1.5V, L = 6.0µH, R_{TOFF} = 270kΩ, FBSEL = GND
E: V_{IN} = 5V, V_{OUT} = 1.5V, L = 6.0µH, R_{TOFF} = 270kΩ, FBSEL = REF

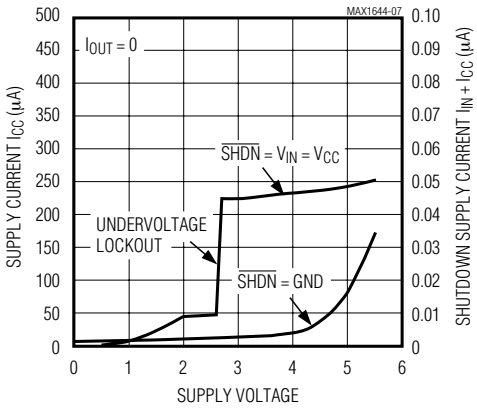
SWITCHING FREQUENCY vs. OUTPUT CURRENT



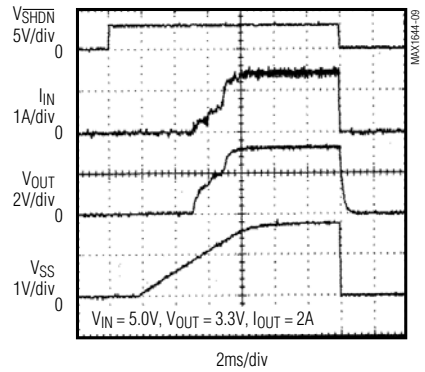
OFF-TIME vs. R_{TOFF}



SUPPLY CURRENT vs. SUPPLY VOLTAGE



STARTUP AND SHUTDOWN TRANSIENTS



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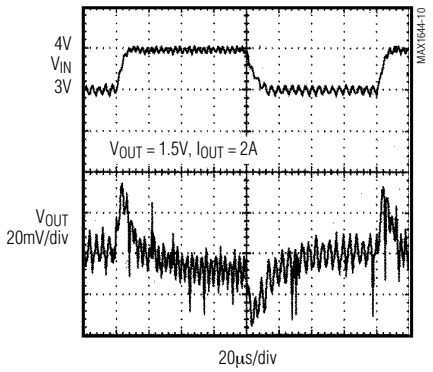
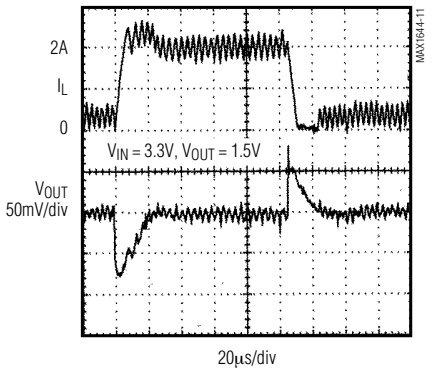
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LINE-TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE (FBSEL = REF)



Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to disable the reference, control circuitry, and internal MOSFETs. Drive high or connect to V_{CC} for normal operation.
2, 4	IN	Supply Voltage Input for the internal PMOS power switch
3, 14, 16	LX	Connection for the drains of the PMOS power switch and NMOS synchronous-rectifier switch. Connect the inductor from this node to output filter capacitor and load.
5	SS	Soft-Start. Connect a capacitor from SS to GND to limit inrush current during start-up.
6	COMP	Integrator Compensation. Connect a capacitor from COMP to V_{CC} for integrator compensation. See the *Integrator Amplifier* section.
7	TOFF	Off-Time Select Input. Sets the PMOS power switch off-time during constant-off-time operation. Connect a resistor from TOFF to GND to adjust the PMOS switch off-time.
8	FB	Feedback Input for both preset-output and adjustable-output operating modes. Connect directly to output for fixed-voltage operation or to a resistor-divider for adjustable operating modes.
9	GND	Analog Ground
10	REF	Reference Output. Bypass REF to GND with a 1µF capacitor.
11	FBSEL	Feedback Select Input. Selects AC load-regulation error and output voltage. See Table 2 for programming instructions.
12	V_{CC}	Analog Supply Voltage Input. Supplies internal analog circuitry. Bypass V_{CC} with a 10Ω and 2.2µF low-pass filter. See Figure 1.
13, 15	PGND	Power Ground. Internally connected to the internal NMOS synchronous-rectifier switch.

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Detailed Description

The MAX1644 synchronous, current-mode, constant-off-time, PWM DC-DC converter steps down input voltages of +3V to +5.5V to a preset output voltage of either +3.3V or +2.5V, or to an adjustable output voltage from +1.1V to V_{IN}. The device delivers up to 2A of continuous load current. Internal switches composed of a 0.1Ω PMOS power switch and a 0.1Ω NMOS synchronous-rectifier switch improve efficiency, reduce component count, and eliminate the need for an external Schottky diode.

The MAX1644 optimizes performance by operating in constant-off-time mode under heavy loads and in Maxim's proprietary Idle Mode under light loads. A single resistor-programmable constant-off-time control sets switching frequencies up to 350kHz, allowing the user to optimize performance trade-offs in efficiency, switching noise, component size, and cost. Under low-dropout conditions, the device operates in a 100% duty-cycle mode, where the PMOS switch remains permanently on. Idle Mode enhances light-load efficiency by skipping cycles, thus reducing transition and gate-charge losses.

When power is drawn from a regulated supply, constant-off-time PWM architecture essentially provides constant-frequency operation. This architecture has the inherent advantage of quick response to line and load transients.

The MAX1644's current-mode, constant-off-time PWM architecture regulates the output voltage by changing the PMOS switch on-time relative to the constant off-time. Increasing the on-time increases the peak inductor current and the amount of energy transferred to the load per pulse.

Modes of Operation

The current through the PMOS switch determines the mode of operation: constant-off-time mode (for load currents greater than 0.2A) or Idle Mode (for load currents less than 0.2A). Current sense is achieved through a proprietary architecture that eliminates current-sensing I^2R losses.

Constant-Off-Time Mode

Constant-off-time operation occurs when the current through the PMOS switch is greater than the Idle Mode threshold current (0.4A, which corresponds to a load current of 0.2A). In this mode, the regulation comparator turns the PMOS switch on at the end of each off-time, keeping the device in continuous-conduction mode. The PMOS switch remains on until the output is in regulation or the current limit is reached. When the PMOS switch turns off, it remains off for the programmed off-time (t_{OFF}). If the output falls dramatically out of regulation—approximately V_{FB} / 4—the PMOS switch remains off for approximately four times t_{OFF}. The NMOS synchronous rectifier turns on shortly after the PMOS switch turns off, and it remains on until shortly before the PMOS switch turns back on.

Idle Mode

Under light loads, the device improves efficiency by switching to a pulse-skipping Idle Mode. Idle Mode operation occurs when the current through the PMOS switch is less than the Idle Mode threshold current. Idle Mode forces the PMOS to remain on until the current through the switch reaches 0.4A, thus minimizing the unnecessary switching that degrades efficiency under light loads. In Idle Mode, the device operates in discontinuous conduction. Current-sense circuitry monitors the current through the NMOS synchronous switch, turning it off before the current reverses. This prevents current from being pulled from the output filter through the inductor and NMOS switch to ground. As the device switches between operating modes, no major shift in circuit behavior occurs.

100% Duty-Cycle Operation

When the input voltage drops near the output voltage, the duty cycle increases until the PMOS MOSFET is on continuously. The dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal PMOS switch and parasitic resistance in the inductor. The PMOS switch remains on continuously as long as the current limit is not reached.

Shutdown

Drive $\overline{SHDN}$ to a logic-level low to place the MAX1644 in low-power shutdown mode and reduce supply current to less than 1µA. In shutdown, all circuitry and internal MOSFETs turn off, and the LX node becomes high impedance. Drive $\overline{SHDN}$ to a logic-level high or connect to V_{CC} for normal operation.

Summing Comparator

Three signals are added together at the input of the summing comparator (Figure 1): an output voltage error signal relative to the reference voltage, an integrated output voltage error correction signal, and the sensed PMOS switch current. The integrated error signal is provided by a transconductance amplifier with an external capacitor at COMP. This integrator provides high DC accuracy without the need for a high-gain amplifier. Connecting a capacitor at COMP modifies the overall loop response (see the *Integrator Amplifier* section).

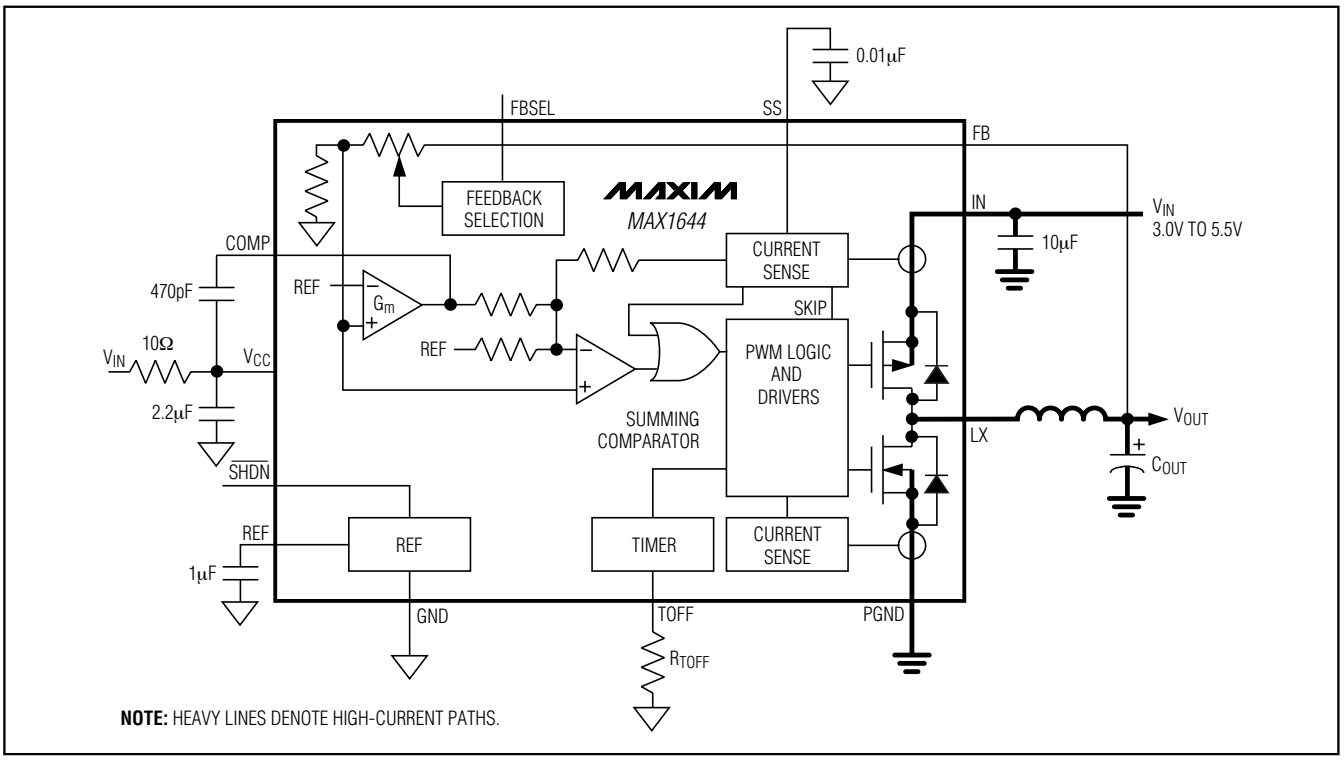


Figure 1. Functional Diagram

Synchronous Rectification

In a step-down regulator without synchronous rectification, an external Schottky diode provides a path for current to flow when the inductor is discharging. Replacing the Schottky diode with a low-resistance NMOS synchronous switch reduces conduction losses and improves efficiency.

The NMOS synchronous-rectifier switch turns on following a short delay after the PMOS power switch turns off, thus preventing cross conduction or "shoot through." In constant-off-time mode, the synchronous-rectifier switch turns off just prior to the PMOS power switch turning on. While both switches are off, inductor current flows through the internal body diode of the NMOS switch. The internal body diode's forward voltage is relatively high.

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area immediately surrounding the IC leads. The MAX1644 evaluation kit has 0.5 in.^{2} of copper area and a thermal resistance of 60°C/W with no airflow. Airflow over the IC significantly reduces the junction-to-ambient thermal resistance. For heatsinking purposes, evenly distribute the copper area connected at the IC among the high-current pins.

Power Dissipation

Power dissipation in the MAX1644 is dominated by conduction losses in the two internal power switches. Power dissipation due to supply current in the control section and average current used to charge and discharge the gate capacitance of the internal switches are less than 30mW at 300kHz. This number is reduced when the switching frequency decreases as the part enters Idle Mode. Combined conduction losses in the two power switches are approximated by:

$$P_D = I_{OUT}^2 \cdot R_{ON}$$

The junction-to-ambient thermal resistance required to dissipate this amount of power is calculated by:

$$\theta_{JA} = (T_{J,MAX} - T_{A,MAX}) / P_D$$

where: θ_{JA} = junction-to-ambient thermal resistance

$T_{J,MAX}$ = maximum junction temperature

$T_{A,MAX}$ = maximum ambient temperature

2A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Design Procedure

For typical applications, use the recommended component values in Table 1. For other applications, take the following steps:

1) Select the desired PWM-mode switching frequency; 300kHz is a good starting point.
2) Select the constant-off-time as a function of input voltage, output voltage, and switching frequency.
3) Select R_{TOFF} as a function of off-time.
4) Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

Table 1. Recommended Component Values (I_{OUT} = 2A, f_{PWM} = 300kHz)

V_{IN} (V)	V_{OUT} (V)	L (µH)	R_{TOFF} (kΩ)
5	3.3	6.0	120
5	2.5	6.8	180
5	1.8	6.8	240
5	1.5	6.0	270
3.3	2.5	3.3	82
3.3	1.8	4.7	180
3.3	1.5	4.7	200

Table 2. Output Voltage and AC Load-Regulation Selection

PIN		OUTPUT VOLTAGE (V)	AC LOAD-REGULATION ERROR (%)
FBSEL	FB		
V_{CC}	Output Voltage	2.5	2
Unconnected	Output Voltage	3.3	2
REF	Resistor Divider	Adjustable	2
GND	Resistor Divider	Adjustable	1

Setting the Output Voltage

The output of the MAX1644 is selectable between one of two preset output voltages: (2.5V or 3.3V) with a 2% AC load-regulation error, or an adjustable output voltage from the reference voltage (nominally 1.1V) up to V_{IN} with a 1% or 2% AC load-regulation error. For a preset output voltage, connect FB to the output voltage, and connect FBSEL to V_{CC} (2.5V output voltage) or leave unconnected (3.3V output voltage). Internal resistor-dividers divide down the output voltage, regulating the divided voltage to the internal reference voltage. For output voltages other than 2.5V or 3.3V, or for tighter AC load regulation, connect FBSEL to GND (1% regulation) or to REF (2% regulation), and connect FB to a resistor divider between the output voltage and ground (Figure 2). Regulation is maintained for adjustable output voltages when V_{FB} equals V_{REF}. Use 50kΩ for R1. R2 is given by the equation:

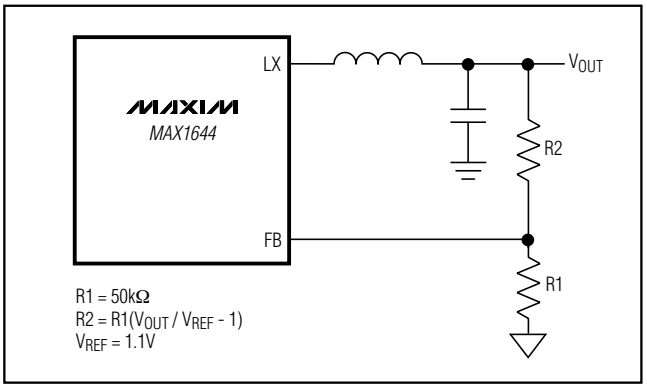


Figure 2. Adjustable Output Voltage

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} is typically 1.1V.

Programming the Switching Frequency and Off-Time

The MAX1644 features a programmable PWM mode switching frequency, which is set by the input and output voltage and the value of R_{TOFF}, connected from TOFF to GND. R_{TOFF} sets the PMOS power switch off-time in PWM mode. Use the following equation to select the off-time according to your desired switching frequency in PWM mode (I_{OUT} > 0.2A):

$$t_{OFF} = \frac{(V_{IN} - V_{OUT} - V_{PMOS})}{f_{PWM}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

where: t_{OFF} = the programmed off-time
V_{IN} = the input voltage
V_{OUT} = the output voltage
V_{NMOS} = the voltage drop across the internal PMOS power switch
V_{PMOS} = the voltage drop across the internal NMOS synchronous-rectifier switch

f_{PWM} = switching frequency in PWM mode (I_{OUT} > 0.2A)

Select R_{TOFF} according to the formula:

$$R_{TOFF} = (t_{OFF} - 0.07\mu s)\ (150k\Omega / 1.26\mu s)$$

Recommended values for R_{TOFF} range from 39kΩ to 470kΩ for off-times of 0.4µs to 4µs.

Inductor Selection

Three key inductor parameters must be specified: inductor value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC current (ripple current) to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple-current to load-current ratio (LIR = 0.25), which corresponds to a peak inductor current 1.125 times higher than the DC load current:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{OUT} \times LIR}$$

where: I_{OUT} = maximum DC load current

LIR = ratio of peak-to-peak AC inductor current to DC load current, typically 0.25

The peak inductor current at full load is 1.125 • I_{OUT} if the above equation is used; otherwise, the peak current is calculated by:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT} \times t_{OFF}}{2 \times L}$$

Choose an inductor with a saturation current at least as high as the peak inductor current. To minimize loss, choose an inductor with a low DC resistance.

Capacitor Selection

The input filter capacitor reduces peak currents and noise at the voltage source. Use a low-ESR and low-ESL capacitor located no further than 5mm from IN. Select the input capacitor according to the RMS input ripple-current requirements and voltage rating:

$$I_{RIPPLE} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The output filter capacitor affects the output voltage ripple, output load-transient response, and feedback loop stability. For stable operation, the MAX1644 requires a minimum output ripple voltage of $V_{RIPPLE} \geq 2\% \cdot V_{OUT}$ (with 2% load regulation setting).

The minimum ESR of the output capacitor should be:

$$ESR > 1\% \times \frac{L}{t_{OFF}}$$

Stable operation requires the correct output filter capacitor. When choosing the output capacitor, ensure that:

$$C_{OUT} \geq (t_{OFF} / V_{OUT}) \times (64\mu FV / \mu s)$$

With an AC load regulation setting of 1%, the C_{OUT} requirement doubles, and the minimum ESR of the output capacitor is halved.

Integrator Amplifier

An internal transconductance amplifier fine tunes the output DC accuracy. A capacitor, C_{COMP}, from COMP to V_{CC} compensates the transconductance amplifier. For stability, choose:

$$C_{COMP} \geq 470pF$$

A large capacitor value maintains a constant average output voltage but slows the loop response to changes in output voltage. A small capacitor value speeds up the loop response to changes in output voltage but decreases stability. Choose the capacitor values that result in optimal performance.

Setting the AC Loop Gain

The MAX1644 allows selection of a 1% or 2% AC load-regulation error when the adjustable output voltage mode is selected (Table 2). A 2% setting is automatically selected in preset output voltage mode (FBSEL connected to V_{CC} or unconnected). A 2% load-regulation error setting reduces output filter capacitor requirements, allowing the use of smaller and less expensive capacitors. Selecting a 1% load-regulation error reduces transient load errors, but requires larger capacitors.

2A Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Soft-Start

Soft-start allows a gradual increase of the internal current limit to reduce input surge currents at start-up and at exit from shutdown. A charging capacitor, C_{SS}, placed from SS to GND sets the rate at which the internal current limit is changed. Upon power-up, when the device comes out of undervoltage lockout (2.6V typ) or after the $\overline{SHDN}$ pin is pulled high, a 5µA constant-current source charges the soft-start capacitor and the voltage on SS increases. When the voltage on SS is less than approximately 0.7V, the current limit is set to zero. As the voltage increases from 0.7V to approximately 1.8V, the current limit is adjusted from 0 to 2.9A. The voltage across the soft-start capacitor changes with time according to the equation:

$$V_{SS} = \frac{5\mu A \times t}{C_{SS}}$$

The soft-start current limit varies with the voltage on the soft-start pin, SS, according to the equation:

$$I_{LIMIT} = (V_{SS} - 0.7V) \cdot 2.7A/V, \text{ for } V_{SS} > 0.7V$$

The constant-current source stops charging once the voltage across the soft-start capacitor reaches 1.8V (Figure 3).

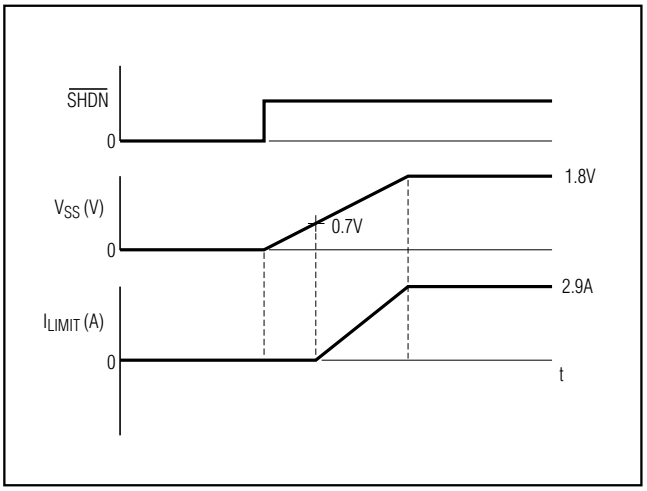


Figure 3. Soft-Start Current Limit over Time

Circuit Layout and Grounding

Good layout is necessary to achieve the MAX1644's intended output power level, high efficiency, and low noise. Good layout includes the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths. The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND together.
2) Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm.
3) Place the LX node components as close together and as near to the device as possible. This reduces resistive and switching losses as well as noise.
4) A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane.

Chip Information

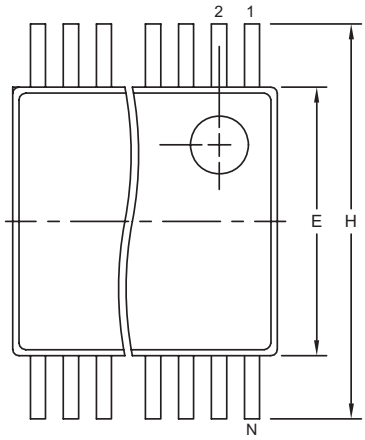
TRANSISTOR COUNT: 1758

2A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches

Package Information

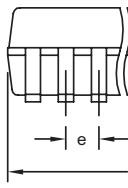
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

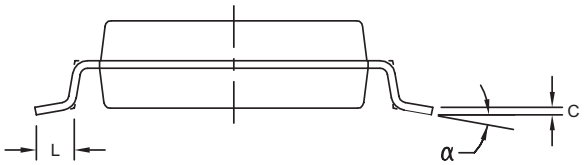
SSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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