150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
CNVST, SCLK, DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
REF, AIN1 (AIN+), AIN2 (AIN-) to GND.....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 9.70mW/°C above T_A = +70°C) ...696mW
8-Pin TDFN (derate 18.5mW/°C above T_A = +70°C) ...1481mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free Packages.....+260°C
Packages Containing Lead(Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, V_{REF} = +2.5V for MAX1287/MAX1289, or V_{DD} = +4.75V to +5.25V, V_{REF} = +4.096V for MAX1286/MAX1288, 0.1µF capacitor at REF, f_{SCLK} = 8MHz (50% duty cycle), AIN- = GND for MAX1288/MAX1289. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error				±2	±4	LSB
Gain Error (Note 3)				±2	±4	LSB
Gain Temperature Coefficient				±0.4		ppm/°C
Offset Temperature Coefficient				±0.4		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB
Input Common-Mode Rejection	CMR	V_{CM} = 0V to V_{DD}; zero scale input		±0.1		mV
DYNAMIC SPECIFICATIONS: (f_{IN} (sine-wave) = 10kHz, V_{IN} = 4.096Vp-p for MAX1286/MAX1288 or V_{IN} = 2.5V_{p-p} for MAX1287/MAX1289, 150ksps, f_{SCLK} = 8MHz, (50% duty cycle) AIN- = GND for MAX1288/MAX1289)						
Signal to Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-82		dB
Spurious-Free Dynamic Range	SFDR			86		dB
Full-Power Bandwidth		-3dB point		1		MHz
Full-Linear Bandwidth		SINAD > 68dB		100		kHz
CONVERSION RATE						
Conversion Time	t_{CONV}	Does not include t_{ACQ}			3.7	µs
T/H Acquisition Time	t_{ACQ}				1.4	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Maximum Serial Clock Frequency	f_{SCLK}		8			MHz
Duty Cycle			30		70	%
ANALOG INPUT						
Input Voltage Range (Note 4)		Unipolar	0		V_{REF}	V
		Bipolar	-V_{REF} /2		V_{REF}/2	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = +2.5V for MAX1287/MAX1289, or V_{DD} = +4.75V to +5.25V, V_{REF} = +4.096V for MAX1286/MAX1288, 0.1µF capacitor at REF, f_{SCLK} = 8MHz (50% duty cycle), AIN- = GND for MAX1288/MAX1289. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Leakage Current		Channel not selected or conversion stopped			±0.01	±1	µA
Input Capacitance					34		pF
EXTERNAL REFERENCE INPUT							
Input Voltage Range	V_{REF}			1.0		V_{DD} +50mV	V
Input Current	I_{REF}	V_{REF} = +2.5V at 150ksps			16	30	µA
		V_{REF} = +4.096V at 150ksps			26	45	
		Acquisition/Between conversions			±0.01	±1	
DIGITAL INPUTS/OUTPUTS (SCLK, CNVST, DOUT)							
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			V_{DD} -1			V
Input Leakage Current	I_L				±0.01	±1.0	µA
Input Capacitance	C_{IN}				15		pF
Output Low Voltage	V_{OL}	I_{SINK} = 2mA				0.4	V
		I_{SINK} = 4mA				0.8	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1.5mA		V_{DD} -0.5			V
Three-State Leakage Current		CNVST = GND			±0.05	±10	µA
Three-State Output Capacitance	C_{OUT}	CNVST = GND			15		pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	MAX1286/MAX1288		4.75	5.0	5.25	V
		MAX1287/MAX1289		2.7	3.0	3.6	
Positive Supply Current	I_{DD}	V_{DD} = +3V	f_{SAMPLE} = 150ksps		245	350	µA
			f_{SAMPLE} = 100ksps		150		
			f_{SAMPLE} = 10ksps		15		
			f_{SAMPLE} = 1ksps		2		
		V_{DD} = +5V	f_{SAMPLE} = 150ksps		320	400	
			f_{SAMPLE} = 100ksps		215		
			f_{SAMPLE} = 10ksps		22		
			f_{SAMPLE} = 1ksps		2.5		
		Shutdown			0.2	5	
Positive Supply Rejection	PSR	V_{DD} = 5V ±5%; full-scale input			±0.3	±1.0	mV
		V_{DD} = +2.7V to +3.6V; full-scale input			±0.4	±1.2	

150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

TIMING CHARACTERISTICS (Figures 1, 2, and 5)

(V_{DD} = +2.7V to +3.6V, V_{REF} = +2.5V, 0.1µF capacitor at REF, or V_{DD} = +4.75V to +5.25V for MAX1286/MAX1288, V_{REF} = +4.096V, 0.1µF capacitor at REF, f_{SCLK} = 8MHz (50% duty cycle); AIN- = GND for MAX1288/MAX1289. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		38			ns
SCLK Pulse Width Low	t_{CL}		38			ns
SCLK Fall to DOUT Transition	t_{DOT}	C_{LOAD} = 30pF			60	ns
SCLK Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 30pF	100		500	ns
CNVST Rise to DOUT Enable	t_{DOE}	C_{LOAD} = 30pF			80	ns
CNVST Fall to MSB Valid	t_{CONV}	C_{LOAD} = 30pF			3.7	µs
CNVST Pulse Width	t_{CSW}		30			ns

Note 1: Unipolar mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: Offset nulled.
Note 4: The absolute input voltage range for the analog inputs is from GND to V_{DD}.

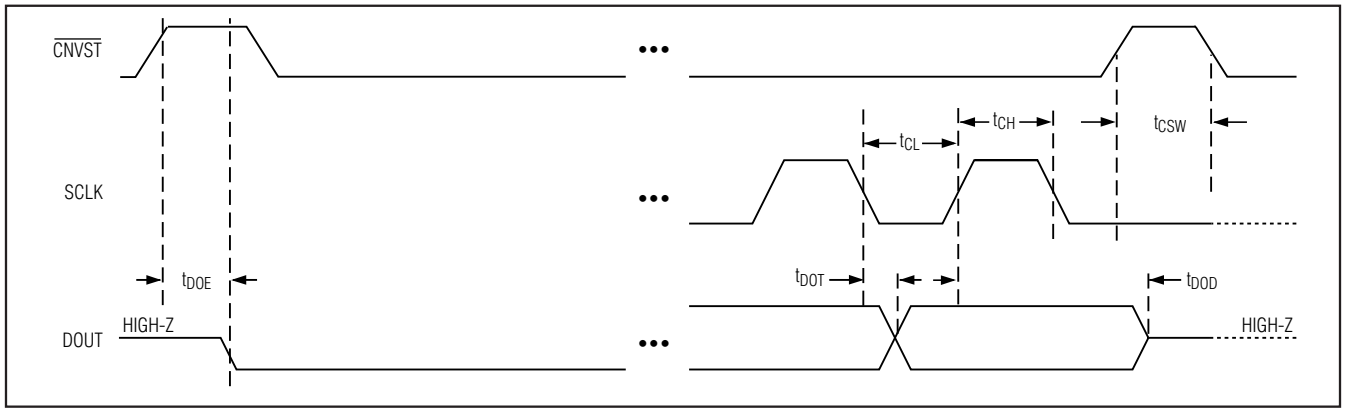


Figure 1. Detailed Serial-Interface Timing Sequence

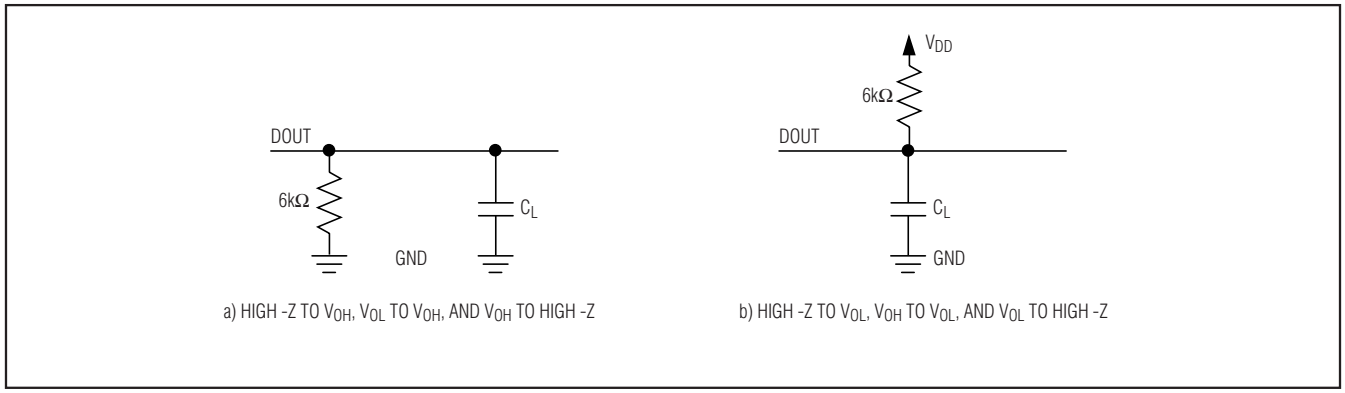
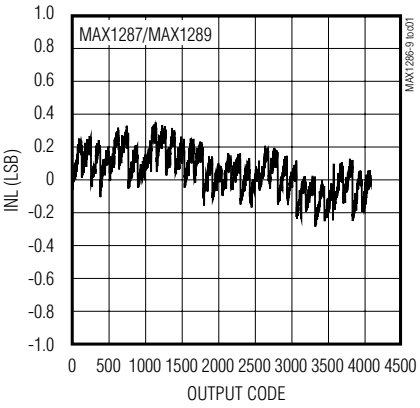


Figure 2. Load Circuits for Enable/Disable Times

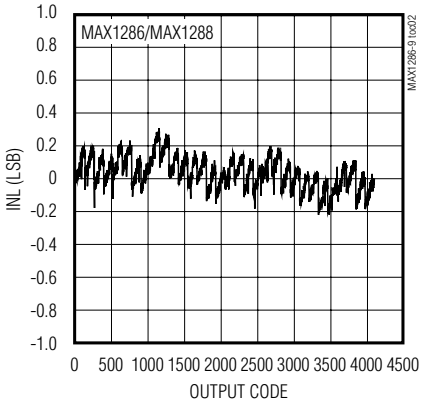
Typical Operating Characteristics

(V_{DD} = +3V, V_{REF} = +2.5V for MAX1287/MAX1289. V_{DD} = +5V, V_{REF} = +4.096V for MAX1286/MAX1288; 0.1µF capacitor at REF, f_{SCLK} = 8MHz (50% duty cycle); AIN- = GND for MAX1288/MAX1289, T_A = +25°C, unless otherwise noted.)

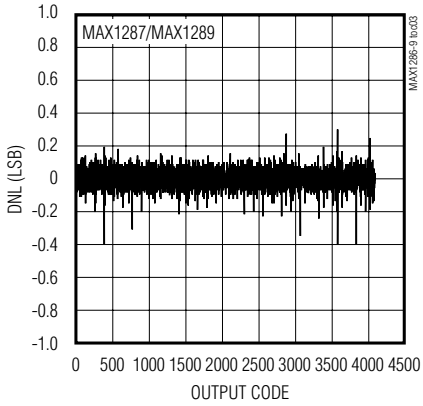
INTEGRAL NONLINEARITY vs. OUTPUT CODE



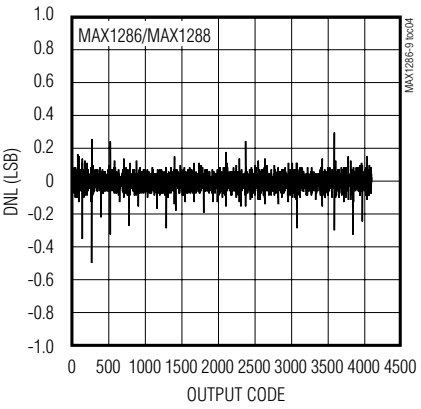
INTEGRAL NONLINEARITY vs. OUTPUT CODE



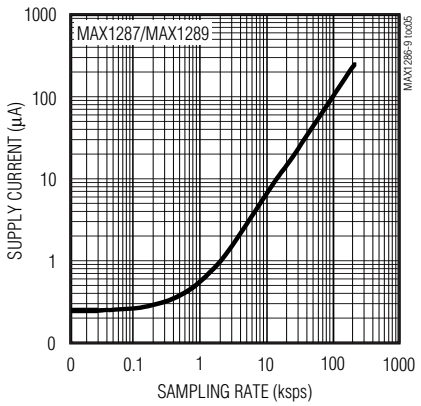
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



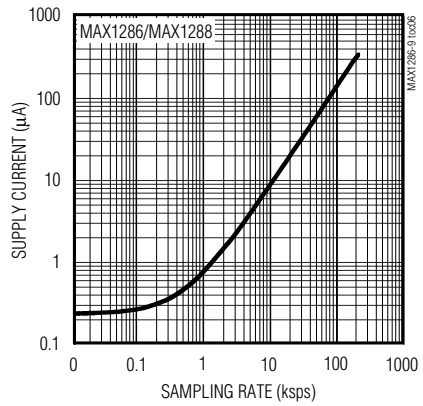
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



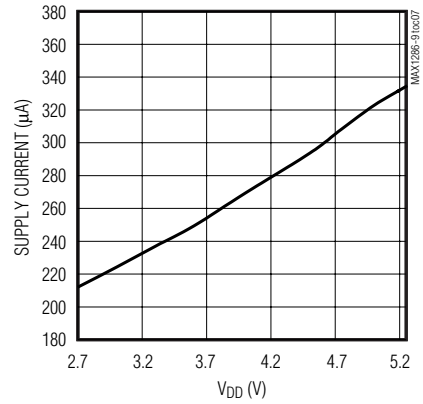
SUPPLY CURRENT vs. SAMPLING RATE



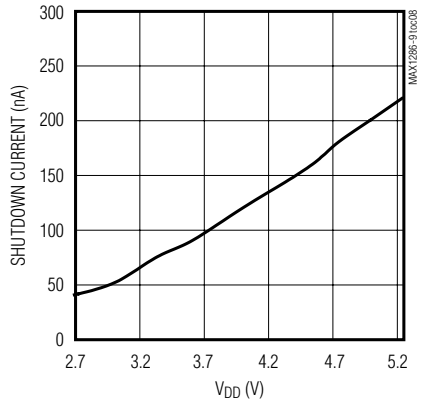
SUPPLY CURRENT vs. SAMPLING RATE



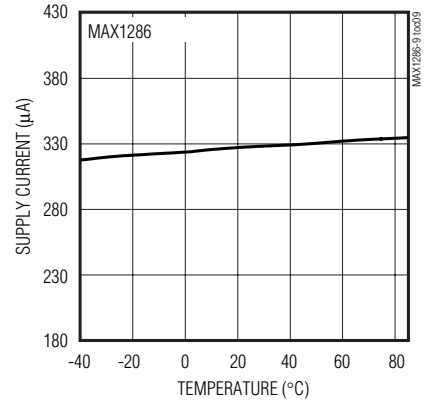
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

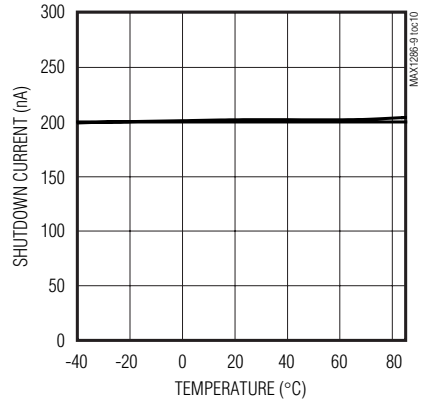


150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

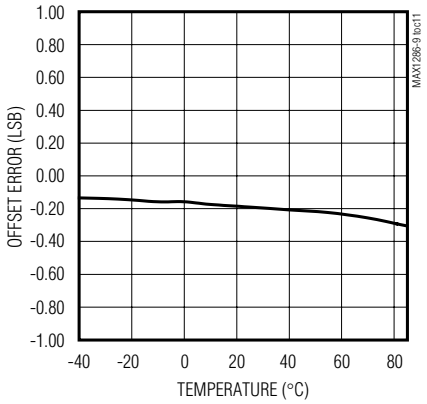
Typical Operating Characteristics (continued)

(V_{DD} = +3V, V_{REF} = +2.5V for MAX1287/MAX1284. V_{DD} = +5V, V_{REF} = +4.096V for MAX1286/MAX1288; 0.1µF capacitor at REF, f_{SCLK} = 8MHz (50% duty cycle); AIN- = GND for MAX1288/MAX1289, T_A = +25°C, unless otherwise noted.)

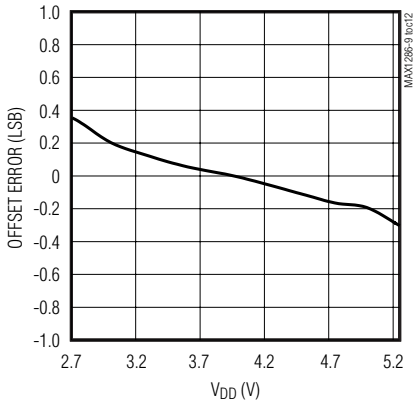
SHUTDOWN CURRENT vs. TEMPERATURE



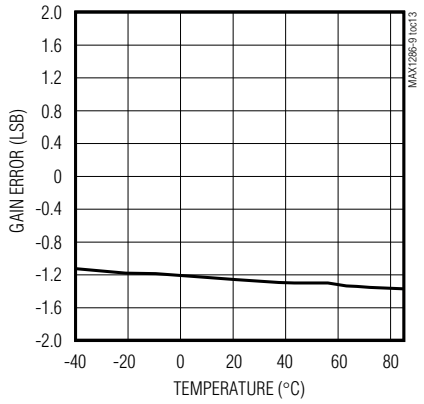
OFFSET ERROR vs. TEMPERATURE



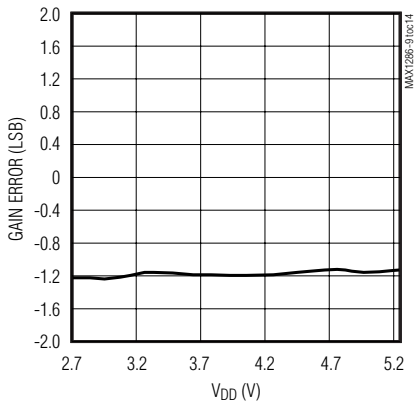
OFFSET ERROR vs. SUPPLY VOLTAGE



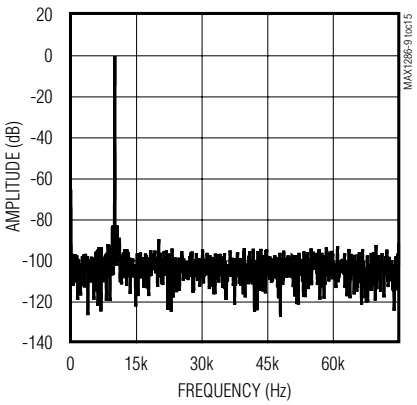
GAIN ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



FFT PLOT (SINAD)



Pin Description

PIN	NAME		FUNCTION
	MAX1286 MAX1287	MAX1288 MAX1289	
1	V_{DD}	V_{DD}	Positive Supply Voltage. +2.7V to +3.6V (MAX1287/MAX1289); +4.75V to +5.25V (MAX1286/MAX1288). Bypass with a 0.1µF capacitor to GND.
2	AIN1	AIN+	Analog Input Channel 1 (MAX1286/MAX1287) or Positive Analog Input (MAX1288/MAX1289)
3	AIN2	AIN-	Analog Input Channel 2 (MAX1286/MAX1287) or Negative Analog Input (MAX1288/MAX1289)
4	GND	GND	Ground
5	REF	REF	External Reference Voltage Input. Sets the analog voltage range. Bypass with a 0.1µF capacitor to GND.
6	CNVST	CNVST	Conversion Start. A rising edge powers up the IC and places it in track mode. At the falling edge of CNVST, the device enters hold mode and begins conversion. CNVST also selects the input channel (MAX1286/MAX1287) or input polarity (MAX1288/MAX1289).
7	DOUT	DOUT	Serial Data Output. DOUT transitions the falling edge of SCLK. DOUT goes low at the start of a conversion and presents the MSB at the completion of a conversion. DOUT goes high impedance once data has been fully clocked out.
8	SCLK	SCLK	Serial Clock Input. Clocks out data at DOUT MSB first.
—	EP	EP	Exposed Pad. Connect the exposed pad to ground or leave unconnected.

Detailed Description

The MAX1286–MAX1289 ADCs use a successive-approximation conversion (SAR) technique and an on-chip track-and-hold (T/H) structure to convert an analog signal into a 12-bit digital result.

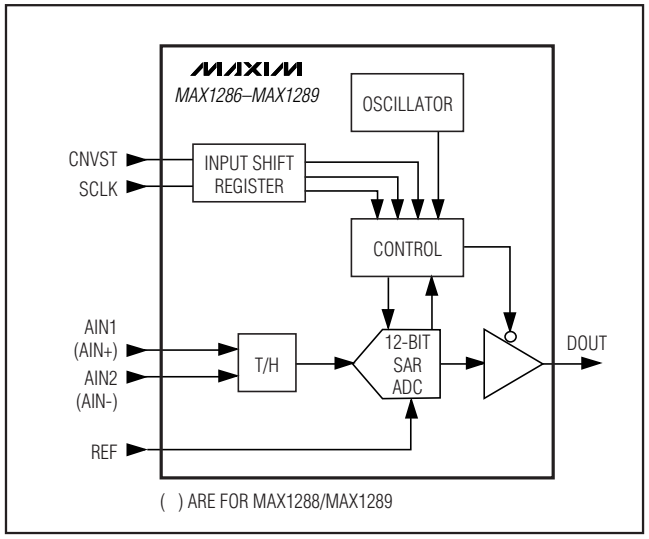


Figure 3. Simplified Functional Diagram

The serial interface provides easy interfacing to microprocessors (µPs). Figure 3 shows the simplified internal structure for the MAX1286/MAX1287 (2 channels, single ended) and the MAX1288/MAX1289 (1 channel, true differential).

True-Differential Analog Input T/H

The equivalent circuit of Figure 4 shows the MAX1286–MAX1289s' input architecture, which is composed of a T/H, input multiplexer, comparator, and switched-capacitor DAC. The T/H enters its tracking mode on the rising edge of CNVST. The positive input capacitor is connected to AIN1 or AIN2 (MAX1286/MAX1287) or AIN+ (MAX1288/MAX1289). The negative input capacitor is connected to GND (MAX1286/MAX1287) or AIN- (MAX1288/MAX1289). The T/H enters its hold mode on the falling edge of CNVST and the difference between the sampled positive and negative input voltages is converted. The time required for the T/H to acquire an input signal is determined by how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and CNVST must be held high for a longer period of time. The acquisition time, t_{ACQ}, is the maximum time needed for the signal to be acquired, plus the power-up time. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 24pF + t_{PWR}$$

150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

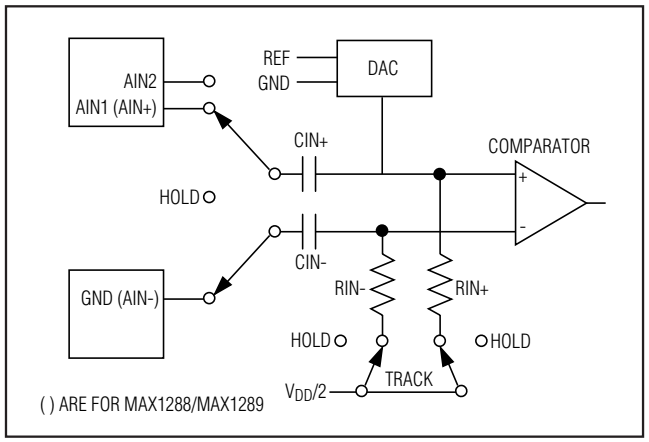


Figure 4. Equivalent Input Circuit

where R_{IN} = 1.5kΩ, R_S is the source impedance of the input signal, and t_{PWR} = 1µs is the power-up time of the device.

Note: t_{ACQ} is never less than 1.4µs and any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive and negative analog inputs.

Selecting AIN1 or AIN2 (MAX1286/MAX1287)

Select one of the MAX1286/MAX1287s' two positive input channels using the CNVST pin. If AIN1 is desired (Figure 5a), drive CNVST high to power up the ADC and place the T/H in track mode with AIN1 connected to the positive input capacitor. Hold CNVST high for t_{ACQ} to fully acquire the signal. Drive CNVST low to place the T/H in hold mode. The ADC then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK. Clock out all 12 bits of data before driving CNVST high for the next conversion. If all 12 bits of data are not clocked out before CNVST is driven high, AIN2 is selected for the next conversion.

If AIN2 is desired (Figure 5b), drive CNVST high for at least 30ns. Next, drive it low for at least 30ns, and then high again. This powers up the ADC and places the T/H in track mode with AIN2 connected to the positive input capacitor. Now hold CNVST high for t_{ACQ} to fully acquire the signal. Drive CNVST low to place the T/H in hold mode. The ADC then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK. If all 12 bits of data are not clocked out before CNVST is driven high, AIN2 is selected for the next conversion.

Selecting Unipolar or Bipolar Conversions (MAX1288/MAX1289)

Initiate true-differential conversions with the MAX1288/MAX1289s' unipolar and bipolar modes, using the CNVST pin. AIN+ and AIN- are sampled at the falling edge of CNVST. In unipolar mode, AIN+ can exceed AIN- by up to V_{REF}. The output format is straight binary. In bipolar mode, either input can exceed the other by up to $V_{REF}/2$. The output format is two's complement.

Note: In both modes, AIN+ and AIN- must not exceed V_{DD} by more than 50mV or be lower than GND by more than 50mV.

If unipolar mode is desired (Figure 5a), drive CNVST high to power up the ADC and place the T/H in track mode with AIN+ and AIN- connected to the input capacitors. Hold CNVST high for t_{ACQ} to fully acquire the signal. Drive CNVST low to place the T/H in hold mode. The ADC then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK. Clock out all 12 bits of data before driving CNVST high for the next conversion. If all 12 bits of data are not clocked out before CNVST is driven high, bipolar mode is selected for the next conversion.

If bipolar mode is desired (Figure 5b), drive CNVST high for at least 30ns. Next, drive it low for at least 30ns and then high again. This places the T/H in track mode with AIN+ and AIN- connected to the input capacitors. Now hold CNVST high for t_{ACQ} to fully acquire the signal. Drive CNVST low to place the T/H in hold mode. The ADC then performs a conversion and shutdown automatically. The MSB is available at DOUT after 3.7µs. Data can then be clocked out using SCLK. If all 12 bits of data are not clocked out before CNVST is driven high, bipolar mode is selected for the next conversion.

Input Bandwidth

The ADC's input tracking circuitry has a 1MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

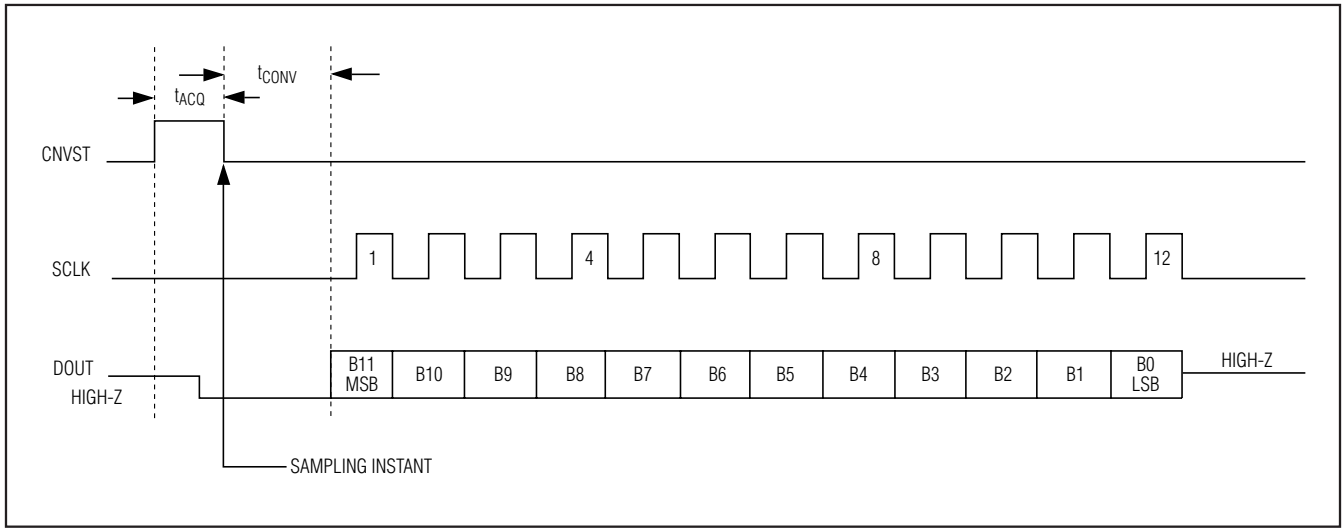


Figure 5a. Single Conversion AIN1 vs. GND (MAX1286/MAX1287), Unipolar Mode AIN+ vs. AIN- (MAX1288/MAX1289)

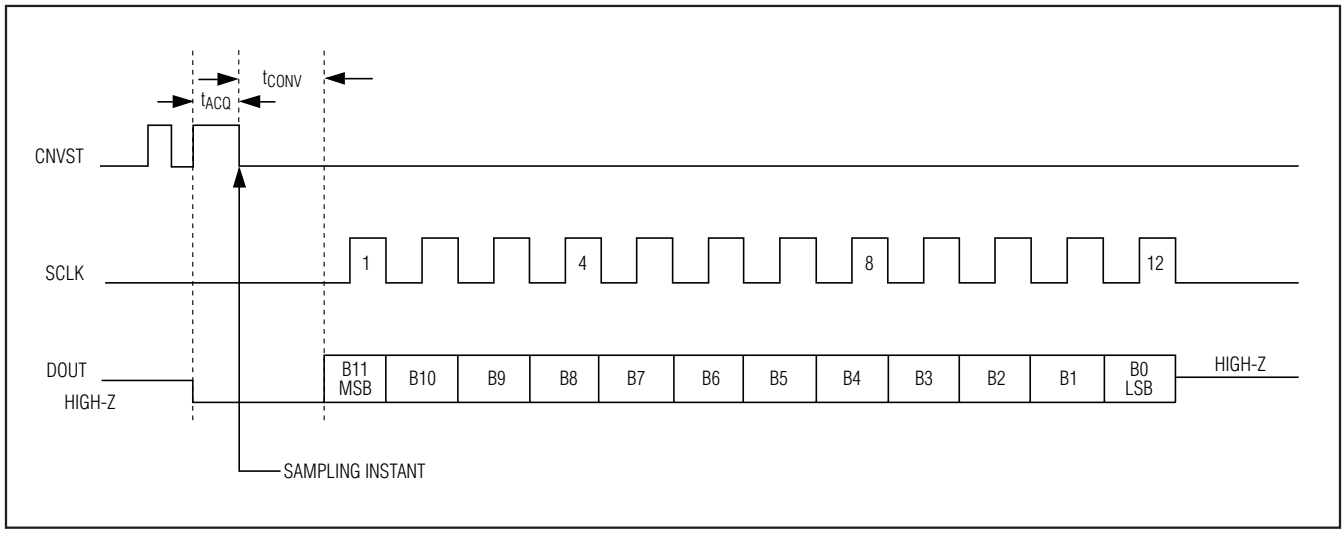


Figure 5b. Single Conversion AIN2 vs. GND (MAX1286/MAX1287), Bipolar Mode AIN+ vs. AIN- (MAX1288/MAX1289)

Analog Input Protection

Internal protection diodes that clamp the analog input to V_{DD} and GND allow the analog input pins to swing from GND - 0.3V to V_{DD} + 0.3V without damage. Both inputs must not exceed V_{DD} by more than 50mV or be lower than GND by more than 50mV for accurate conversions. **If an off-channel analog input voltage exceeds the supplies, limit the input current to 2mA.**

Internal Clock

The MAX1286–MAX1289 operate from an internal oscillator, which is accurate within 10% of the 4MHz specified clock rate. This results in a worst-case conversion time of 3.7µs. The internal clock releases the system microprocessor from running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0 to 8MHz.

150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

Output Data Format

Figures 5a and 5b illustrate the conversion timing for the MAX1286–MAX1289. The 12-bit conversion result is output in MSB-first format. Data on DOUT transitions on the falling edge of SCLK. All 12 bits must be clocked out before CNVST transitions again. For the MAX1288/MAX1289, data is straight binary for unipolar mode and two's complement for bipolar mode. For the MAX1286/MAX1287, data is always straight binary.

Transfer Function

Figure 6 shows the unipolar transfer function for the MAX1286–MAX1289. Figure 7 shows the bipolar transfer function for the MAX1288/MAX1289. Code transitions occur halfway between successive-integer LSB values.

Applications Information

Automatic Shutdown Mode

With CNVST low, the MAX1286–MAX1289 default to an AutoShutdown state (< 0.2µA) after power-up and between conversions. After detecting a rising edge on CNVST, the part powers up, sets DOUT low, and enters track mode. After detecting a falling edge on CNVST, the device enters hold mode and begins the conversion. A maximum of 3.7µs later, the device completes conversion, enters shutdown, and MSB is available at DOUT.

External Reference

An external reference is required for the MAX1286–MAX1289. Use a 0.1µF bypass capacitor for best performance. The reference input structure allows a voltage range of +1V to V_{DD} + 50mV.

Connection to Standard Interfaces

The MAX1286–MAX1289 feature a serial interface that is fully compatible with SPI, QSPI, and MICROWIRE. If a serial interface is available, establish the CPU's serial interface as a master, so that the CPU generates the serial clock for the ADCs. Select a clock frequency up to 8MHz.

How to Perform a Conversion

1) Use a general-purpose I/O line on the CPU to hold CNVST low between conversions.
2) Drive CNVST high to acquire AIN1(MAX1286/MAX1287) or unipolar mode (MAX1288/MAX1289). To acquire AIN2 (MAX1286/MAX1287) or bipolar mode (MAX1288/MAX1289), drive CNVST low and high again.
3) Hold CNVST high for 1.4µs.
4) Drive CNVST low and wait approximately 3.7µs for conversion to complete. After 3.7µs, the MSB is available at DOUT.

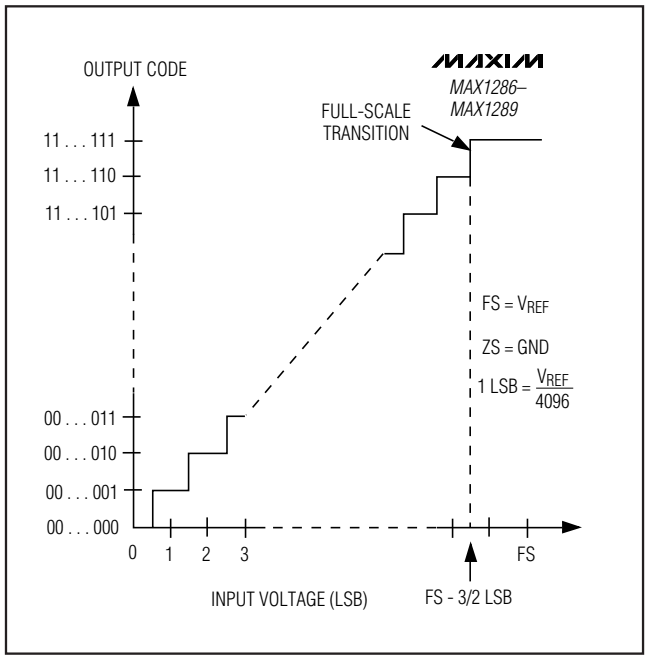


Figure 6. Unipolar Transfer Function

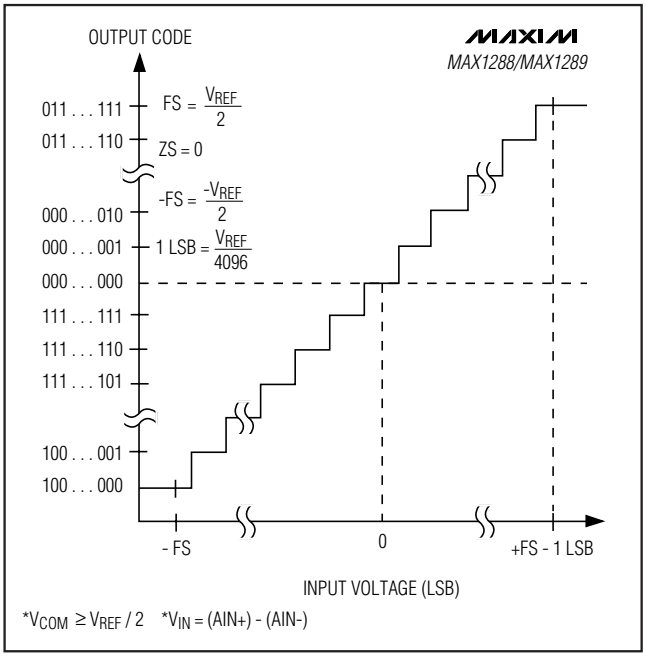


Figure 7. Bipolar Transfer Function

5) Activate SCLK for a minimum of 12 rising clock edges. DOUT transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Clock data into the µP on SCLK's rising edge.

SPI and MICROWIRE Interface

When using an SPI (Figure 8a) or MICROWIRE interface (Figures 8a and 8b), set CPOL = CPHA = 0. Two 8-bit readings are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µP on SCLK's rising edge. The first 8-bit data stream contains the first 8-bits of DOUT starting with the MSB. The second 8-bit data stream contains the remaining four result bits. DOUT then goes high impedance.

QSPI Interface

Using the high-speed QSPI interface (Figure 9a) with CPOL = 0 and CPHA = 0, the MAX1286–MAX1289 support a maximum f_{SCLK} of 8MHz. One 12- to 16-bit reading is necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µP on SCLK's rising edge. The first 12 bits are the data. DOUT then goes high impedance (Figure 9b).

PIC16 and SSP Module and PIC17 Interface

The MAX1286–MAX1289 are compatible with a PIC16/PIC17 µC, using the synchronous serial port (SSP) module

To establish SPI communication, connect the controller as shown in Figure 10a and configure the PIC16/PIC17 as system master. This is done by initializing its synchronous serial port control register (SSPCON) and synchronous serial port status register (SSPSTAT) to the bit patterns shown in Tables 1 and 2.

In SPI mode, the PIC16/PIC17 µCs allow 8 bits of data to be synchronously transmitted and received simultaneously. Two consecutive 8-bit readings (Figure 10b) are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µC on SCLK's rising edge. The first 8-bit data stream contains the first 8 data bits starting with the MSB. The second data stream contains the remaining bits, D3 through D0.

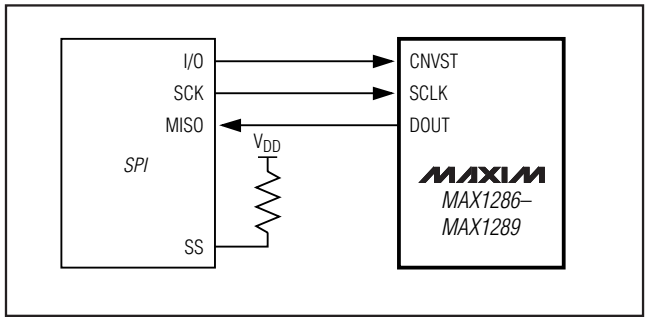


Figure 8a. SPI Connections

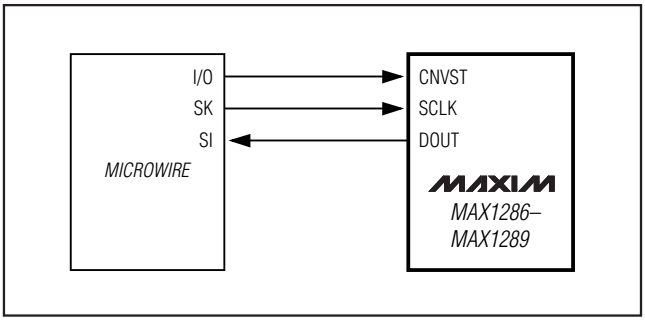


Figure 8b. MICROWIRE Connections

Table 1. Detailed SSPCON Register Content

CONTROL BIT		MAX1286–MAX1289 SETTINGS	SYNCHRONOUS SERIAL PORT CONTROL REGISTER (SSPCON)
WCOL	Bit 7	X	Write Collision Detection Bit
SSPOV	Bit 6	X	Receive Overflow Detect Bit
SSPEN	Bit 5	1	Synchronous Serial Port Enable Bit: 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial port pins.
CKP	Bit 4	0	Clock Polarity Select Bit. CKP = 0 for SPI master mode selection.
SSPM3	Bit 3	0	Synchronous Serial Port Mode Select Bit. Sets SPI master mode and selects $F_{CLK} = f_{OSC} / 16$.
SSPM2	Bit 2	0	
SSPM1	Bit 1	0	
SSPM0	Bit 0	1	

150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

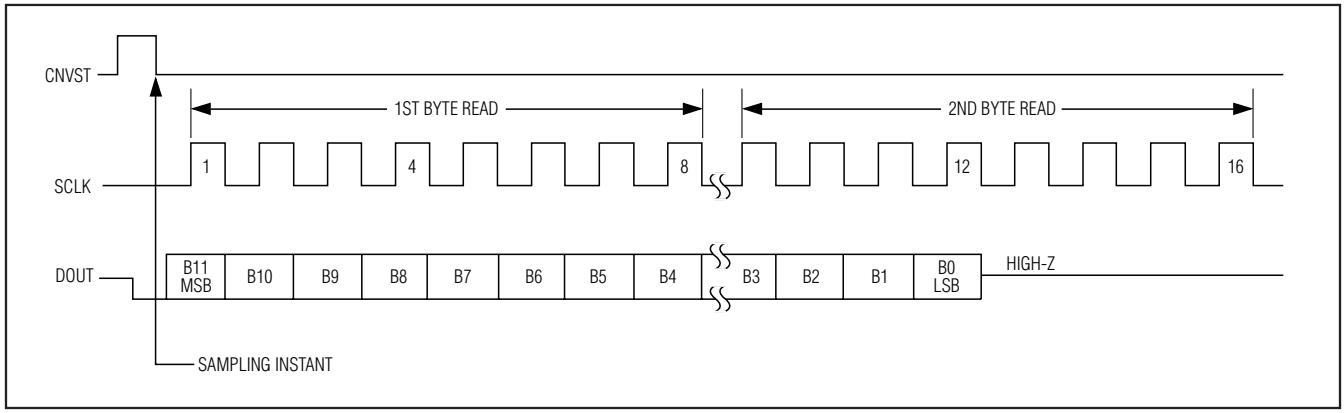


Figure 8c. SPI/MICROWIRE Interface Timing Sequence (CPOL = CPHA = 0)

Layout, Grounding, and Bypassing

For best performance, use printed circuit (PC) boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital PC board ground sections with only one starpoint (Figure 11), connecting the two ground systems (analog and digital). For lowest-noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply (V_{DD}) may degrade the performance of the ADC's fast comparator. Bypass V_{DD} to the star ground with a 0.1µF capacitor, located as close as possible to the MAX1286–MAX1289s' power-supply pin. Minimize capacitor lead length for best supply-noise rejection. Add an attenuation resistor (5Ω) if the power supply is extremely noisy.

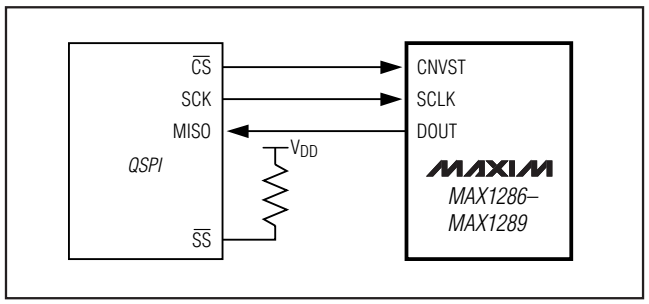


Figure 9a. QSPI Connections

Table 2. Detailed SSPSTAT Register Content

CONTROL BIT		MAX1286–MAX1289 SETTINGS	SYNCHRONOUS SERIAL STATUS REGISTER (SSPSTAT)
SMP	Bit 7	0	SPI Data Input Sample Phase. Input data is sampled at the middle of the data output time.
CKE	Bit 6	1	SPI Clock Edge Select Bit. Data is transmitted on the rising edge of the serial clock.
D/A	Bit 5	X	Data Address Bit
P	Bit 4	X	Stop Bit
S	Bit 3	X	Start Bit
R/W	Bit 2	X	Read/Write Bit Information
UA	Bit 1	X	Update Address
BF	Bit 0	X	Buffer Full Status Bit

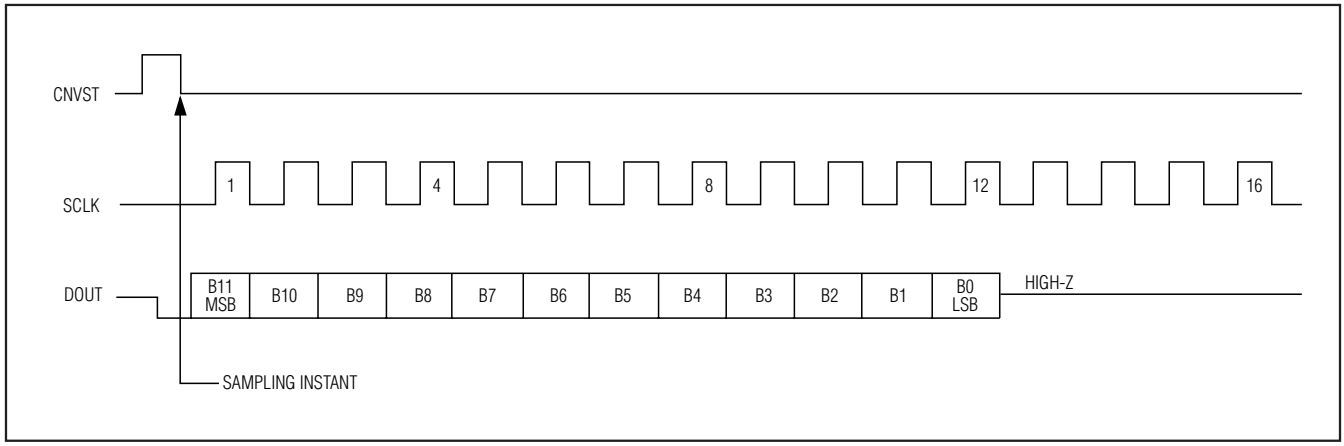


Figure 9b. QSPI Interface Timing Sequence (CPOL = CPHA = 0)

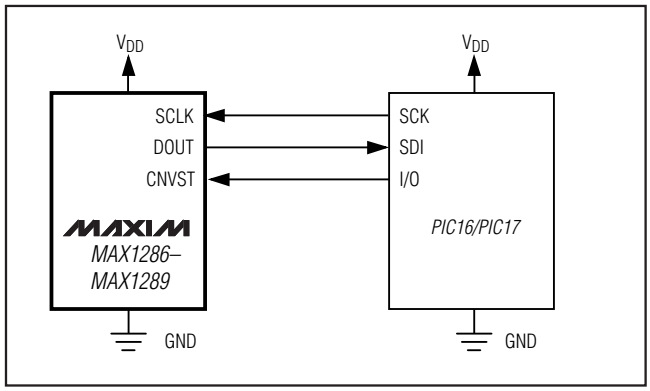


Figure 10a. SPI Interface Connection for a PIC16/PIC17 Controller

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1286–MAX1289 are measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

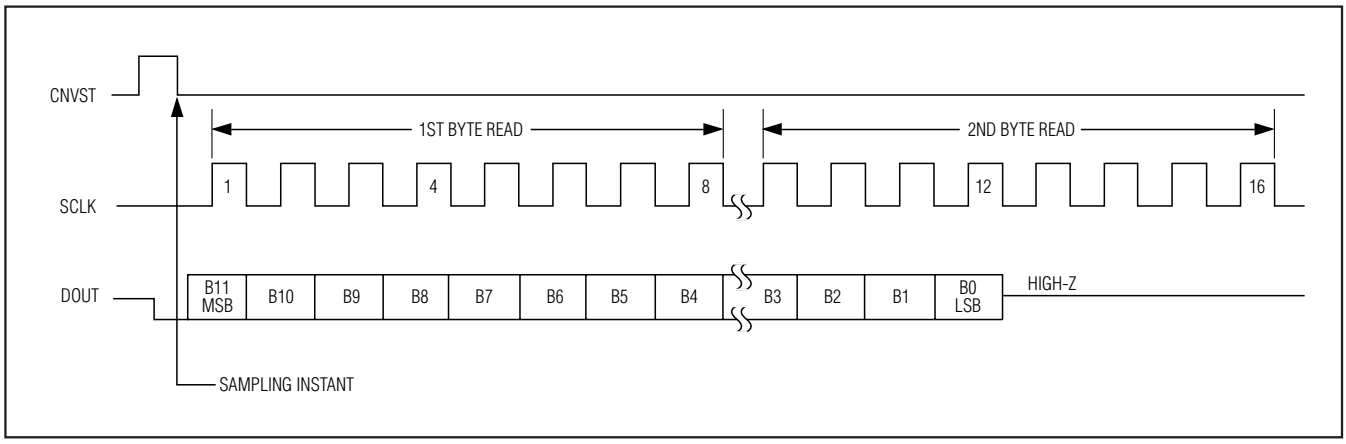


Figure 10b. SPI Interface Timing with PIC16/PIC17 in Master Mode (CKE = 1, CKP = 0, SMP = 0, SSPM3 - SSPM0 = 0001)

150ksps, 12-Bit, 2-Channel Single-Ended, and 1-Channel True-Differential ADCs

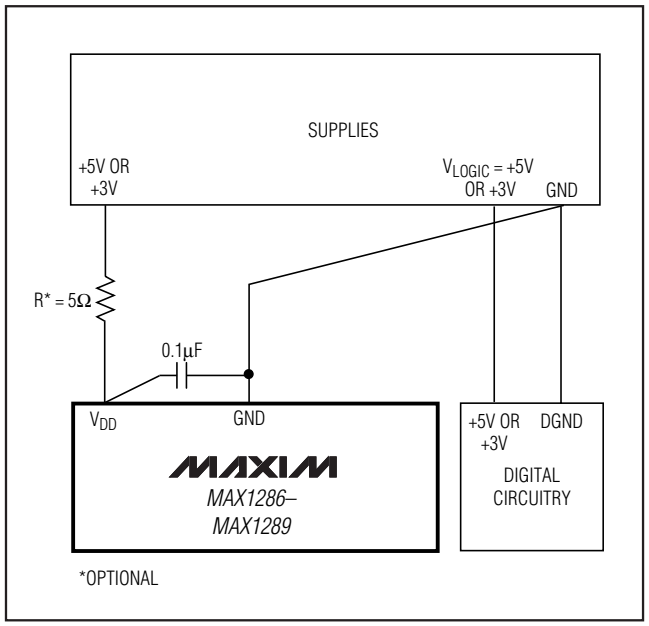


Figure 11. Power-Supply and Grounding Connections

Aperture Definitions

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples. Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD\ (dB) = 20 \times \log\ (Signal_{RMS} / Noise_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\sqrt{\frac{V2^2 + V3^2 + V4^2 + V5^2}{V_1}}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

TRANSISTOR COUNT: 6922

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8F-4	21-0078	90-0176
8 TDFN	T833+2	21-0137	90-0059

Revision History

REVISION	REVISION	DESCRIPTION	PAGES CHANGED
3	8/10	Added exposed pad to TDFN package and soldering temperature	1, 2