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SUMMARY DESCRIPTION

The M68AW256M is a 4 Mbit (4,194,304 bit) CMOS SRAM, organized as 262,144 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW256 is available in TFBGA48 (6x8mm - 6x8 active ball array, 0.75mm pitch), TFBGA48

(7x8mm - 6x8 active ball array, 0.75 mm pitch) and in TSOP44 Type II packages.

In addition to the standard version, both packages are also available in Lead-free version, in compliance with the JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

Figure 2. Logic Diagram

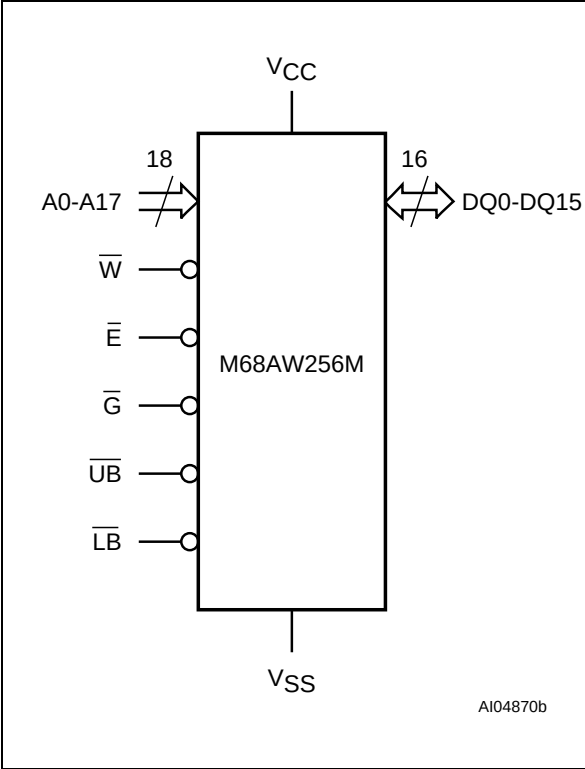


Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
VCC	Supply Voltage
VSS	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TSOP Connections

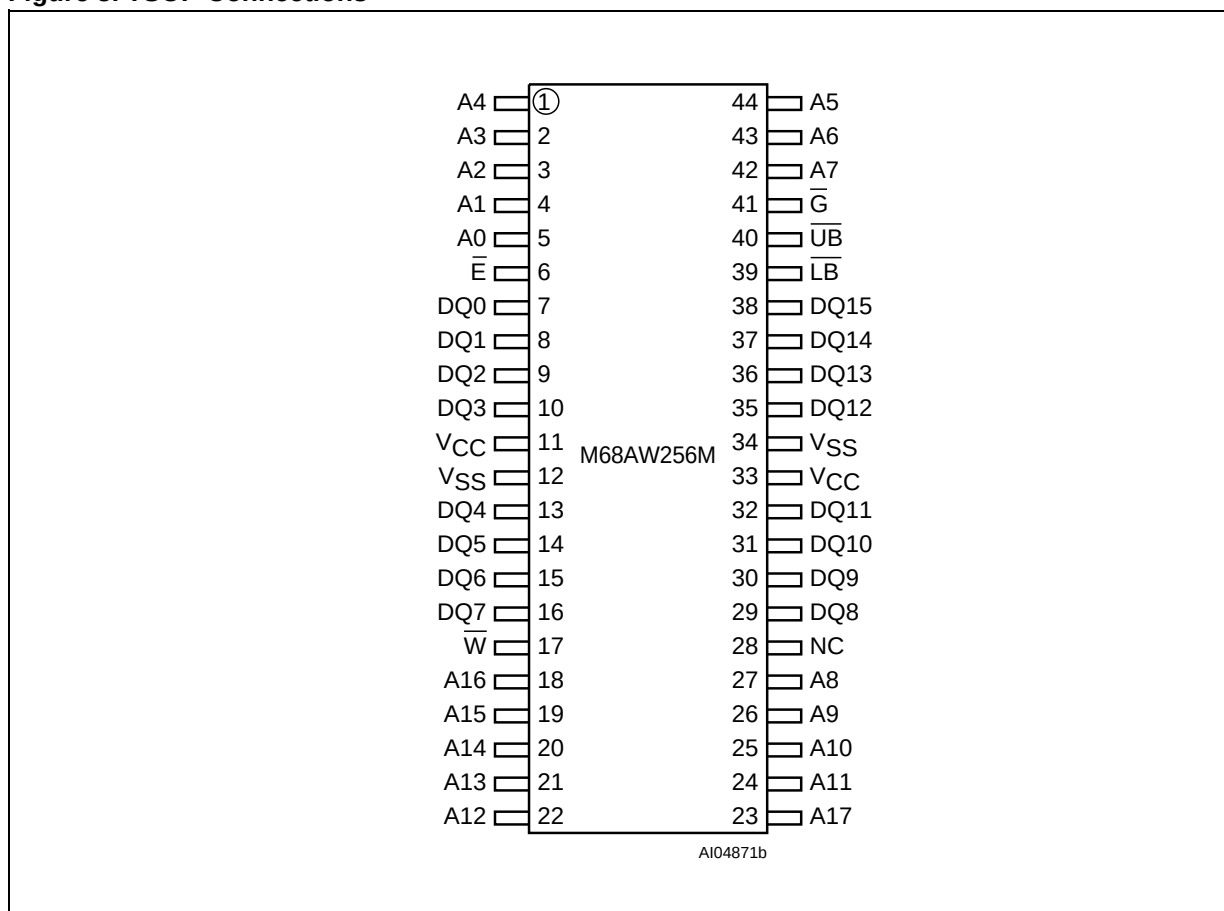


Figure 4. TFBGA Connections (Top view through package)

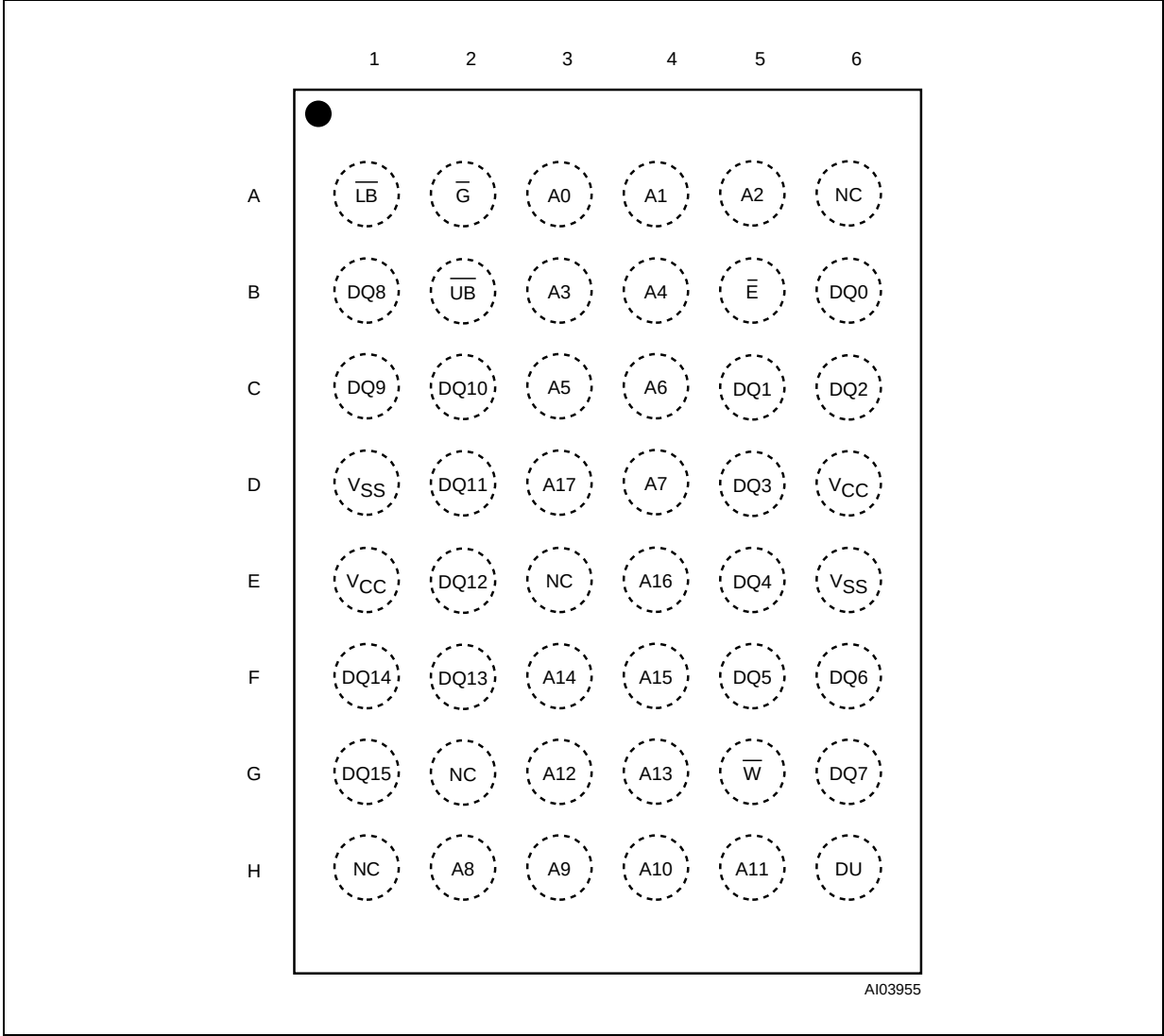
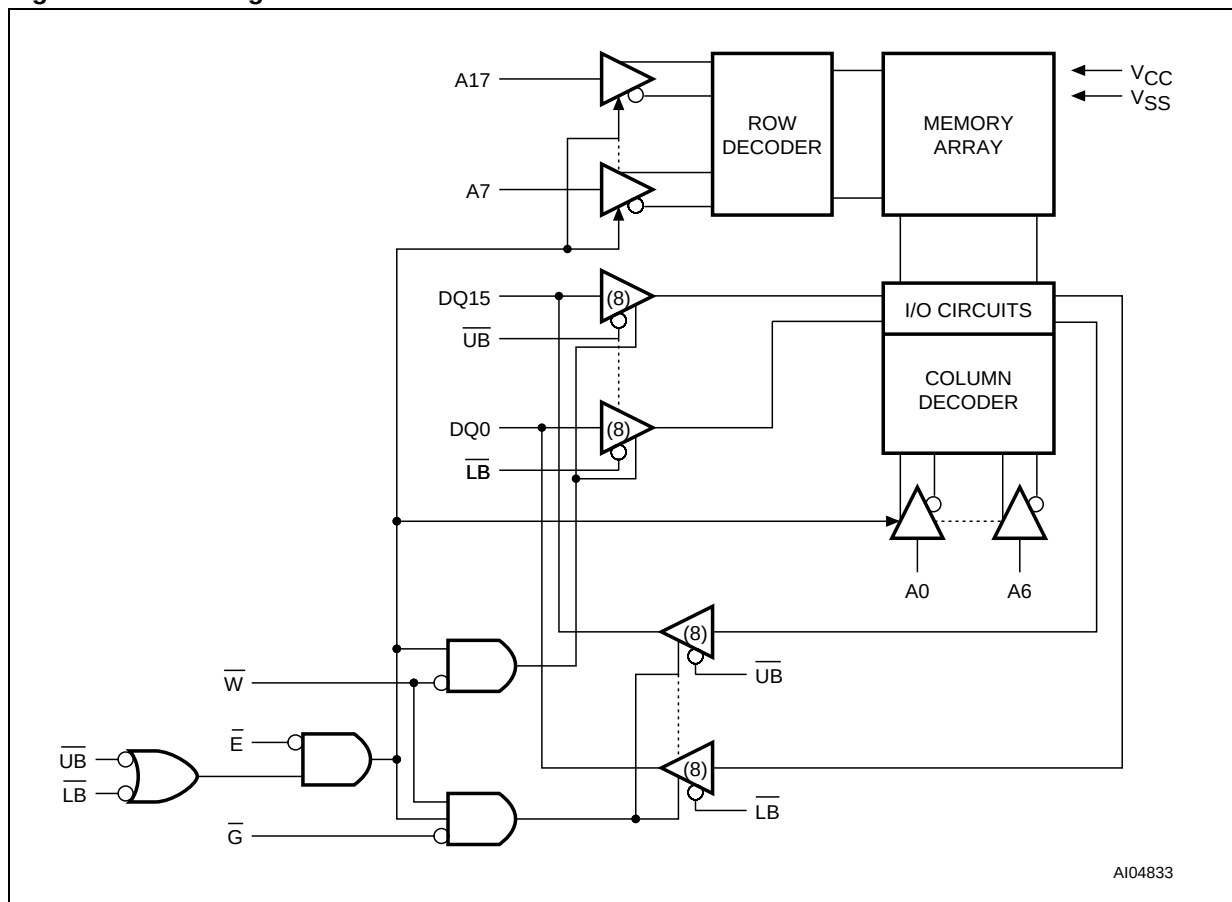


Figure 5. Block Diagram



OPERATION

The device has four standard operating modes:

Output Disabled, Read, Write and Standby/Power-Down. These modes are determined by the control inputs $\overline{E}$, $\overline{W}$, $\overline{G}$, $\overline{LB}$ and $\overline{UB}$ as summarized in Table 2., Operating Modes.

Output Disabled. The Output Enable signal, $\overline{G}$, provides high-speed tri-state control of DQ0-DQ15, allowing fast read/write cycles on the I/O data bus. The device is in Output Disabled mode when Output Enable, $\overline{G}$, is High. In this mode, $\overline{LB}$ and $\overline{UB}$ are Don't care and DQ0-DQ15 are high impedance.

Read Mode. The M68AW256M is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted.

This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 4,194,304 locations in the static memory array, specified by the 18 address inputs. If only one of the Byte Enable inputs is at V_{IL} , the M68AW256M is in Byte Read mode. If the two Byte Enable inputs are at V_{IL} , the M68AW256M is in Word Read mode. So depending on the status of the $\overline{UB}$ and $\overline{LB}$ signals, valid data will be available on the lower eight, the upper eight or all sixteen output pins, t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low.

If either of $\overline{E}$ or $\overline{G}$ is asserted after t_{AVQV} has elapsed, data access will be measured from the limiting parameter (t_{ELQV} , t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} , t_{GLQX} and t_{BLQX} but data lines will always be valid at t_{AVQV} .

Write Mode. The M68AW256M is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E}$ ($\overline{W}$) is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ ($\overline{E}$)'s falling edge. When $\overline{E}$ and $\overline{W}$ are Low, and $\overline{UB} = \overline{LB} = \text{High}$, write cycle begins on the first falling edge of $\overline{UB}$ or $\overline{LB}$. Therefore, address setup time is referenced to Write Enable, Chip Enable or $\overline{UB}/\overline{LB}$ as t_{AVWL} , t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E}$, $\overline{W}$ or $\overline{UB}/\overline{LB}$. If the Output is enabled ($\overline{E} = \text{Low}$, $\overline{G} = \text{Low}$, $\overline{LB}$ or $\overline{UB} = \text{Low}$), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, or for t_{DVBH} before the rising edge of $\overline{UB}/\overline{LB}$ whichever occurs first, and remain valid for t_{WHDX} , t_{EHDX} and t_{BHDX} respectively.

Standby/Power-Down. The M68AW256M has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E} = \text{High}$) or $\overline{LB}$ and $\overline{UB}$ are de-asserted ($\overline{LB}$ and $\overline{UB} = \text{High}$). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 2).

Table 2. Operating Modes

Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected (Standby/Power-Down)	V_{IH}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})
Output Disabled	V_{IH}	X	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})

Note: 1. X = V_{IH} or V_{IL} .

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$I_O^{(1)}$	Output Current	20	mA
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering ⁽²⁾	260 ⁽³⁾	°C
V_{CC}	Supply Voltage	–0.5 to 4.6	V
$V_{IO}^{(4)}$	Input or Output Voltage	–0.5 to $V_{CC} + 0.5$	V
P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.

2. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

3. Not exceeding 250°C for more than 30s, and peaking at 260°C.

4. Up to a maximum operating V_{CC} of 3.6V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter		M68AW256M
V _{CC} Supply Voltage		2.7 to 3.6V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	−40 to 85°C
Load Capacitance (C _L)		30pF
Output Circuit Protection Resistance (R ₁)		3.0kΩ
Load Resistance (R ₂)		3.1kΩ
Input Rise and Fall Times		1ns/V
Input Pulse Voltages		0 to V _{CC}
Input and Output Timing Ref. Voltages		V _{CC} /2
Output Transition Timing Ref. Voltages		V _{RL} = 0.3V _{CC} ; V _{RH} = 0.7V _{CC}

Figure 6. AC Measurement I/O Waveform

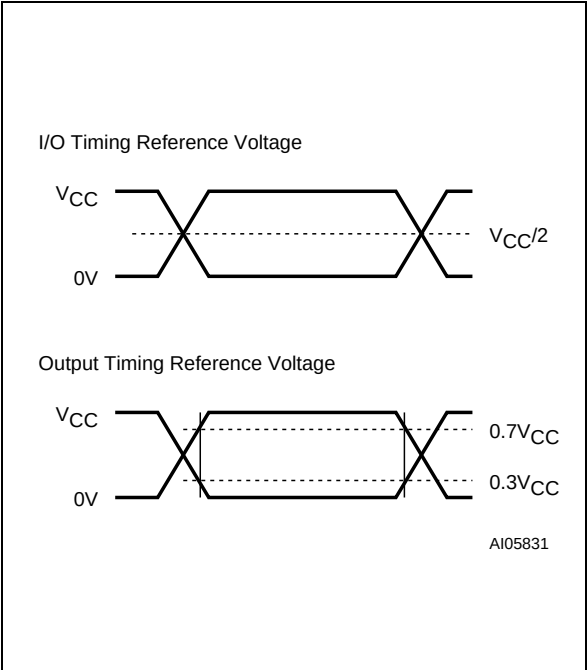


Figure 7. AC Measurement Load Circuit

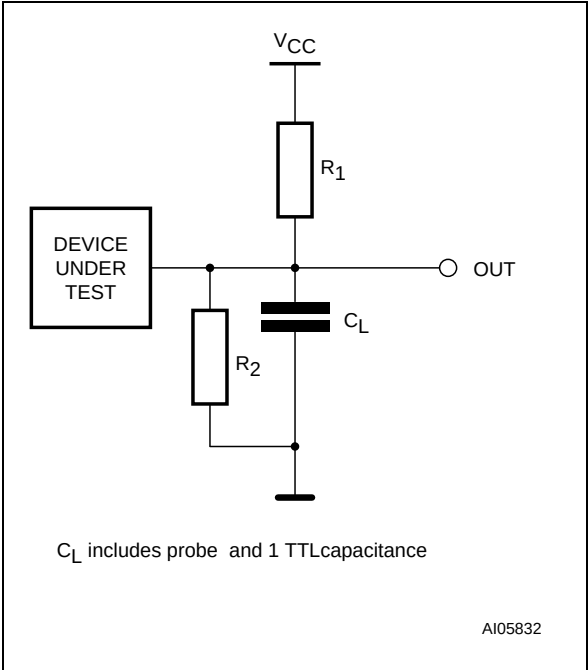


Table 5. Capacitance

Symbol	Parameter ^(1,2)	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance on all pins (except DQ)	V _{IN} = 0V		8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		10	pF

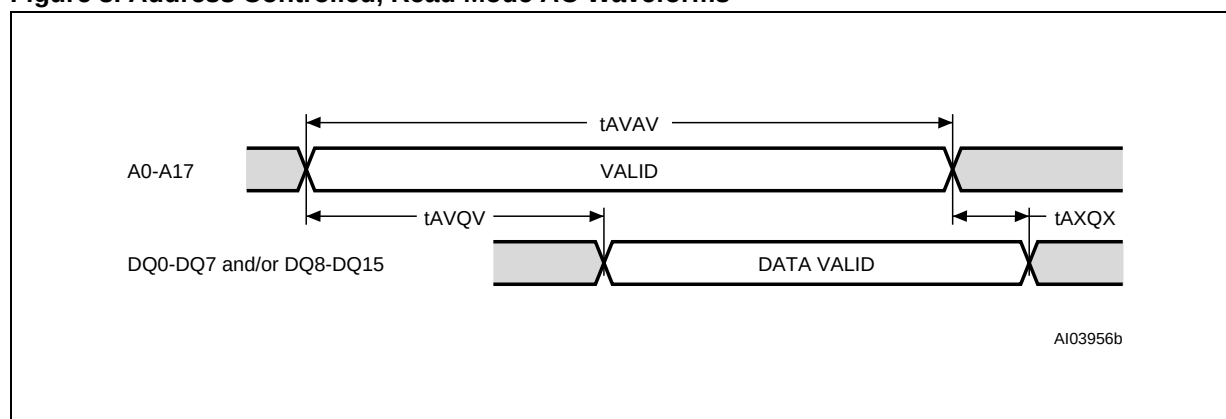
Note: 1. Sampled only, not 100% tested.
 2. At T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V.

Table 6. DC Characteristics

Symbol	Parameter	Test Condition	-L		-N		Unit
			Min	Max	Min	Max	
I _{CC1} ^(1,2)	Operating Supply Current	V _{CC} = 3.6V, f = 1/t _{AVAV} , I _{OUT} = 0mA		20		10	mA
				26		15	
I _{CC2} ⁽³⁾	Operating Supply Current	V _{CC} = 3.6V, f = 1MHz, I _{OUT} = 0mA		2		2	mA
I _{SB}	Standby Supply Current CMOS	V _{CC} = 3.6V, f = 0, $\overline{E} \geq V_{CC} - 0.2V$ or LB=UB $\geq V_{CC} - 0.2V$		20		20	μA
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	-1	1	-1	1	μA
I _{LO}	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC} ⁽⁴⁾	-1	1	-1	1	μA
V _{IH}	Input High Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage		-0.3	0.6	-0.3	0.6	V
V _{OH}	Output High Voltage	I _{OH} = -1.0mA	2.4		2.4		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		0.4		0.4	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
 2. $\overline{E} = V_{IL}$, LB OR/AND UB = V_{IL}, V_{IN} = V_{IL} OR V_{IH}.
 3. E ≤ 0.2V, LB OR/AND UB ≤ 0.2V, V_{IN} ≤ 0.2V OR V_{IN} ≥ V_{CC} - 0.2V.
 4. Output disabled.

Figure 8. Address Controlled, Read Mode AC Waveforms



Note: E = Low, G = Low, W = High, UB = Low and/or LB = Low.

Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AW256M		Unit
			55	70	
t_{AVAV}	Read Cycle Time	Min	55	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	55	70	ns
$t_{AXQX}^{(1)}$	Data hold from address change	Min	5	5	ns
$t_{BHQZ}^{(2,3)}$	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	25	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
$t_{BLQX}^{(1)}$	Upper/Lower Byte Enable Low to Output Transition	Min	5	5	ns
$t_{EHQZ}^{(2,3)}$	Chip Enable High to Output Hi-Z	Max	20	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	55	70	ns
$t_{ELQX}^{(1)}$	Chip Enable Low to Output Transition	Min	5	5	ns
$t_{GHQZ}^{(2,3)}$	Output Enable High to Output Hi-Z	Max	20	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	25	35	ns
$t_{GLQX}^{(2)}$	Output Enable Low to Output Transition	Min	5	5	ns
$t_{PD}^{(4)}$	Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down	Max	0	0	ns
$t_{PU}^{(4)}$	Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up	Min	55	70	ns

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CC}$ or $0.7V_{CC}$.

2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX} , t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.

3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

4. Tested initially and after any design or process changes that may affect these parameters.

Figure 11. Write Enable Controlled, Write AC Waveforms

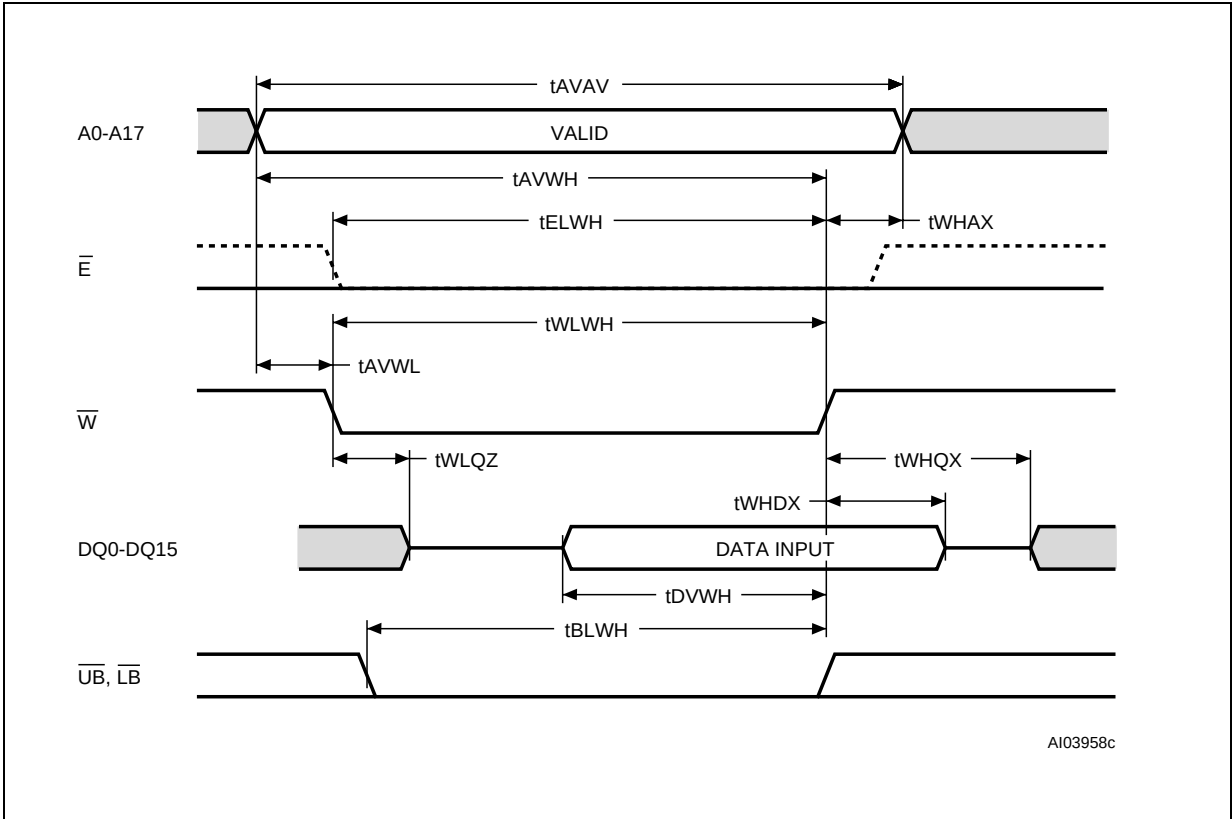


Figure 12. Chip Enable Controlled, Write AC Waveforms

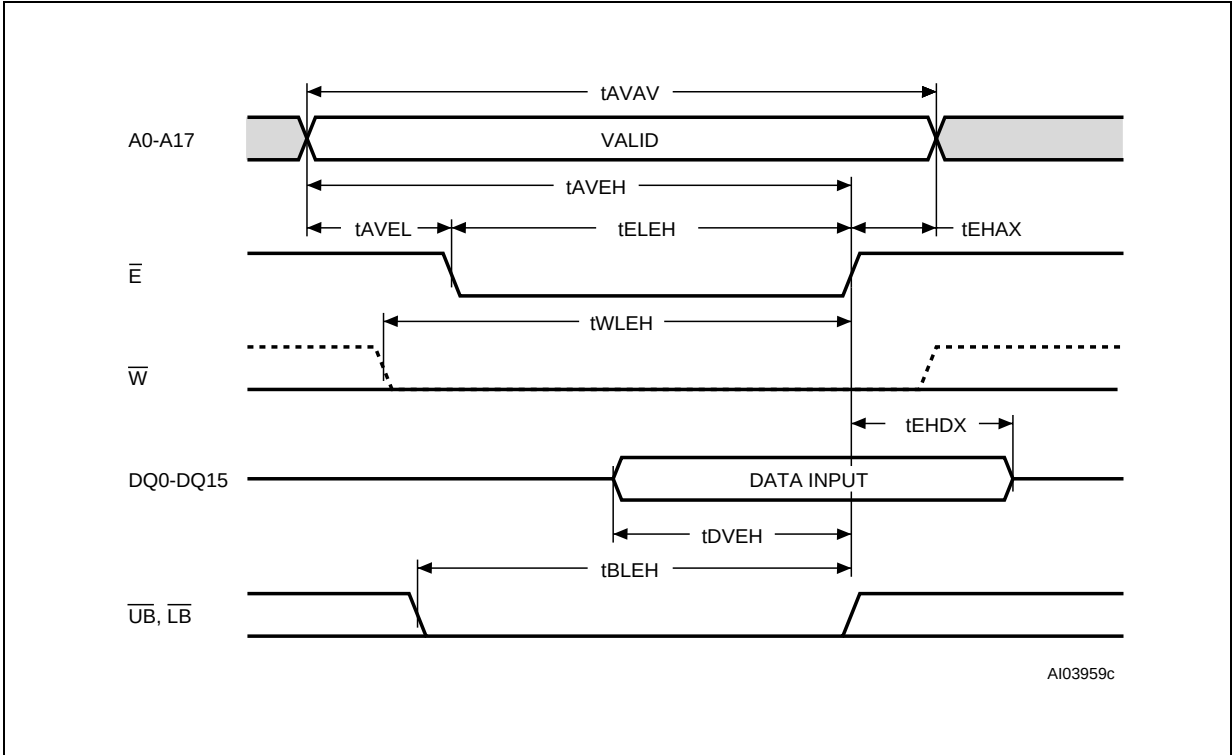
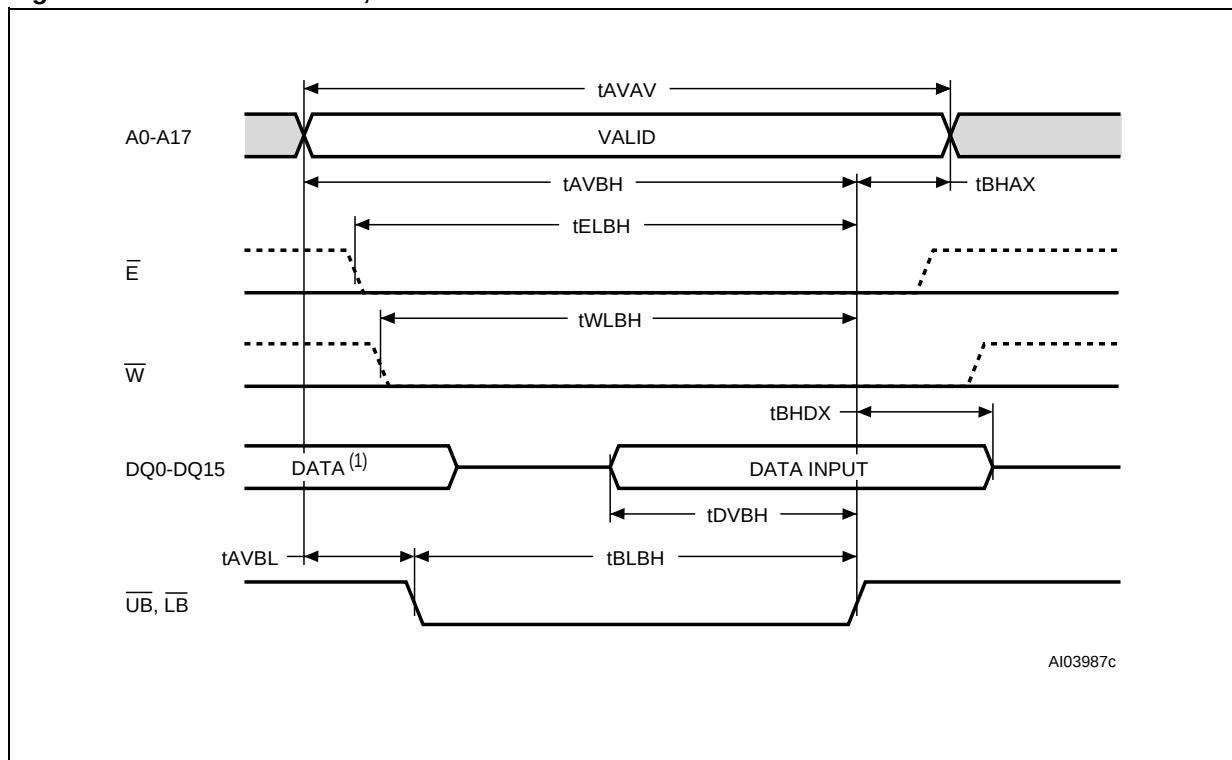


Figure 13. $\overline{\text{UB}}/\overline{\text{LB}}$ Controlled, Write AC Waveforms

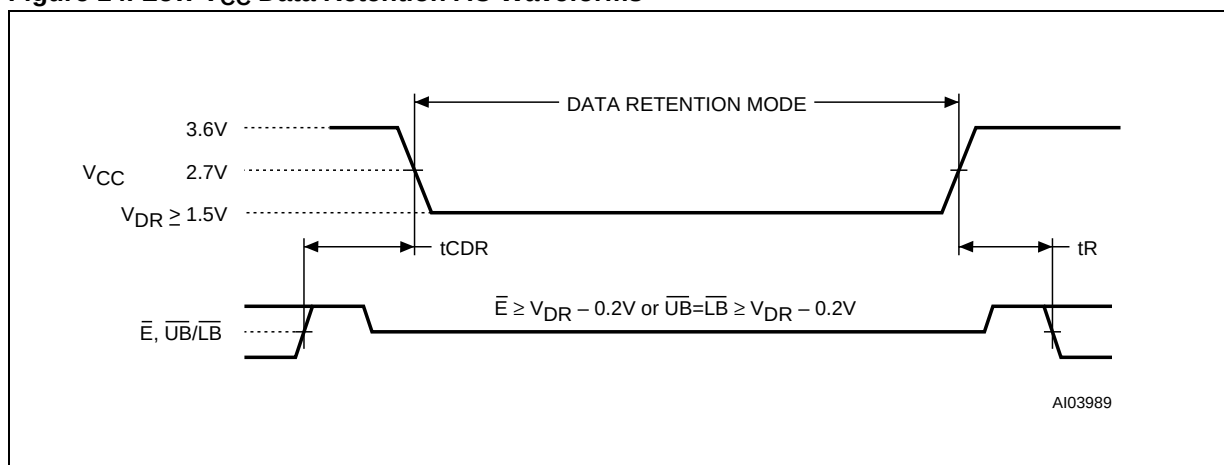
Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AW256M		Unit	
			55	70		
t _{AVAV}	Write Cycle Time	Min	55	70	ns	
t _{AVBH}	Address Valid to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns	
t _{AVBL}	Address Valid to $\overline{LB}$, $\overline{UB}$ Low	Min	0	0	ns	
t _{AVEH}	Address Valid to Chip Enable High	Min	45	60	ns	
t _{AVEL}	Address valid to Chip Enable Low	Min	0	0	ns	
t _{AVWH}	Address Valid to Write Enable High	Min	45	60	ns	
t _{AVWL}	Address Valid to Write Enable Low	Min	0	0	ns	
t _{BHAX}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	Min	0	0	ns	
t _{BHDX}	$\overline{LB}$, $\overline{UB}$ High to Input Transition	Min	0	0	ns	
t _{BLBH}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns	
t _{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	Min	45	60	ns	
t _{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	Min	45	60	ns	
t _{DVBH}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	Min	25	30	ns	
t _{DVEH}	Input Valid to Chip Enable High	Min	25	30	ns	
t _{DVWH}	Input Valid to Write Enable High	Min	25	30	ns	
t _{EHAX}	Chip Enable High to Address Transition	Min	0	0	ns	
t _{EHDX}	Chip enable High to Input Transition	Min	0	0	ns	
t _{ELBH}	Chip Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns	
t _{ELEH}	Chip Enable Low to Chip Enable High	Min	45	60	ns	
t _{ELWH}	Chip Enable Low to Write Enable High	Min	45	60	ns	
t _{WHAX}	Write Enable High to Address Transition	Min	0	0	ns	
t _{WHDX}	Write Enable High to Input Transition	Min	0	0	ns	
t _{WHQX} ⁽¹⁾	Write Enable High to Output Transition	Min	5	5	ns	
t _{WLBH}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	45	60	ns	
t _{WLEH}	Write Enable Low to Chip Enable High	Min	45	60	ns	
t _{WLQZ} ^(1,2)	Write Enable Low to Output Hi-Z	Max	20	20	ns	
t _{WLWH}	Write Enable Low to Write Enable High	-L version	Min	45	60	ns
		-N version	Min	40	50	ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.

2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 14. Low V_{CC} Data Retention AC WaveformsTable 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{CCDR}^{(1)}$	Supply Current (Data Retention)	$V_{CC} = 1.5V, \bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V, f = 0^{(3)}$		4.5	9	μA
$t_{CDR}^{(1,2)}$	Chip Deselected to Data Retention Time		0			ns
$t_R^{(2)}$	Operation Recovery Time		t_{AVAV}			ns
$V_{DR}^{(1)}$	Supply Voltage (Data Retention)	$\bar{E} \geq V_{CC} - 0.2V$ or $\bar{UB} = \bar{LB} \geq V_{CC} - 0.2V, f = 0$	1.5			V

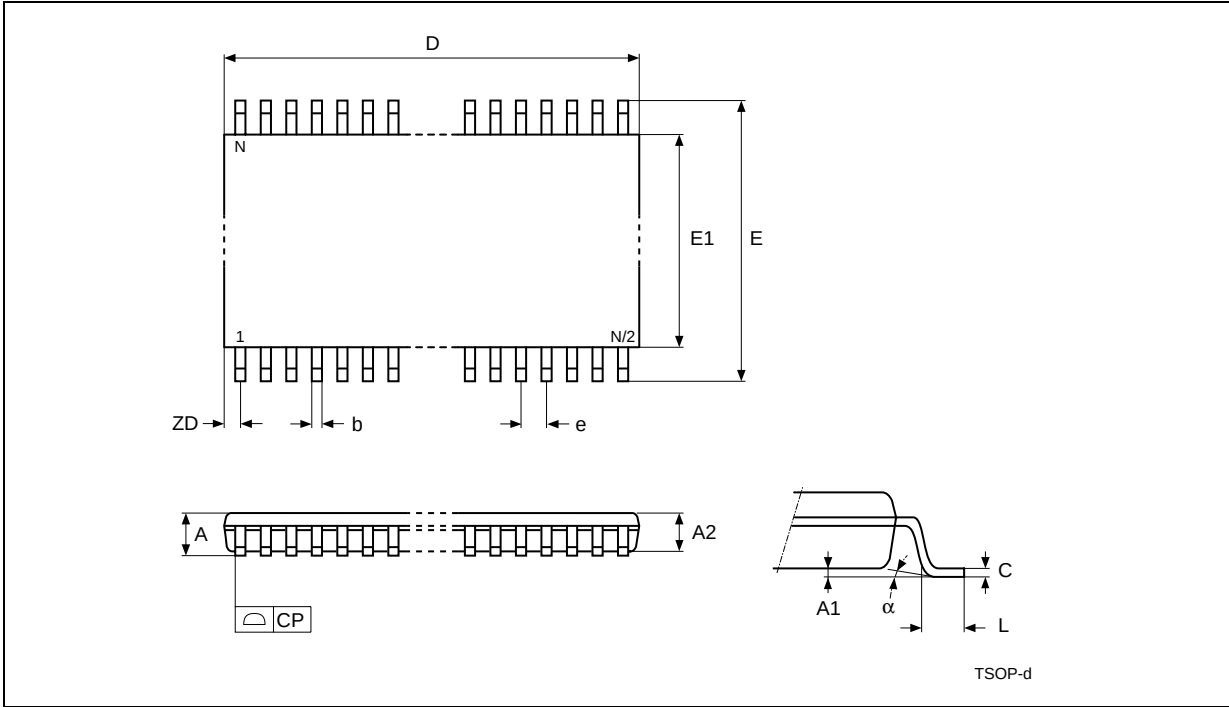
Note: 1. All other Inputs at $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$.

2. Tested initially and after any design or process changes that may affect these parameters. t_{AVAV} is Read cycle time.

3. No input may exceed $V_{CC} + 0.2V$.

PACKAGE MECHANICAL

Figure 15. TSOP44 II - 44 lead Plastic Thin Small Outline Type II, Package Outline

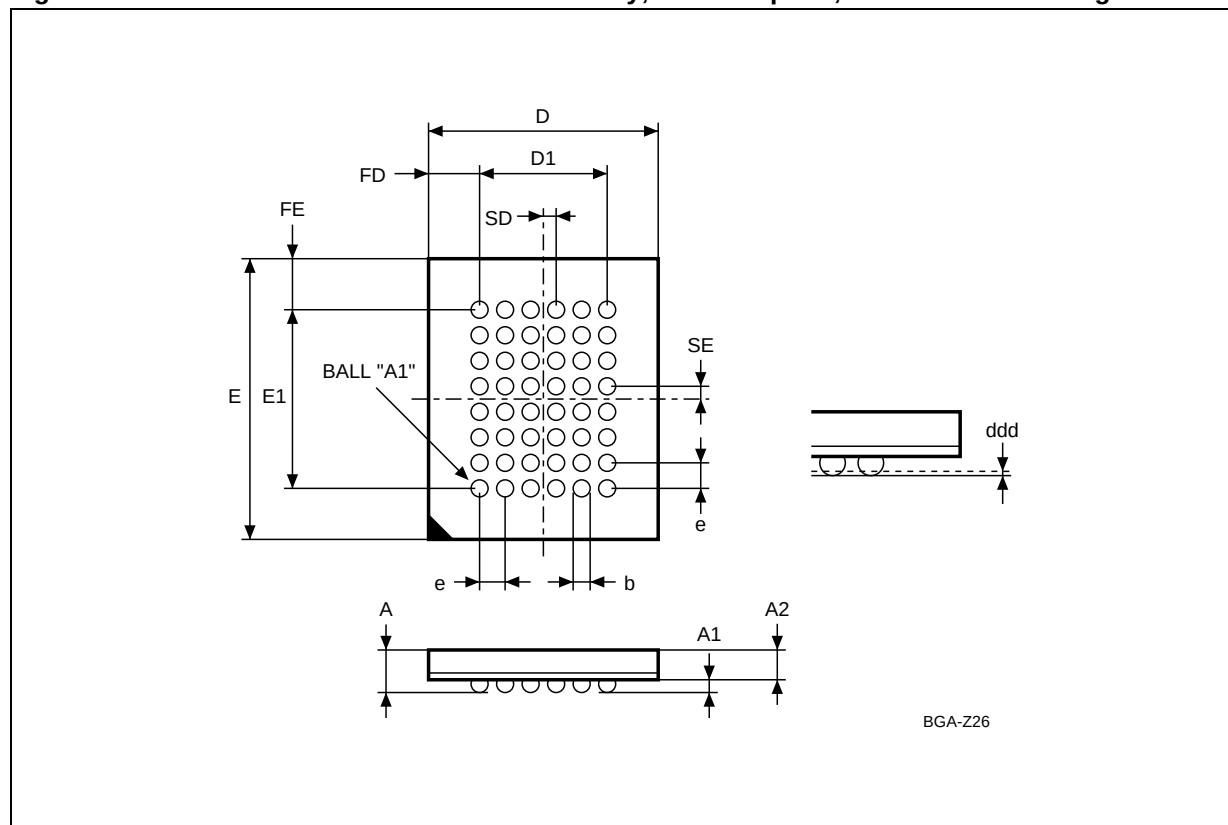


Note: Drawing is not to scale.

Table 10. TSOP 44 II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
b	0.350			0.0138		
c		0.120	0.210		0.0047	0.0083
D	18.410	—	—	0.7248	—	—
E	11.760	—	—	0.4630	—	—
E1	10.160	—	—	0.4000	—	—
e	0.800	—	—	0.0315	—	—
L	0.500	0.400	0.600	0.0197	0.0157	0.0236
ZD	0.805	—	—	0.0317	—	—
alfa		0	5		0	5
CP			0.100			0.0039
N	44			44		

Figure 16. TFBGA48 6x8mm - 6x8 active ball array, 0.75 mm pitch, Bottom View Package Outline

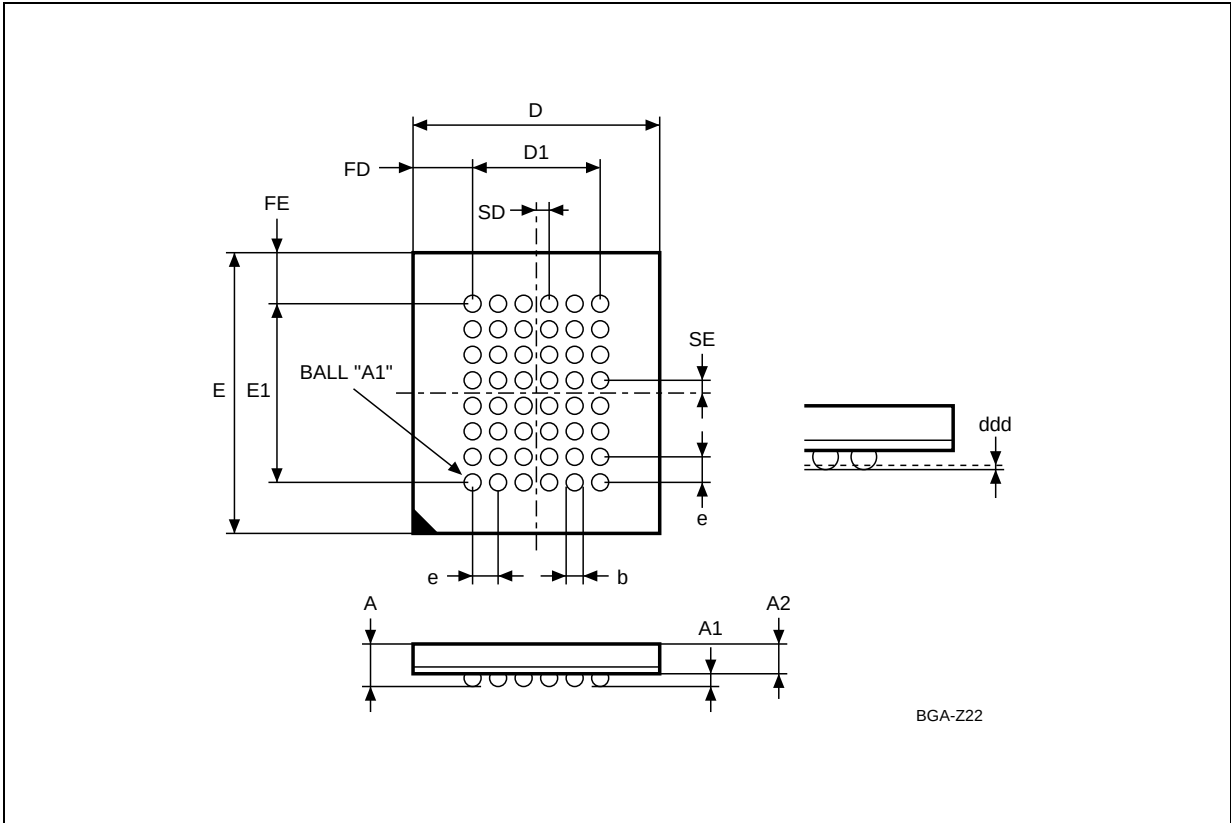


Note: Drawing is not to scale.

Table 11. TFBGA48 6x8mm - 6x8 active ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	—	—	0.1476	—	—
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	—	—	0.2067	—	—
e	0.750	—	—	0.0295	—	—
FD	1.125	—	—	0.0443	—	—
FE	1.375	—	—	0.0541	—	—
SD	0.375	—	—	0.0148	—	—
SE	0.375	—	—	0.0148	—	—

Figure 17. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 12. TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	7.000	6.900	7.100	0.2756	0.2717	0.2795
D1	3.750	—	—	0.1476	—	—
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	—	—	0.2067	—	—
e	0.750	—	—	0.0295	—	—
FD	1.625	—	—	0.0640	—	—
FE	1.375	—	—	0.0541	—	—
SD	0.375	—	—	0.0148	—	—
SE	0.375	—	—	0.0148	—	—

PART NUMBERING

Table 13. Ordering Information Scheme

Example:	M68AW256	M	L	55	ZB	6	T
Device Type							
M68							
Mode							
A = Asynchronous							
Operating Voltage							
W = 2.7 to 3.6V							
Array Organization							
256 = 4 Mbit (256K x16)							
Option 1							
M = 1 Chip Enable; Write and Standby from UB and LB							
Option 2							
L = L-Die							
N = N-Die							
Speed Class							
55 = 55 ns							
70 = 70 ns							
Package							
ND = TSOP 44 Type II							
ZH = TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch							
ZB= TFBGA48 7x8mm - 6x8 ball array, 0.75 mm pitch							
Operative Temperature							
1 = 0 to 70 °C							
6 = -40 to 85 °C							
Shipping							
Blank = Standard Packing (Tray)							
T = Tape & Reel Packing							
E = Lead-Free Package, Standard Packing (Tray)							
F = Lead-Free Package, Tape and Reel Packing							

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 14. Document Revision History

Date	Version	Revision Details
February 2002	-01	First Issue
13-Mar-2002	-02	Tables 4, 7 and 9 clarified Figure 14 clarified
17-Jun-2002	-03	I _{CCDR} clarified (Table 9) I _{SB} clarified (Table 6)
09-Oct-2002	3.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 03 equals 3.0). Part number modified.
20-Feb-2004	4.0	TFBGA48 7x8 replaced by TFBGA48 6x7: Figure 16. , TFBGA48 6x8mm - 6x8 active ball array, 0.75 mm pitch, Bottom View Package Outline and Table 11. , TFBGA48 6x8mm - 6x8 active ball array, 0.75 mm pitch, Package Mechanical Data updated. I _{CC1} and I _{SB} updated in Table 6. , DC Characteristics . t _{WLWH} updated in Table 8. , Write Mode AC Characteristics . Minor content modifications. FEATURES SUMMARY , SUMMARY DESCRIPTION , Table 13. , Ordering Information Scheme updated with Package Lead-free information. TLEAD parameter added in Table 3. , Absolute Maximum Ratings .
27-Apr-2004	5.0	TFBGA48 7x8mm - 6x8 active ball array, 0.75mm pitch reintroduced. TFBGA 6x7mm -6x8mm active ball array replaced by TFBGA48 6x8mm- 6x8 active ball array, 0.75mm pitch.

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