Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} supply voltage	V_{CC}		8 to 23	V
LDOIN input voltage	V_{LDOIN}		8 to 28	V
SW voltage	V_{SW}		-0.3 to 28	V
EN voltage	V_{EN}		0 to 23	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, V_{EN}=V_{CTL}=2V

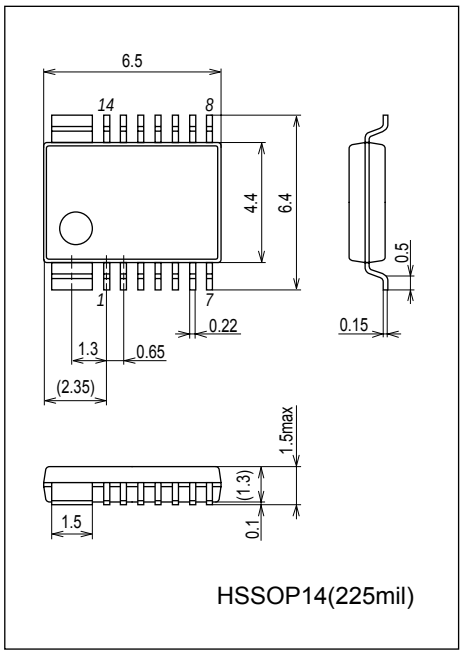
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
ALL						
Supply current	I_{CC}	Switching is turned off		2.1	4.0	mA
	I_{OFF}	EN=0V, LDOIN=0V			10	μA
Reference voltage	VREF			1.26		V
LDO output voltage	LDOOUT1	CTL=High	(-2%)	15.9	(2%)	V
	LDOOUT2	CTL=Low	(-2%)	11.7	(2%)	V
DCDC output voltage	DCDCOUT1	CTL=High	(-2%)	16.5	(2%)	V
	DCDCOUT2	CTL=Low	(-2%)	12.3	(2%)	V
Enable voltage	V_{EN}		2.0			V
Disable voltage	V_{DIS}				0.4	V
EN input current	I_{EN}	V_{EN}=2.0V			10	μA
PGOOD threshold	V_{PG}	Power-good output is “good” when LDO is 85% or higher of the setting value.		85		%
PGOOD sink current	I_{PG}	Where power-good output is “no good” and V_{PGOOD}=0.5V.		1.0		mA
PGOOD leak current	$I_{PG}LK$	Where power-good output is “good” and V_{PGOOD}=2V			10	μA
PGDLY source current	I_{PGDLY}		3.84	4.8	5.76	μA
PGDLY threshold	V_{PGDLY}			1.26		V
CTL high voltage	$V_{CTL}H$	15V output setting	2.0			V
CTL low voltage	$V_{CTL}L$	11V output setting			0.4	V
CTL input current	I_{CTL}	V_{CTL}=2V			20	μA
UVLO on voltage	V_{UVLO}			7.0		V
Thermal shutdown temperature	TTSD	*2		155		°C
TSD hysteresis	THYS	*2		30		°C
DC/DC boost converter						
FB output voltage “Low”	FB low	IN=2.0V, I_{FB}=-20μA (sink)			0.2	V
FB output voltage “High”	HB high	IN=2.0V, I_{FB}=20μA (source)	1.8			V
Soft-start time	TSS			2.6		ms
Oscillator frequency	f_{OSC}			1		MHz
Max ON duty	D max			85		%
SW ON resistance	R_{ON}			0.7		Ω
SW peak current	I_{PK}			1.8		A
SCP timer	t_{SCP}			1.6		ms
LDO						
Maximum output current	IO max		450	620	800	mA
Line regulation	R_{LN}	16.5V ‹ LDOIN ‹ 21.5V			20	mV
Load regulation	R_{LD}	10mA ‹ I_O ‹ 300mA			50	mV
Dropout voltage	V_{DROP}	I_O=400mA		0.35	0.5	V
Short current	I_{SHORT}	LDOOUT=GND			100	mA

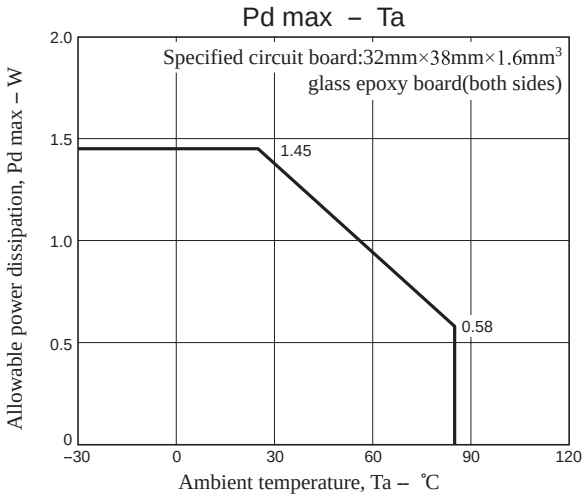
*2: Design guarantee value.

Package Dimensions

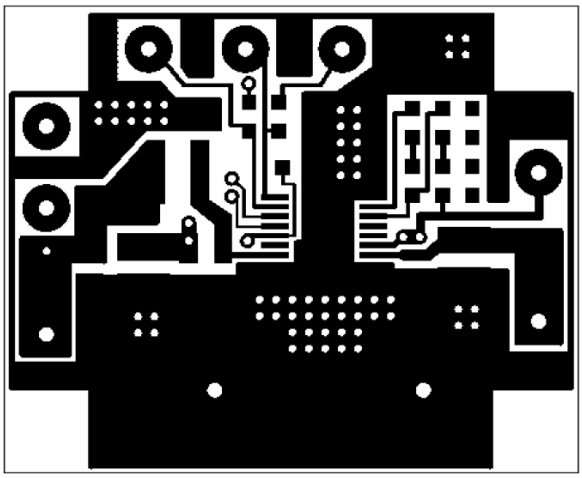
unit : mm (typ)

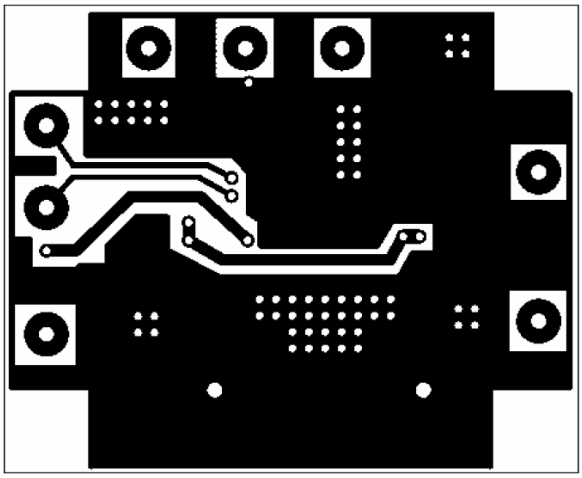
3313



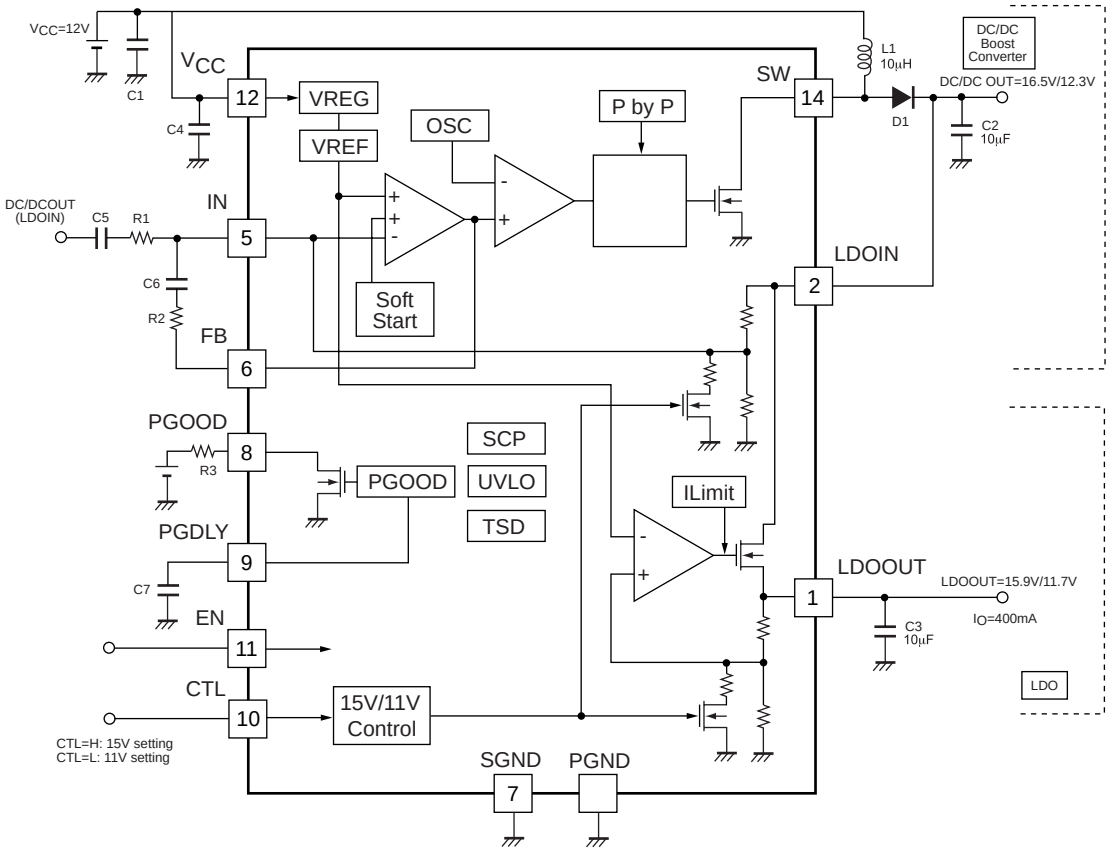


Specified board (32mm×38mm×1.6mm, glass epoxy, double side board)



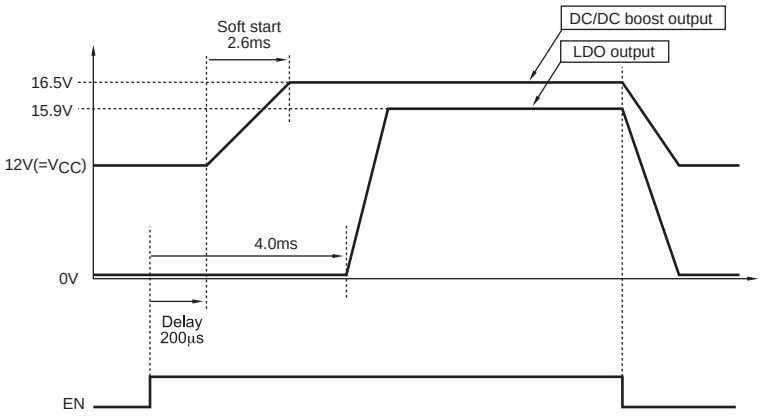


Block diagram and Application circuit

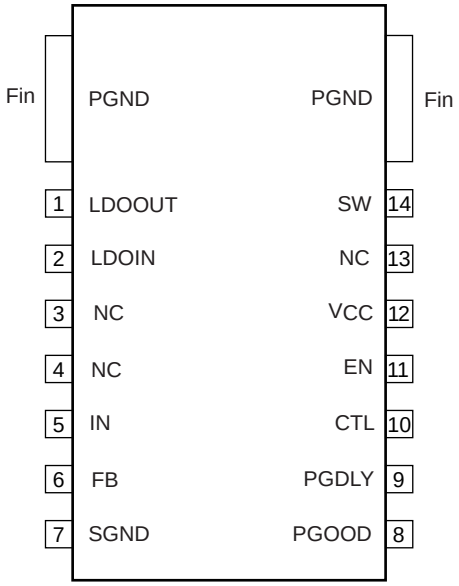


Start and stop

Output waveform during start and stop is shown below.

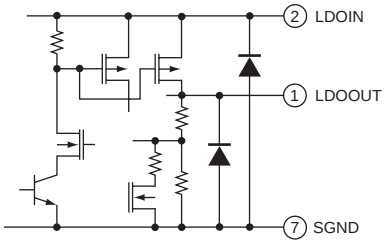
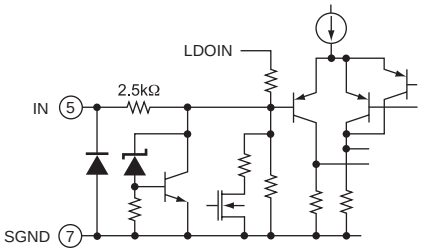
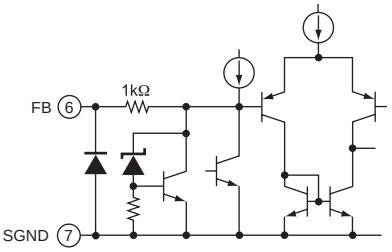
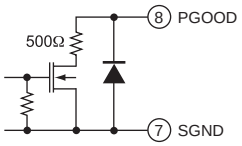


Pin arrangement



Top view

Pin function

Pin No.	Pin name	Function	Equivalent circuit
1 2 7	LDOOUT LDOIN SGND	LDO output LDO input Signal ground	
5	IN	DC/DC error amplifier input	
6	FB	DC/DC error amplifier output	
8	PGOOD	Power good output	

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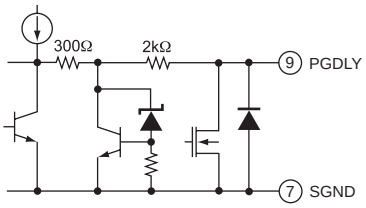
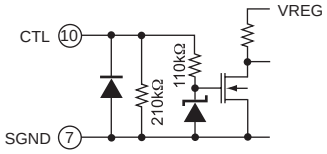
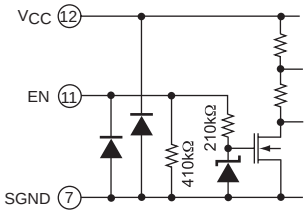
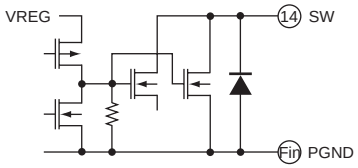
Pin No.	Pin name	Function	Equivalent circuit
9	PGDLY	PGDLY capacitor connection pin for delay time setting	
10	CTL	15V, 11V output voltage switching	
11 12	EN V_{CC}	Enable Power supply	
14 Fin	SW PGND	DC/DC open drain output Power ground	

Function overview

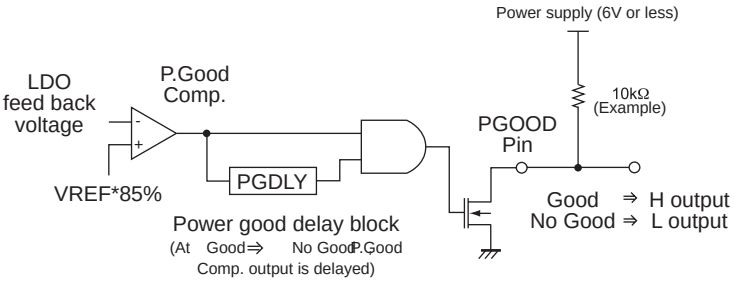
(1) UVLO (Under Voltage Lockout)

UVLO stops outputs of both DC/DC and to LDO to prevent malfunction when V_{CC} decreases. UVLO operates when V_{CC} falls below the UVLO voltage. This function is a non-latch-type, and recovers these outputs automatically when V_{CC} exceeds the UVLO voltage.

(2) Power good

Power good notifies that the output voltage of LDO is within the range of the setting voltage. The output is judged to be "power good" when both outputs are 85% or higher compared to the setting voltages. If the output voltage falls below 85%, PGOOD output becomes H→L (No Good). At "Good"→"No Good", delay time can be set. It explains this at (3). When EN=L (OFF), PGOOD output is H.

[Power good circuit diagram]

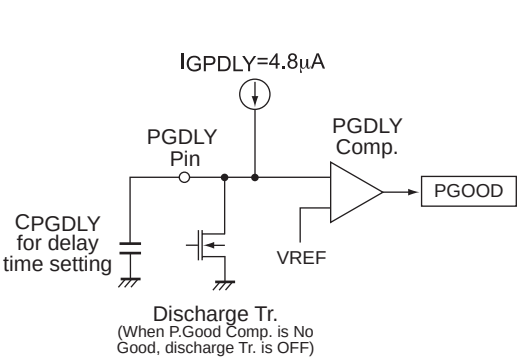


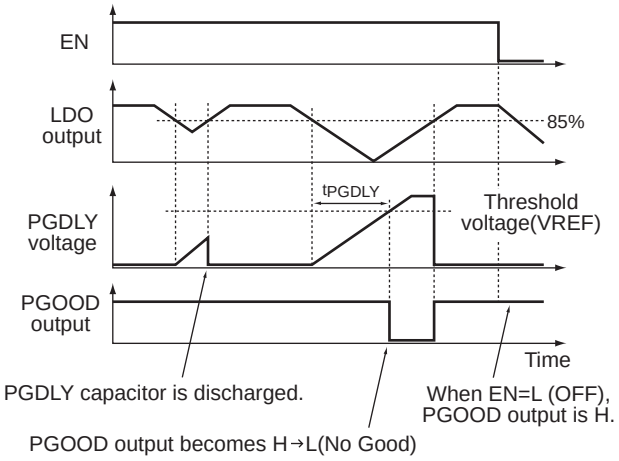
(3) Power good delay

If the output voltage of LDO falls below 85%, charge at 4.8μA constant starts to PGDLY capacitor for delay time setting. When PGDLY voltage exceeds the threshold voltage (=VREF), PGOOD voltage reaches to the threshold voltage, PGDLY capacitor using the following formula because delay time (t_{PGDLY}) depends on capacitance.

$$C_{PGDLY} = (I_{PGDLY} \times t_{PGDLY}) / VREF$$

[PGDLY circuit diagram]

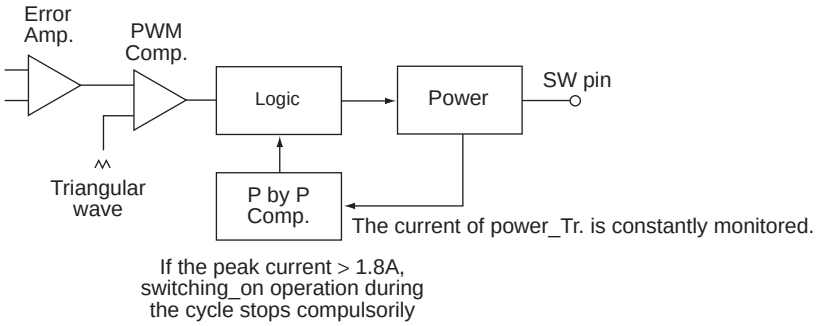




(4) Pulse-by-Pulse over current protection (P by P)

The P by P stops switch-on operation of a certain cycle by force when the current of power MOSFET reaches the maximum output peak current.

[P by P circuit diagram]



(5) Short circuit protector (SCP)

When output voltage of DC/DC decreases due to short-circuit; for example, SCP latches off the outputs of DC/DC and LDO by timer.

When output voltage of DC/DC decreases and FB that is the error amplifier output turns to H, the internal counter starts, latch-off occurs after 1.6ms.

To restart the output after latch-off, you need to input EN signal again.

(6) Output voltage switching function

Where CTL=High, 15V output setting is selected.

Where CTL=Low, 11V output setting is selected.