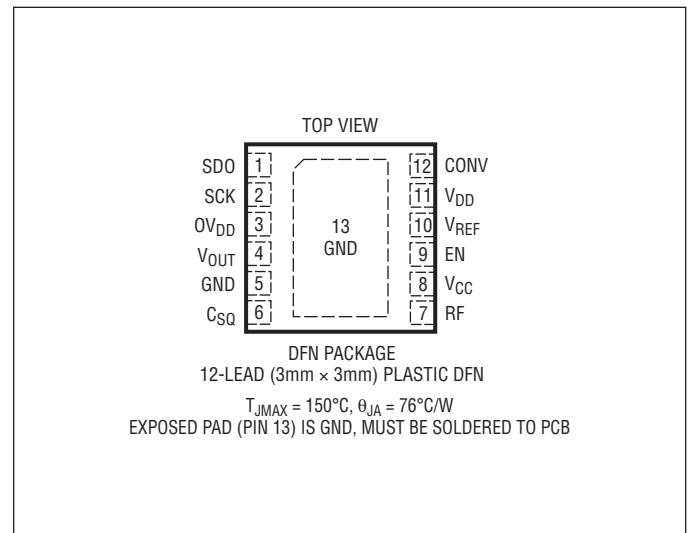


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{DD}$ , $V_{CC}$ Voltage, (Note 12)	4V
$OV_{DD}$ Supply Voltage	$\text{Min}(V_{DD} + 0.3V, 4V)$
Maximum Input Signal Power (Average)	15dBm
Maximum Input Signal Power (Peak)	25dBm
DC Voltage at RF	-0.3V to 2V
$V_{OUT}$ Voltage	-0.3V to $V_{DD} + 0.3V$
EN Voltage	-0.3V to $V_{DD} + 0.3V$
SDO, SCK, CONV Voltage	-0.3V to $V_{DD} + 0.3V$
$V_{REF}$ Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation	100mW
Maximum Junction Temperature, $T_{JMAX}$	150°C
Operating Temperature Range (Note 2)	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C

## PIN CONFIGURATION



Caution: This part is sensitive to electrostatic discharge. It is very important that proper ESD precautions be observed when handling the LTC5587.

## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5587IDD#PBF	LTC5587IDD#TRPBF	LFRH	12-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$  (Note 2).  $V_{CC} = V_{DD} = OV_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted. Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>RF Input</b>					
Input Frequency Range (Note 4)			10 to 6000		MHz
Input Impedance			205  1.6		$\Omega  pF$
<b><math>f_{RF} = 450\text{MHz}</math></b>					
RF Input Power Range	Externally Matched to 50 $\Omega$ Source		-34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	$\pm 1\text{dB}$ Linearity Error		40		dB
Linear Dynamic Range, CDMA (Note 3)	$\pm 1\text{dB}$ Linearity Error; CDMA 4-Carrier		40		dB
Output Slope			73		LSB/dB
Logarithmic Intercept (Note 5)			-42		dBm
Output Variation vs Temperature	Normalized to Output at 25°C; $P_{IN} = -34\text{dBm}$ to 6dBm		$\pm 1$		dB

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2).  $V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted. Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -27\text{dBm}$ to $-10\text{dBm}$		$\pm 0.5$		dB
Deviation from CW Response; $P_{IN} = -34\text{dBm}$ to $0\text{dBm}$	TETRA $\pi/4$ DQPSK		$\pm 0.1$		dB
	CDMA 4-Carrier 64-Channel Fwd 1.23Mcps		$\pm 0.5$		dB
2nd Order Harmonic Distortion	At RF Input; CW Input; $P_{IN} = 0\text{dBm}$		-57		dBc
3rd Order Harmonic Distortion	At RF Input; CW Input; $P_{IN} = 0\text{dBm}$		-52		dBc
<b><math>f_{RF} = 880\text{MHz}</math></b>					
RF Input Power Range	CW Input: Externally Matched to $50\Omega$ Source		-34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	$\pm 1\text{dB}$ Linearity Error		40		dB
Linear Dynamic Range, EDGE (Note 3)	$\pm 1\text{dB}$ Linearity Error; EDGE $3\pi/8$ -Shifted 8PSK		40		dB
Output Slope			73		LSB/dB
Logarithmic Intercept (Note 5)			-42		dBm
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -34\text{dBm}$ to $6\text{dBm}$		$\pm 1$		dB
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -27\text{dBm}$ to $-10\text{dBm}$		$\pm 0.5$		dB
Deviation from CW Response; $P_{IN} = -34\text{dBm}$ to $6\text{dBm}$	EDGE $3\pi/8$ Shifted 8PSK		$\pm 0.1$		dB
<b><math>f_{RF} = 2140\text{MHz}</math></b>					
RF Input Power Range	CW Input: Externally Matched to $50\Omega$ Source		-34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	$\pm 1\text{dB}$ Linearity Error		43		dB
Linear Dynamic Range, WCDMA (Note 3)	$\pm 1\text{dB}$ Linearity Error; 4-Carrier WCDMA		37		dB
Output Slope			73		LSB/dB
Logarithmic Intercept (Note 5)			-42		dBm
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -34\text{dBm}$ to $6\text{dBm}$		$\pm 1$		dB
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -27\text{dBm}$ to $-10\text{dBm}$		$\pm 0.5$		dB
Deviation from CW Response; $P_{IN} = -34\text{dBm}$ to $-4\text{dBm}$	WCDMA 1-Carrier Uplink		$\pm 0.1$		dB
	WCDMA 64-Channel 4-Carrier Downlink		$\pm 0.5$		dB
<b><math>f_{RF} = 2600\text{MHz}</math></b>					
RF Input Power Range	CW Input: Externally Matched to $50\Omega$ Source		-34 to 6		dBm
Linear Dynamic Range, CW (Note 3)	$\pm 1\text{dB}$ Linearity Error		40		dB
Output Slope			73		LSB/dB
Logarithmic Intercept (Note 5)			-42		dBm
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -34\text{dBm}$ to $6\text{dBm}$		$\pm 1$		dB
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -27\text{dBm}$ to $-10\text{dBm}$		$\pm 0.5$		dB
Deviation from CW Response; $P_{IN} = -34\text{dBm}$ to $2\text{dBm}$	WiMax OFDMA Preamble		$\pm 0.1$		dB
	WiMax OFDM Burst		$\pm 0.5$		dB
<b><math>f_{RF} = 3500\text{MHz}</math></b>					
RF Input Power Range	CW Input: Externally Matched to $50\Omega$ Source		-30 to 6		dBm
Linear Dynamic Range, CW (Note 3)	$\pm 1\text{dB}$ Linearity Error		36		dB
Output Slope			73		LSB/dB
Logarithmic Intercept (Note 5)			-40		dBm

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2).  $V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted. Test circuit is shown in Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -30\text{dBm}$ to $6\text{dBm}$		$\pm 1$		dB
Output Variation vs Temperature	Normalized to Output at $25^\circ\text{C}$ ; $P_{IN} = -27\text{dBm}$ to $-10\text{dBm}$		$\pm 0.5$		dB
Deviation from CW Response; $P_{IN} = -34\text{dBm}$ to $-4\text{dBm}$	WiMax OFDMA Preamble WiMax OFDM Burst		$\pm 0.1$ $\pm 0.5$		dB dB

#### Detector Analog Output

Output DC Voltage at $V_{OUT}$	No Signal Applied to RF Input		180		mV
Output Impedance	Internal Series Resistor Allows for Off-Chip Filter Cap		300		$\Omega$
Output Current Sourcing/Sinking			5/5		mA
Rise Time (1000pF on $V_{OUT}$ )	0.2V to 1.6V, 10% to 90%, $f_{RF} = 2140\text{MHz}$		1		$\mu\text{sec}$
Fall Time (1000pF on $V_{OUT}$ )	1.6V to 0.2V, 10% to 90%, $f_{RF} = 2140\text{MHz}$		8		$\mu\text{sec}$
Power Supply Rejection Ratio (Note 6)	For CW RF Input Over Operating Input Power Range		49		dB
Integrated Output Voltage Noise	1 to 6.5 kHz Integration BW, $P_{IN} = 0\text{dBm}$ CW		150		$\mu\text{V}_{RMS}$
Peak-to-Peak ADC Output Noise	$C_{FILT} = 1000\text{pF}$ , $P_{IN} = 0\text{dBm}$ CW		11		LSB

#### ADC Resolution

ADC Resolution	(No Missing Codes)	●	12		Bits
Differential Linearity Error	$EN = 0V$ , Voltage on $V_{OUT} = 0V$ to $1.8V$ , $V_{REF} = 1.8V$	●	$\pm 0.25$	$\pm 1$	LSB
Measurement Resolution	$1\text{LSB} = V_{REF}/(4096 \cdot 32\text{mV/dB})$ , $V_{REF} = 1.8V$		0.014		dB/Bit

#### ADC Digital Timing

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	(Notes 8, 9)	●	500		kHz
$f_{SCK}$	Shift Clock Frequency	(Notes 8, 9)	●		50	MHz
$t_{SCK}$	Shift Clock Period		●	20		ns
$t_{THROUGHPUT}$	Minimum Throughput Time, $t_{ACQ} + t_{CONV}$		●		2	$\mu\text{s}$
$t_{ACQ}$	Acquisition Time		●	0.5		$\mu\text{s}$
$t_{CONV}$	Conversion Time		●	1.5		$\mu\text{s}$
$t_1$	Minimum Positive CONV Pulse Width	(Note 8)	●	1.5		$\mu\text{s}$
$t_2$	$SCK \uparrow$ Setup Time After $CONV \downarrow$	(Note 8)	●	16		ns
$t_3$	SDO Enabled Time After $CONV \downarrow$	(Notes 8, 9)	●		16	ns
$t_4$	SDO Data Valid Access Time After $SCK \downarrow$	(Notes 8, 9, 10)	●		8	ns
$t_5$	$SCK$ Low Time	(Note 7)	●	40%		$t_{SCK}$
$t_6$	$SCK$ High Time	(Note 7)	●	40%		$t_{SCK}$
$t_7$	SDO Data Valid Hold Time After $SCK \downarrow$	(Notes 8, 9, 10)	●	4		ns
$t_8$	SDO Into Hi-Z State Time After $CONV \uparrow$	(Notes 8, 9)		6		ns

#### ADC Digital Inputs and Outputs

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IH}$	$SCK$ , $CONV$ Logic High Input	●	2			V
$V_{IL}$	$SCK$ , $CONV$ Logic Low Input	●			0.8	V
$I_{IH}$	Logic High Input Current	$SCK$ , $CONV = V_{DD}$	●		2.5	$\mu\text{A}$
$I_{IL}$	Logic Low Input Current	$SCK$ , $CONV = 0V$	●	-2.5		$\mu\text{A}$

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2).  $V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted. Test circuit is shown in Figure 1.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN}$	SCK, CONV Input Capacitance			2		pF
$V_{OH}$	SDO Logic High Output	$I_{SOURCE} = 200\mu A$	●	$V_{DD} - 0.2$		V
$V_{OL}$	SDO Logic Low Output	$I_{SINK} = 200\mu A$	●		0.2	V
$I_{OZ}$	Hi-Z Output Leakage	$CONV = V_{DD}$	●		$\pm 3$	$\mu A$
$C_{OZ}$	Hi-Z Output Capacitance	$CONV = V_{DD}$		4		pF
$I_{SOURCE}$	SDO Source Current	SDO Connected to GND = 0V		-10		mA
$I_{SINK}$	SDO Sink Current	SDO Connected to $V_{DD}$		10		mA

**Detector Enable (EN) Low = Off, High = On**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input High Voltage (On)		●	2		V
EN Input Low Voltage (Off)		●		0.3	V
Enable Pin Input Current	$EN = 3.3V$		25		$\mu A$
Turn ON Time; CW RF Input	$V_{OUT}$ within 10% of Final Value; $P_{IN} = 0\text{dBm}$		1		$\mu s$
Turn OFF Time; CW RF Input	$V_{OUT} < 0.18V$ ; $P_{IN} = 0\text{dBm}$		8		$\mu s$

#### Power Supply

$0V_{DD}$ Supply Voltage		●	1	3.3	$V_{DD}$	V
$V_{DD}$ Supply Voltage		●	2.7	3.3	3.6	V
$V_{REF}$ Reference Voltage		●	1.4		$V_{DD} + 0.05$	V
$V_{CC}$ Supply Voltage	Should Be Equal to $V_{DD}$	●	2.7	3.3	3.6	V
Total Supply Current	No RF Input Signal, ADC Operational at 500ksps	●		3	4	mA
	No RF Input Signal, ADC Sleep-Mode	●		1.4	2.5	mA
Shutdown Current	$EN = 0.3V$ , $CONV = 3.3V$ , ADC Sleep-Mode			0.2	10	$\mu A$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The maximum RF input power rating is guaranteed by design and engineering characterization, but not production tested.

**Note 2:** The LTC5587 is guaranteed to be functional over the operating temperature range from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**Note 3:** The linearity error is calculated by the difference between the incremental slope of the output and the average output slope from  $-20\text{dBm}$  to  $0\text{dBm}$ . The dynamic range is defined as the range over which the linearity error is within  $\pm 1\text{dB}$ .

**Note 4:** An external capacitor at the  $C_{SQ}$  pin should be used for input frequencies below 250MHz. Without this capacitor, lower frequency operation results in excessive RF ripple in the output voltage.

**Note 5:** Logarithmic intercept is an extrapolated input power level from the best fitted log-linear straight line, where the converted output code is 0LSB.

**Note 6:** PSRR determined as the dB value of the change in converted output voltage over the change in  $V_{CC}$  supply voltage at a given CW input power level.

**Note 7:** Guaranteed by design not subject to test.

**Note 8:** Guaranteed by characterization. All input signals are specified with  $t_R = t_F = 2\text{ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of 1.6V.

**Note 9:** All timing specifications given are with a 10pF capacitance load. With a capacitance load greater than this value, a digital buffer or latch must be used.

**Note 10:** The time required for the output to cross the  $V_{IH}$  or  $V_{IL}$  voltage.

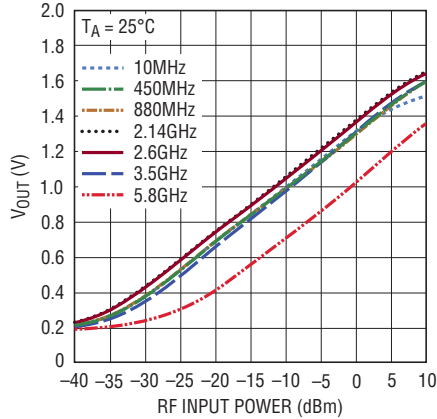
**Note 11:** When pins  $V_{OUT}$  and  $V_{REF}$  are taken below GND or above  $V_{DD}$ , they will be clamped by internal diodes. This product can handle input currents greater than 100mA below GND or above  $V_{DD}$  without latchup.

**Note 12:** The  $V_{DD}$  supply voltage can be the same as  $V_{CC}$  and the pins can share a common bypass capacitor of 2.2 $\mu\text{F}$ .

## TYPICAL PERFORMANCE CHARACTERISTICS

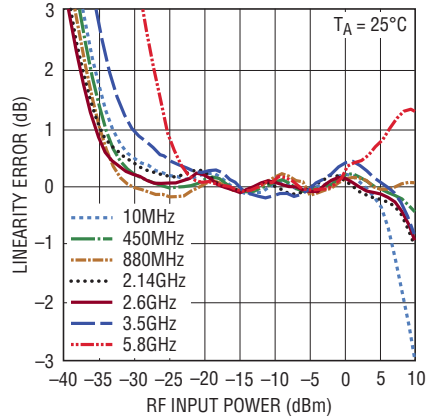
$V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  
 $f_{SAMPL} = f_{SAMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted.  $V_{OUT} = \text{ADC Output (LSB)} \cdot 1.8/4096$ . Test circuit is shown in Figure 1.

Output Voltage vs Frequency



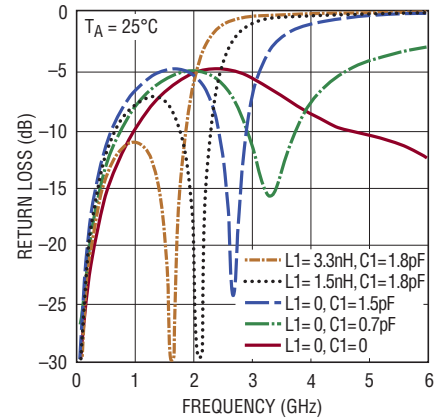
5587 G01

Linearity Error vs Frequency



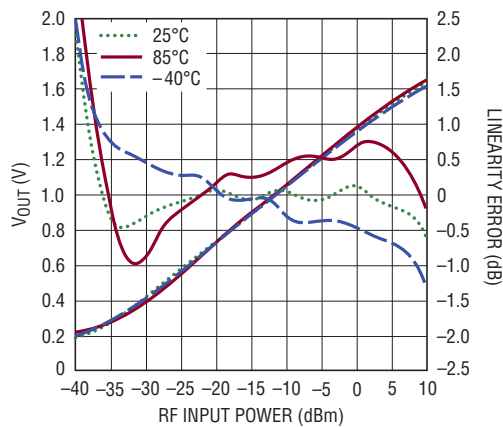
5587 G02

RF Input Return Loss vs Frequency



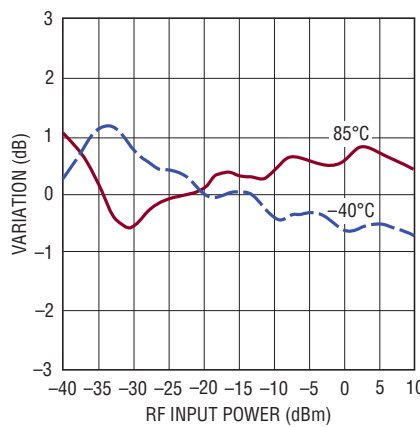
5587 G03

Output Voltage and Linearity Error at 450MHz



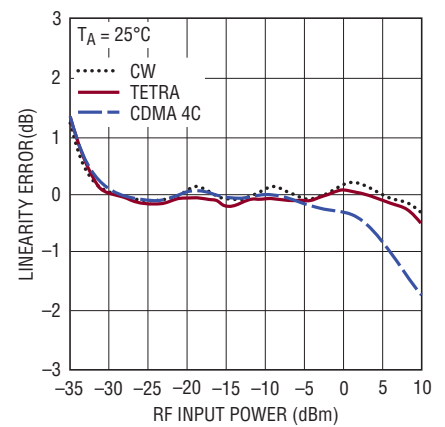
5587 G04

Output Voltage Temperature Variation from 25°C at 450MHz



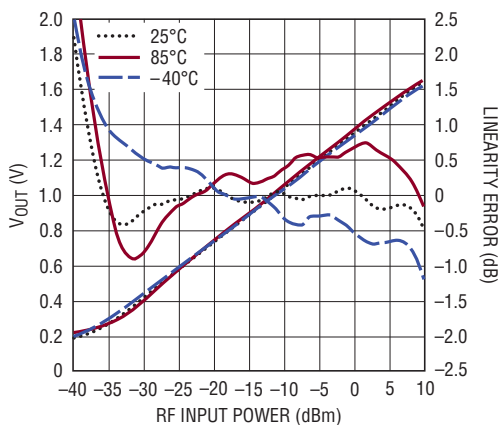
5587 G05

Linearity Error vs RF Input Power 450MHz Modulated Waveforms



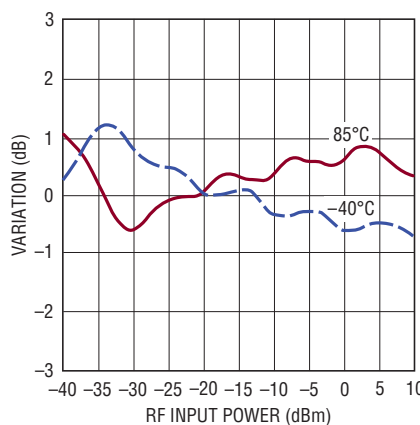
5587 G06

Output Voltage and Linearity Error at 880MHz



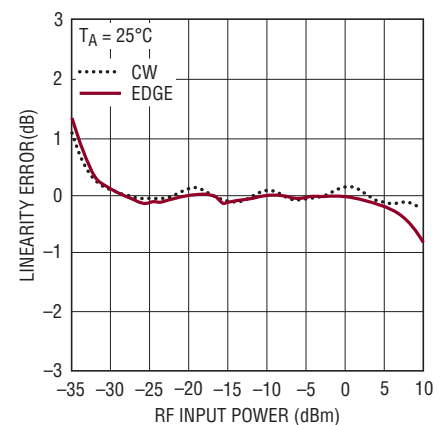
5587 G07

Output Voltage Temperature Variation from 25°C at 880MHz



5587 G08

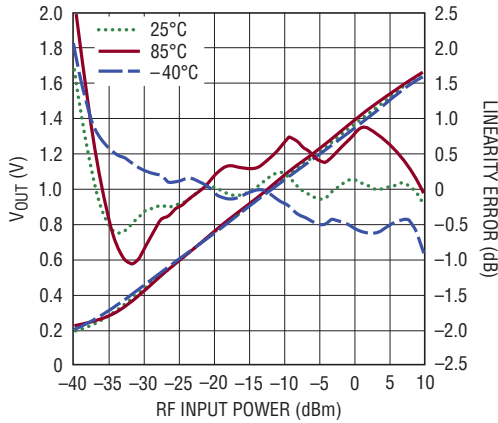
Linearity Error vs RF Input Power 880MHz Modulated Waveforms



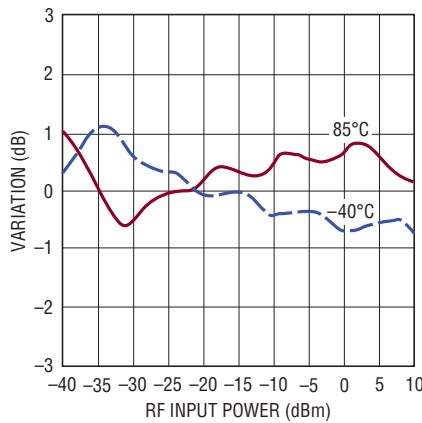
5587 G09

**TYPICAL PERFORMANCE CHARACTERISTICS**

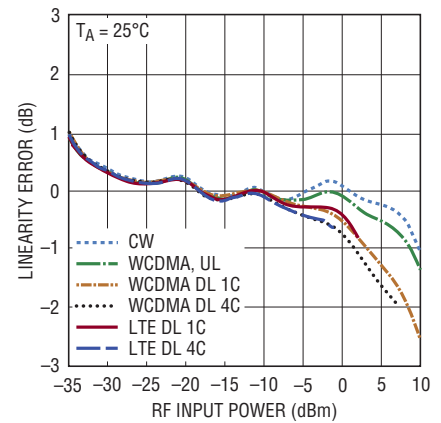
$V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  
 $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted.  $V_{OUT} = \text{ADC Output (LSB)} \cdot 1.8/4096$ . Test circuit is shown in Figure 1.

**Output Voltage and Linearity Error at 2140MHz**

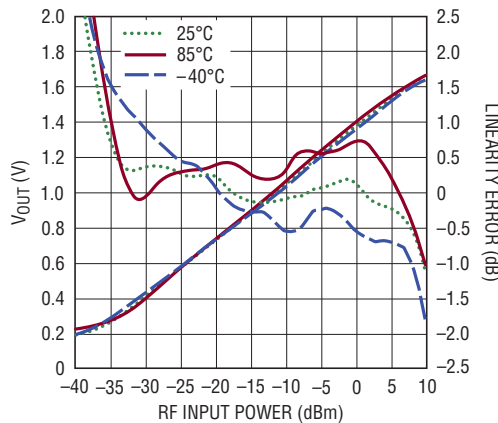
5587 G10

**Output Voltage Temperature Variation from 25°C at 2140MHz**

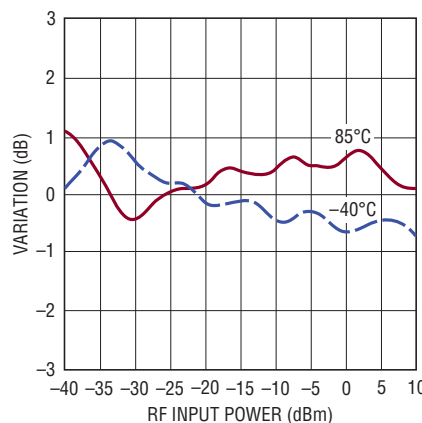
5587 G11

**Linearity Error vs RF Input Power 2140MHz Modulated Waveforms**

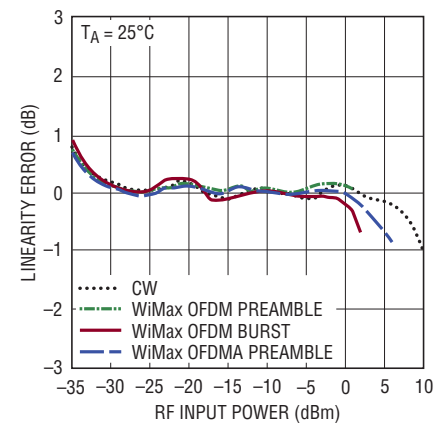
5587 G12

**Output Voltage and Linearity Error at 2600MHz**

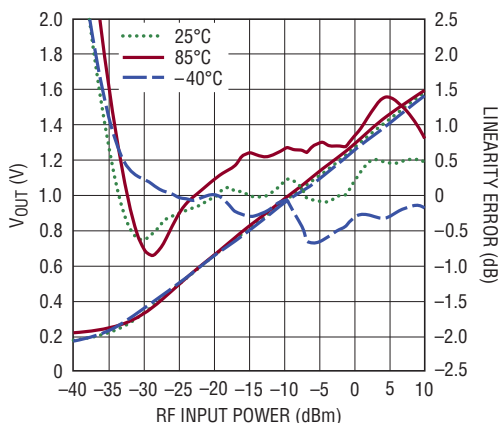
5587 G13

**Output Voltage Temperature Variation from 25°C at 2600 MHz**

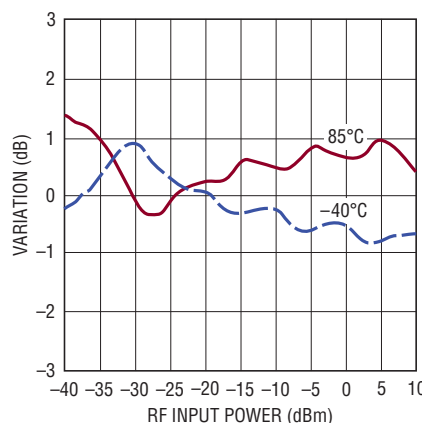
5587 G14

**Linearity Error vs RF Input Power 2.6GHz Modulated Waveforms**

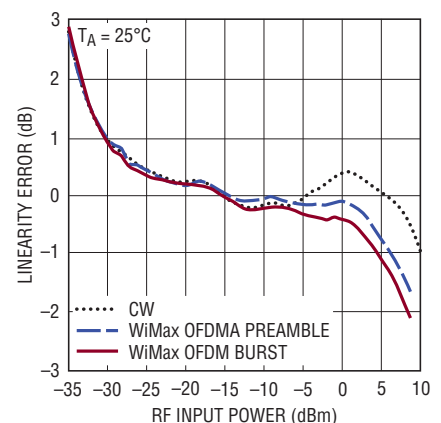
5587 G15

**Output Voltage and Linearity Error at 3500MHz**

5587 G16

**Output Voltage Temperature Variation from 25°C at 3500MHz**

5587 G17

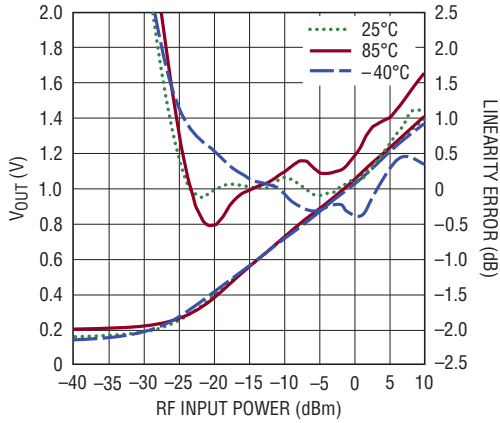
**Linearity Error vs RF Input Power 3.5GHz Modulated Waveforms**

5587 G18

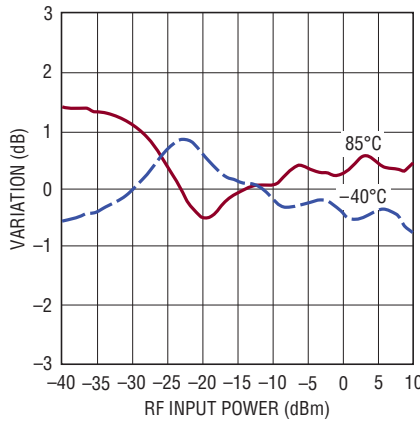
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SMPL} = f_{SMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted.  $V_{OUT} = \text{ADC Output (LSB)} \cdot 1.8/4096$ . Test circuit is shown in Figure 1.

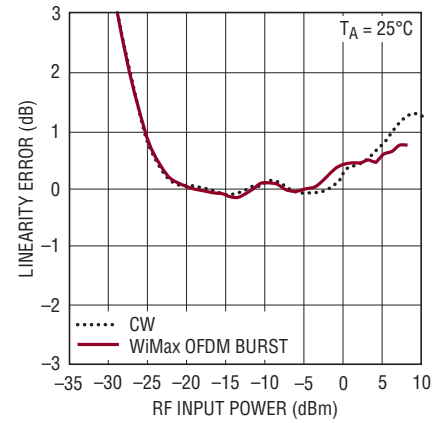
**Output Voltage and Linearity Error at 5800MHz**



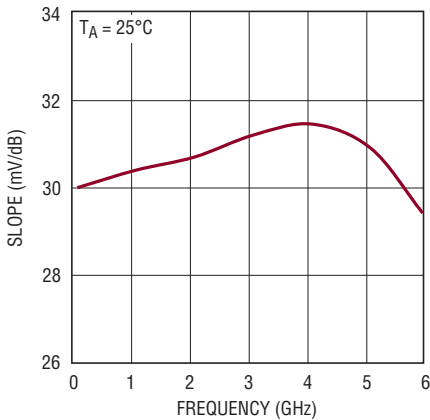
**Output Voltage Temperature Variation from 25°C at 5800MHz**



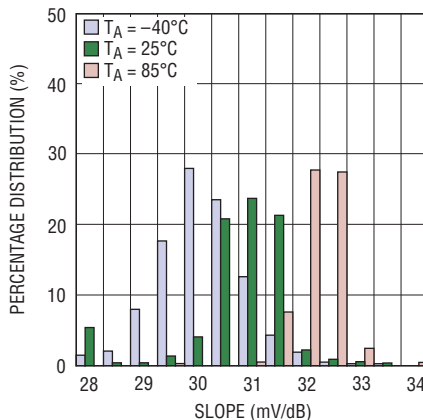
**Linearity Error vs RF Input Power 5.8GHz Modulated Waveforms**



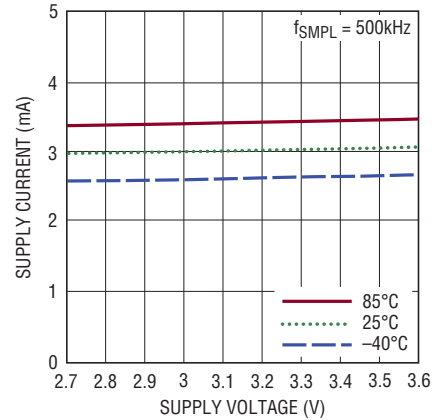
**Slope vs Frequency**



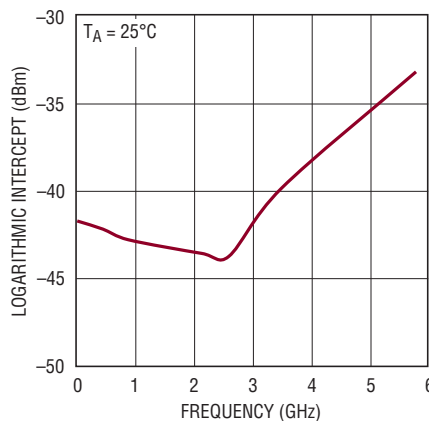
**Slope Distribution vs Temperature**



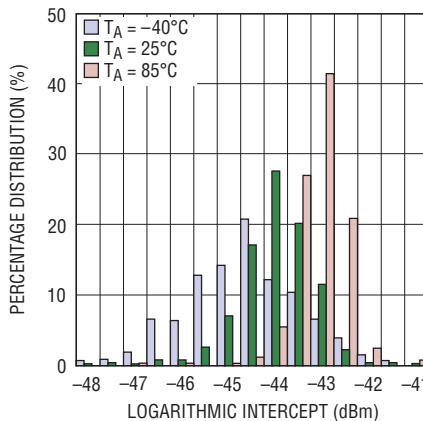
**Supply Current vs Supply Voltage**



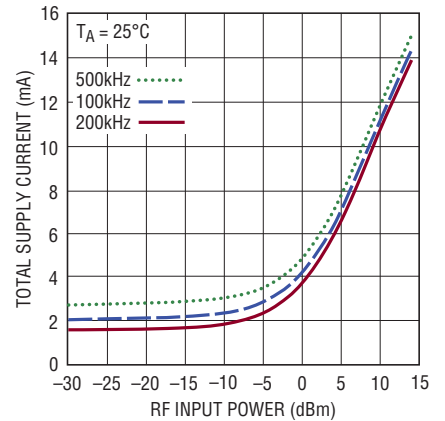
**Logarithmic Intercept vs Frequency**



**Logarithmic Intercept Distribution vs Temperature**



**Total Supply Current vs RF Input Power and Sample Rate**

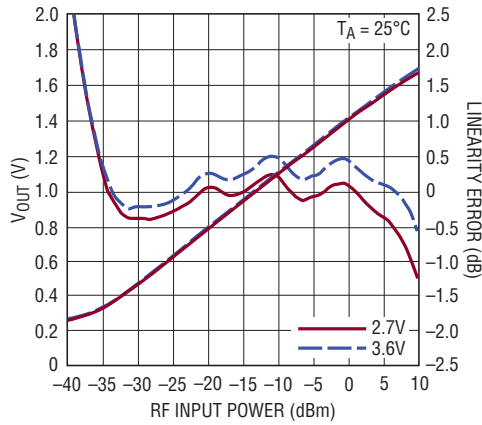




# TYPICAL PERFORMANCE CHARACTERISTICS

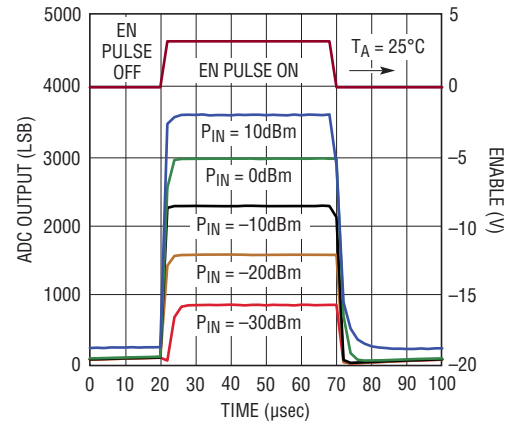
$V_{CC} = V_{DD} = 0V_{DD} = 3.3V$ ,  $V_{REF} = 1.8V$ ,  $EN = 3.3V$ ,  $f_{SAMPL} = f_{SAMPL(MAX)}$  and  $f_{SCK} = f_{SCK(MAX)}$  unless otherwise noted.  $V_{OUT} = \text{ADC Output (LSB)} \cdot 1.8/4096$ . Test circuit is shown in Figure 1.

**Output Voltage and Linearity Error vs  $V_{CC}$  at 2140MHz**



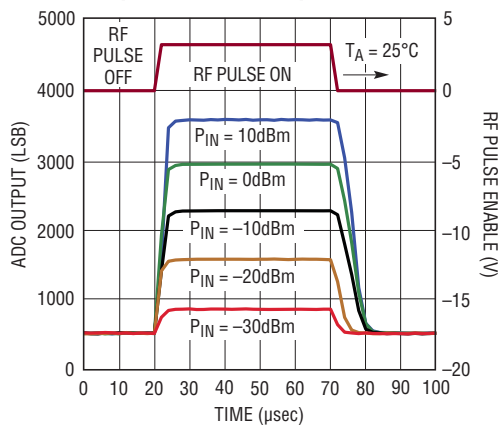
5587 G29

**Output Transient Response with CW RF and EN Pulse**



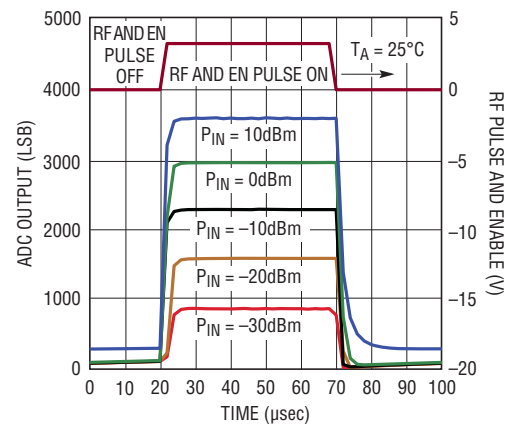
5587 G33

**Output Transient Response**



5587 G32

**Output Transient Response with RF Pulse and EN Pulse**



5587 G31



## PIN FUNCTIONS

**SDO (Pin 1):** Three-State Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with MSB first. The data stream consists of 12 bits of conversion data followed by trailing zeros.

**SCK (Pin 2):** Shift Clock Input. The SCK serial clock synchronizes the serial data transfer. SDO data transitions on the falling edge of SCK.

**OV<sub>DD</sub> (Pin 3):** ADC Output Driver Supply Voltage, 1.0V to 3.6V. OV<sub>DD</sub> should be bypassed with a 1μF ceramic capacitor. OV<sub>DD</sub> can be driven separately from V<sub>DD</sub> and OV<sub>DD</sub> can be higher than V<sub>DD</sub>.

**V<sub>OUT</sub> (Pin 4):** Detector Analog Voltage Output. An internal series 300Ω resistor at the detector output allows for simple R-C filtering with a capacitor placed on this pin to GND. A 1000pF capacitor is recommended for a corner frequency of 500kHz.

**CSQ (Pin 6):** Optional low-frequency range extension capacitor for frequencies below 250MHz. Connect 0.01μF from this pin to ground for 10MHz operation.

**RF (Pin 7):** RF Input Voltage. Should be externally DC-blocked. A capacitor of 1000pF is recommended. This pin has an internal 205 $\Omega$  termination.

**V<sub>CC</sub> (Pin 8):** Detector Power Supply Voltage, 2.7V to 3.6V. Can be connected to the V<sub>DD</sub> voltage supply. V<sub>CC</sub> should be bypassed with a 1μF ceramic capacitor. If V<sub>CC</sub> and V<sub>DD</sub> are tied together, then bypass with 2.2μF.

**EN (Pin 9):** Detector Enable. A logic low or no-connect on the enable pin shuts down the detector. A logic high enables the detector. An internal 500k pull-down resistor ensures the detector is off when the pin is left floating.

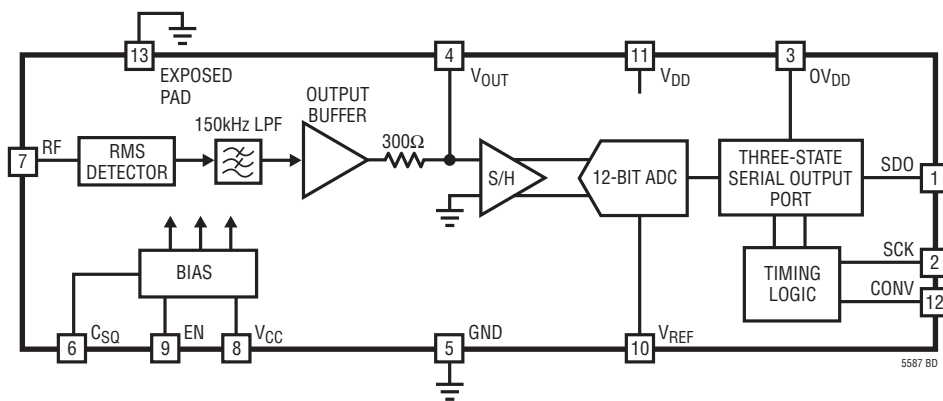
**V<sub>REF</sub> (Pin 10):** ADC Reference Input Voltage. V<sub>REF</sub> defines the input span of the ADC, 0V to V<sub>REF</sub>. The V<sub>REF</sub> range is 1.4V to V<sub>DD</sub>. Bypass to ground with a 1μF ceramic capacitor.

**V<sub>DD</sub> (Pin 11):** ADC Power Supply Voltage, 2.7V to 3.6V. V<sub>DD</sub> should be bypassed with a 1μF ceramic capacitor.

**CONV (Pin 12):** Convert Input. This active high signal starts a conversion on the rising edge. The ADC automatically powers down after conversion. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

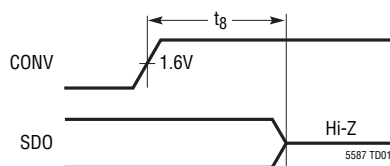
**GND (Pin 5, Exposed Pad Pin 13):** Ground. For high-frequency operation, backside ground connection should have a low-inductance connection to the pcb ground using many through-hole vias. See layout information.

## BLOCK DIAGRAM

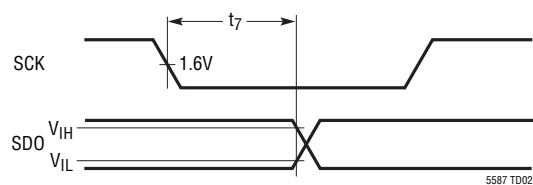


## TIMING DIAGRAMS

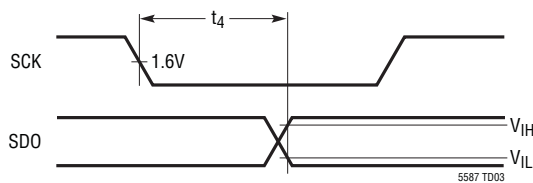
SDO Into Hi-Z State After CONV Rising Edge



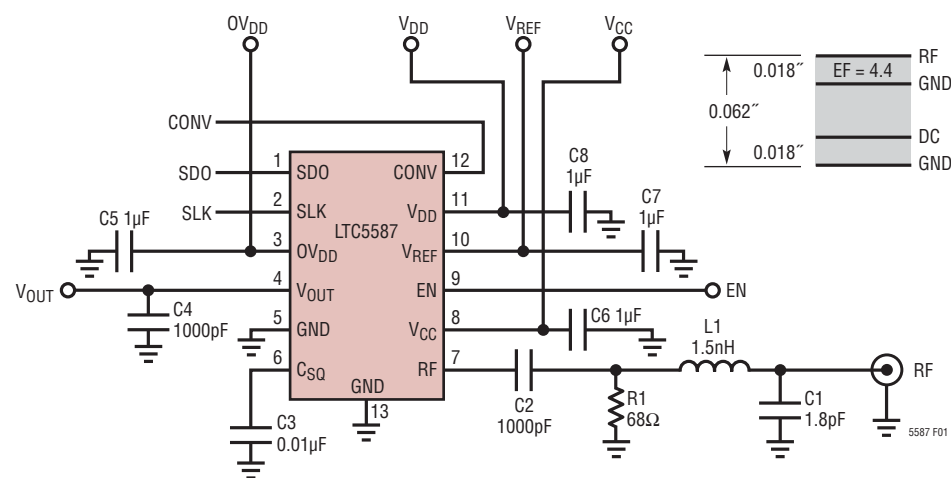
SDO Data Valid Hold Time After SCK Falling Edge



SDO Data Valid Access Time After SCK Falling Edge



TEST CIRCUIT



REF DES	VALUE	SIZE	PART NUMBER
C5, C6, C7, C8	1µF	0402	AVX 0402ZG105ZAT2A
C3	0.01µF	0402	AVX 04023C103KAT2A
C2, C4	1000pF	0402	AVX 04025C102KAT2A
R1	68Ω	0402	CRCW040268R1FKED

FREQUENCY RANGE	RF <sub>IN</sub> MATCH	
	L1	C1
0.04 to 1.8GHz	3.3nH	1.8pF
1.75 to 2.2GHz	1.5nH	1.8pF
2.4 to 2.9GHz	0	1.5pF
2.8 to 3.8GHz	0	0.7pF
4.5 to 6.0GHz	0	0

Figure 1. Evaluation Circuit Schematic

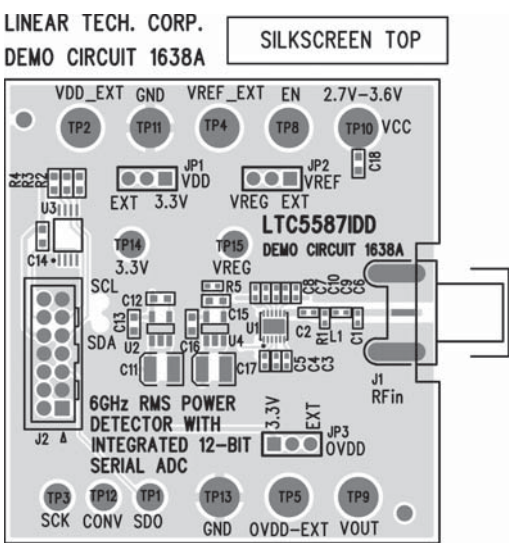


Figure 2. Evaluation Circuit Board

## APPLICATIONS INFORMATION

### Operation

The LTC5587 combines a proprietary high-speed power detector with an internal 150kHz lowpass averaging filter and a true 12-bit successive approximation ADC with a serial output interface. It can accurately measure the RMS power of high crest-factor modulated RF signals. The output voltage of the RF power detector is converted to a 12-bit digital word that is directly proportional to the average RF input power in dBm. The part can be operated from a single supply or dedicated supplies, allowing the user to select a specific voltage range for the ADC conversion in addition to interfacing with 1.8V, 2.5V, or 3V digital systems.

### Evaluation

Figure 1 shows the simplified evaluation circuit schematic, and Figure 2 shows the associated board artwork. To ensure proper operation, good grounding practice should be followed in the board layout, with liberal placement of vias under the exposed pad of the package and around signal and digital lines. The evaluation board shown in Figure 2 contains additional support circuitry not shown in Figure 1 that includes an optional 3.3V regulator for the  $V_{DD}$ ,  $OV_{DD}$ , and  $V_{CC}$  supplies and an optional 1.8V regulator for the  $V_{REF}$  reference. This onboard reference provides good accuracy (less than  $\pm 5\text{mV}$ ) over temperature, contributing less than  $\pm 0.1\text{dB}$  error to the ADC output. To evaluate the digital output, the QuickEval PC-based software can be used with the DC590B USB controller interface board. This board contains a generic USB to serial peripheral interface (SPI) controller. A 14-pin ribbon cable connects the evaluation board to the DC590B board. The DC590B allows the evaluation at approximately a 200Hz sample rate ( $f_{SMPL}$ ). (See <http://cds.linear.com/docs/Reference%20Design/dc590B.pdf>). For higher sample rates the digital I/O pins can be accessed directly on the board. Contact LTC Applications for more information on higher sample rate evaluation.

### RF Input Matching

The input resistance is about  $205\Omega$ . Input capacitance is 1.6pF. The impedance vs frequency of the RF input is detailed in the following table.

Table 1. RF Input Impedance

FREQUENCY (MHz)	INPUT IMPEDANCE ( $\Omega$ )	S11	
		MAG	ANGLE ( $^\circ$ )
10	203.3-j1.4	0.605	-0.7
50	201.8-j7.0	0.605	-3.7
100	197.2-j13.7	0.606	-7.3
200	161.9-j25.8	0.608	-14.6
400	142.5-j43.6	0.614	-28.9
500	125.3-j48.5	0.619	-35.8
800	88.0-j60.4	0.636	-55.6
900	79.2-j62.6	0.643	-61.8
1000	71.8-j64.3	0.650	-67.7
1500	46.6-j68.8	0.685	-94.3
2000	31.1-j69.2	0.715	-116
2100	29.9-j69.0	0.721	-119.9
2500	22.4-j66.8	0.739	-134.1
3000	15.3-j60.7	0.756	-149.6
3500	9.9-j47.3	0.768	-163.2
4000	6.6-j16.9	0.779	-175.5
5000	9.8-j51.7	0.787	162.1
6000	18.5-j69.4	0.792	141.4

A shunt  $68\Omega$  resistor can be used to provide a broadband match at low frequencies up to 1GHz and from 4.5GHz to 6GHz. As shown in Figure 3, a nominal broadband input match can be achieved up to 1.8GHz by using an LC matching circuit consisting of a series 3.3nH inductor (L1) and a shunt 1.8pF capacitor (C1). This match will maintain a return loss of about 10dB across the band. For matching at higher frequencies, L1 and C1 values are listed in the table of Figure 1. The input reflection coefficient referenced to the RF input pin with no external components is shown on the smith chart in Figure 4. Alternatively, it is possible to match using an impedance transformation network by omitting R1 and transforming the  $205\Omega$  input to  $50\Omega$ . This narrow band matching will improve sensitivity up to about 6dB max, and the dynamic range remains the same. For example: by omitting R1 and setting  $L1 = 1.8\text{nH}$  and  $C1 = 3\text{pF}$ , a 2:1 VSWR match can be obtained from 1.95GHz to 2.36GHz with a sensitivity improvement of 5dB.

## APPLICATIONS INFORMATION

The RF input DC-blocking capacitor (C2) and  $C_{SQ}$  bias decoupling capacitor (C3), can be adjusted for low-frequency operation. For input frequencies down to 10MHz, 0.01 $\mu$ F is needed at  $C_{SQ}$ . For frequencies above 250MHz, the on-chip 20pF decoupling capacitor is sufficient and  $C_{SQ}$  may be eliminated as desired. The DC-blocking capacitor can be as large as 2200pF for 10MHz operation or 100pF for 2GHz operation. A DC-blocking capacitor larger than 2200pF results in an undesirable RF pulse response on the falling edge due to the rectifier action of the diode limiter/ESD protection at the RF pin. Therefore, the recommended value for C2 for general applications is conservatively set at 1000pF.

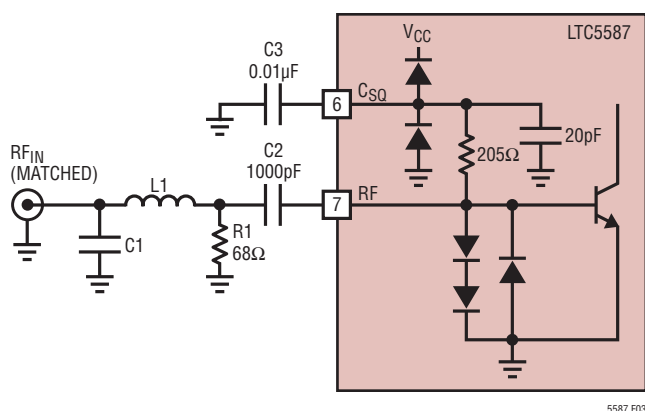


Figure 3. Simplified Schematic of the RF Input Interface

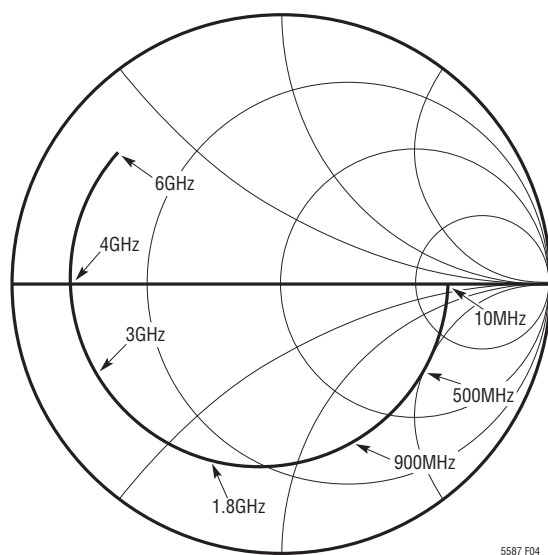


Figure 4. Input Reflection Coefficient

### Filter Capacitor

The interface of the  $V_{OUT}$  pin of the LTC5587 is shown in Figure 5. It includes a push-pull output stage with a series 300 $\Omega$  resistor. The detector output stage is capable of sourcing and sinking 5mA of current. The  $V_{OUT}$  pin can be shorted to GND or  $V_{CC}$  (or  $V_{DD}$  whichever is lower) without damage, but going beyond the  $V_{CC} + 0.5V$  or  $V_{DD} + 0.5V$  and alternatively going beyond  $GND - 0.5V$  may result in damage as the internal ESD protection diodes will start to conduct excessive current.

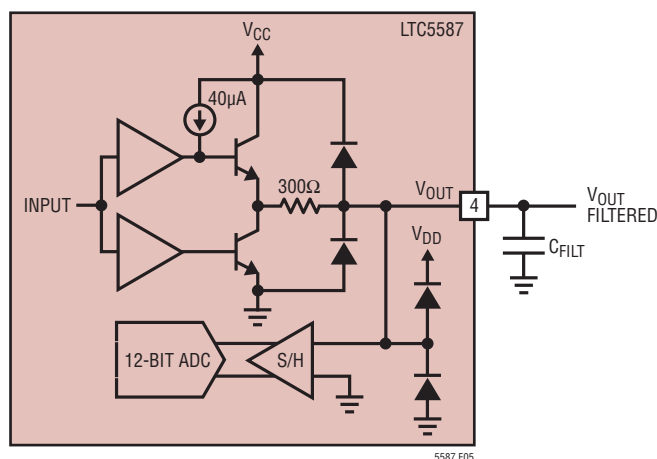


Figure 5. Simplified Schematic of the Detector Analog Output

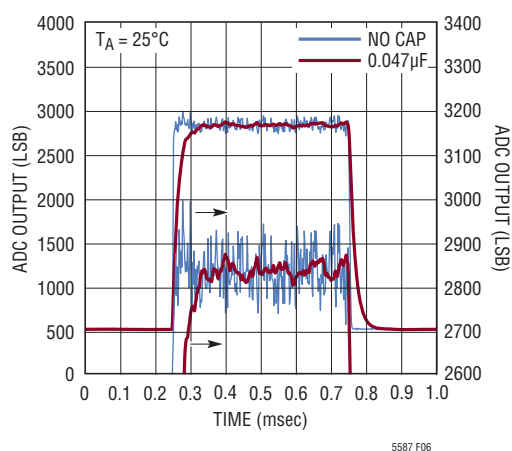
The residual ripple due to RF modulation can be reduced by adding an external capacitor,  $C_{FILT}$  (C4 on evaluation circuit schematic) to the  $V_{OUT}$  pin to form a simple RC lowpass filter. The internal 300 $\Omega$  resistor in series with the output pin enables filtering of the output signal with just the addition of  $C_{FILT}$ . The filter -3dB corner frequency,  $f_c$ , can be calculated with the following equation:

$$f_{c(-3dB)} = 1/(2 \cdot \pi \cdot 300 \cdot C_{FILT})$$

with  $f_c$  in Hz and  $C_{FILT}$  in F. Since the bandwidth of the detected signal is effectively limited by the internal 150kHz filter, a choice of  $C_{FILT} = 1000pF$  sets the ADC -3dB input bandwidth at 530kHz and does not affect the residual modulation ripple much.  $C_{FILT}$  has a small effect on ADC sampling accuracy. For example, when the sample rate of the ADC is changed from 25ksps to 500ksps, the output value changes less than 0.2dB with any choice of  $C_{FILT}$ .

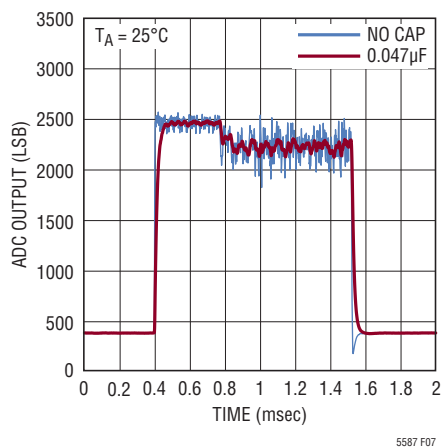
## APPLICATIONS INFORMATION

Figure 6 shows the effect of the external filter capacitor on the residual ripple level for a 4-carrier WCDMA downlink signal at 2.14GHz with  $-10\text{dBm}$ . Adding a  $0.047\mu\text{F}$  capacitor to the output decreases the peak-to-peak output ripple from 150LSB to about 60LSB.



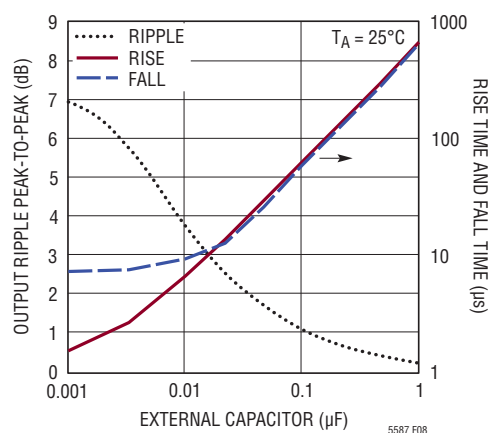
**Figure 6. Residual Ripple, Output Transient Response for RF Pulse with WCDMA 4-Carrier Modulation**

Figure 7 shows the transient response for a 2.6GHz WiMax signal with preamble and burst ripple reduced by a factor of three using a  $0.047\mu\text{F}$  external filter capacitor. The average power in the preamble section is  $-10\text{dBm}$ , while the burst section has 3dB lower average power. With the capacitor, the ripple in the preamble section is about 0.5dB peak to peak. The modulation used was OFDM (WiMax 802.16-2004) MMDS band 1.5MHz BW, with 256 size FFT and 1 burst at QPSK  $3/4$ .



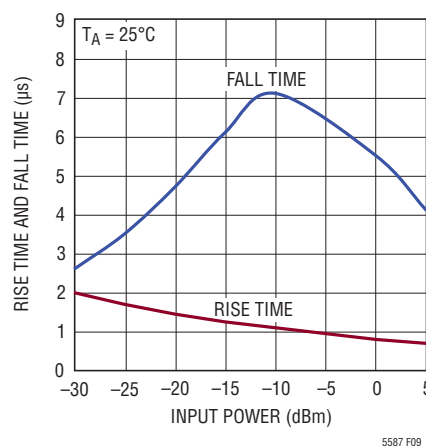
**Figure 7. Residual Ripple for 2.6GHz WiMax OFDM 802.16-2004**

Figure 8 shows how the peak-to-peak ripple decreases with increasing external filter capacitance value. Also shown is how the RF pulse response will have longer rise and fall times with the addition of this lowpass filter cap.



**Figure 8. Residual Ripple, Output Transient Times for RF Pulse with WCDMA 4-Carrier Modulation vs External Filter Capacitor C4**

Figure 9 shows the rise time and fall time is a strong function of the RF input power when the filter capacitor is not present.



**Figure 9. RF Pulse Response Rise Time and Fall Time vs RF Input Power**

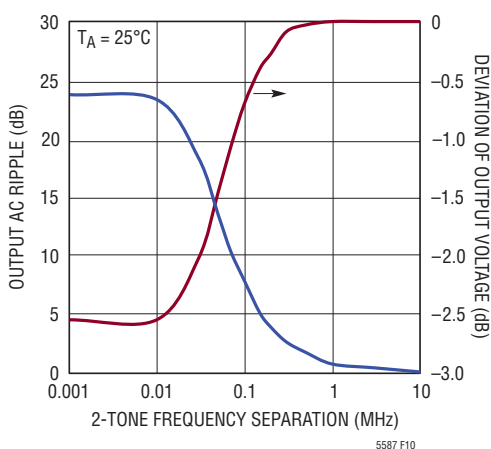
## APPLICATIONS INFORMATION

For a given RF modulation type, WCDMA for example, the internal 150kHz filter provides nominal filtering of the residual ripple level. Additional external filtering happens in the log-domain, which introduces a systematic log-error in relation to the signal's crest factor as shown in the following equation in dB<sup>1</sup>:

$$\text{Error}_{\text{dB}} = 10 \cdot \log_{10}(r + (1-r)10^{-\text{CF}/10}) - \text{CF} \cdot (r-1)$$

Where CF is the crest factor and  $r$  is the duty cycle of the measurement (or number of measurements made at the peak envelope divided by the total number of periodic measurements in the measurement period). It is important to note that the CF refers to the 150kHz low-pass filtered envelope of the signal. The error will depend on the statistics and bandwidth of the modulation signal in relation to the internal 150kHz filter. For example: simulations have shown for the case of WCDMA that it is possible to set the external filter capacitor corner frequency at 15kHz and only introduce an error less than 0.1dB.

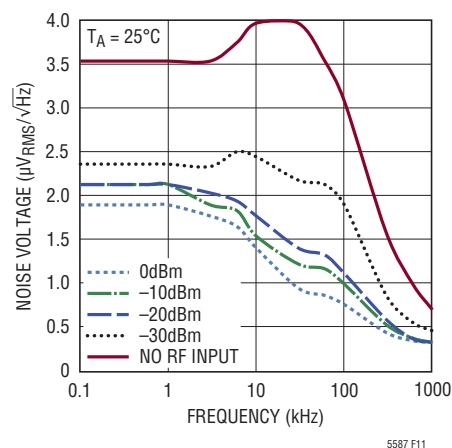
Figure 10 shows the output AC modulation ripple as a function of modulation difference frequency for a 2-tone input signal at 2140MHz with -10dBm input power. The resulting deviation in the output voltage of the detector shows the effect of the internal 150kHz filter.



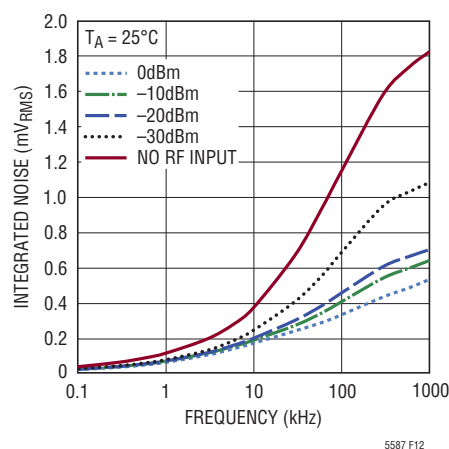
**Figure 10. Output DC Voltage Deviation and Residual Ripple vs 2-Tone Separation Frequency**

1. Steve Murray, "Beware of Spectrum Analyzer Power Averaging Techniques," *Microwaves & RF*, Dec. 2006.

The output voltage noise density and integrated noise are shown respectively in Figures 11 and 12 for various input power levels. The noise is a strong function of input level and there is roughly a 10dB improvement in the output noise level for an input level of 0dBm versus no input.



**Figure 11. Output Voltage Noise Density**



**Figure 12. Integrated Output Voltage Noise**



## APPLICATIONS INFORMATION

The total noise at the ADC output is dominated by the output noise of the detector, and the sampling noise is insignificant. The peak-to-peak output noise is also almost independent of the sample rate. Figure 13 shows the peak-to-peak noise at the ADC output as a function of the RF input level for a CW RF input. Increasing  $C_{\text{FILT}}$  from 1000pF to 0.01 $\mu$ F gives roughly 2x to 3x lower noise over input power.

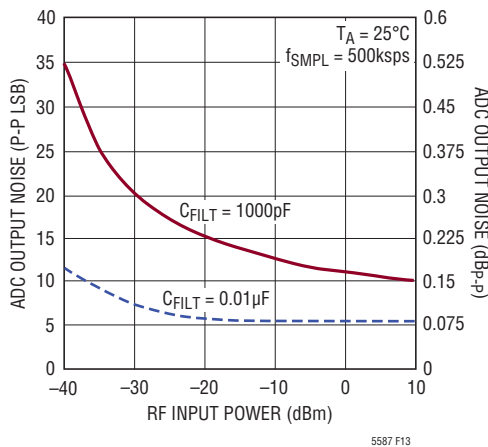


Figure 13. Peak-to-Peak Noise at ADC Output vs RF Input Power

### Serial Interface

The LTC5587 communicates with microcontrollers, DSPs and other external circuitry via a 3-wire interface. Figure 14 shows the operating sequence of the serial interface.

### Data Transfer

A rising CONV edge starts a conversion and disables SDO. After the conversion, the ADC automatically goes into sleep mode, drawing only leakage current. CONV going low enables SDO and clocks out the MSB bit, B11. SCK then synchronizes the data transfer with each bit being transmitted on the falling SCK edge and can be captured on the rising SCK edge. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely (see Figure 14). For example, 16-clocks at SCK will produce the 12-bit data and four trailing zeros on SDO.

### Sleep Mode

The LTC5587 ADC enters sleep mode to save power after each conversion if CONV remains high. In sleep mode, all bias currents are shut down and only leakage currents remain (about 0.1 $\mu$ A). The sample-and-hold is in hold mode while the ADC is in sleep mode. The ADC returns to sample mode after the falling edge of CONV during power-up.

### Exiting Sleep Mode and Power-Up Time

By taking CONV low, the ADC powers up and acquires an input signal completely after the acquisition time ( $t_{\text{ACQ}}$ ). After  $t_{\text{ACQ}}$ , the ADC is ready to perform a conversion again by a rising edge on CONV.

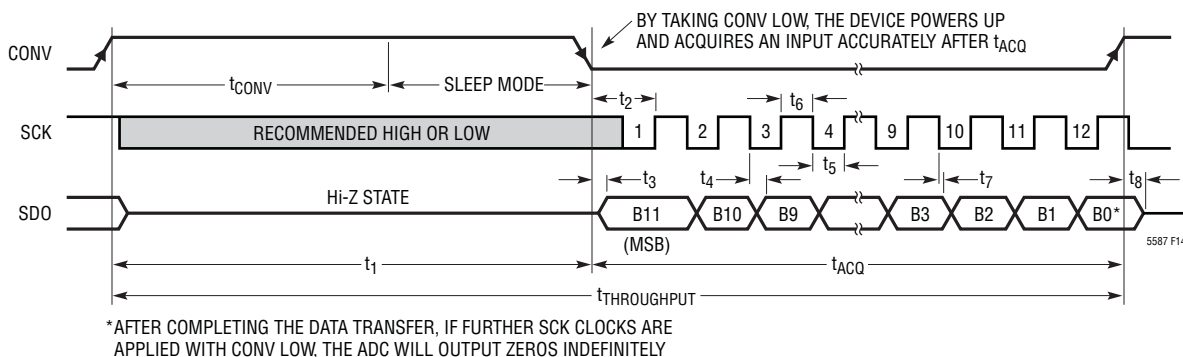
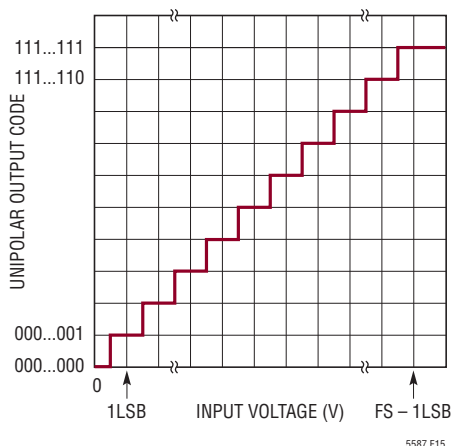
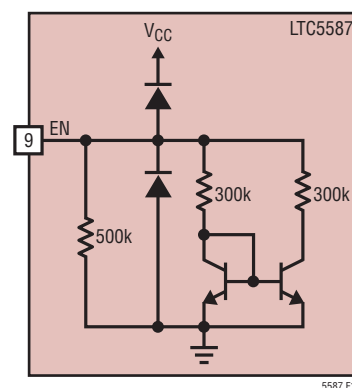


Figure 14. LTC5587 Serial Interface Timing Diagram

The  $V_{REF}$  pin defines the full-scale range of the ADC. The reference voltage can range from  $V_{DD}$  down to 1.4V. If the difference between the input voltage on the  $V_{OUT}$  pin and GND exceeds  $V_{REF}$ , the output code will stay fixed at all ones, and if this difference goes below 0V, the output code will stay fixed at all zeros. Figure 15 shows the ideal input/output characteristics for the ADC. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ...,  $FS - 1.5LSB$ ). The output code is straight binary with  $1LSB = V_{REF}/4096$ . Using the onboard 1.8V reference on the evaluation board, the conversion range can be easily calculated between LSB and dBm. For an analog output slope of 32mV/dB, we can calculate the total 40dB range is equivalent to 2912.7LSB's at the ADC output:

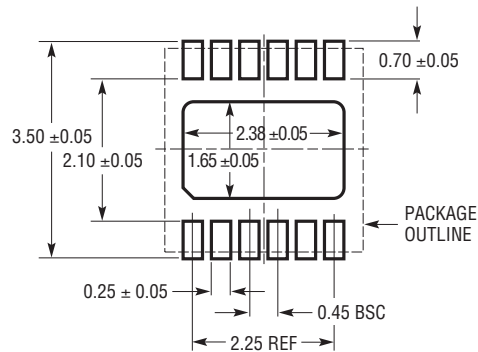


It is important that the voltage applied to the EN pin should never exceed  $V_{CC}$  by more than 0.5V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the EN pin.

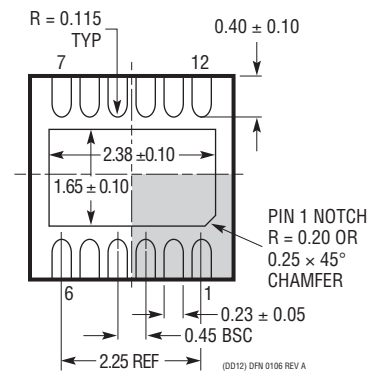
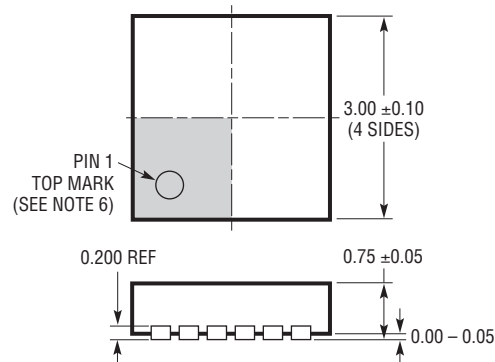


## PACKAGE DESCRIPTION

### DD Package 12-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1725 Rev A)



**RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS**  
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

#### NOTE:

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

