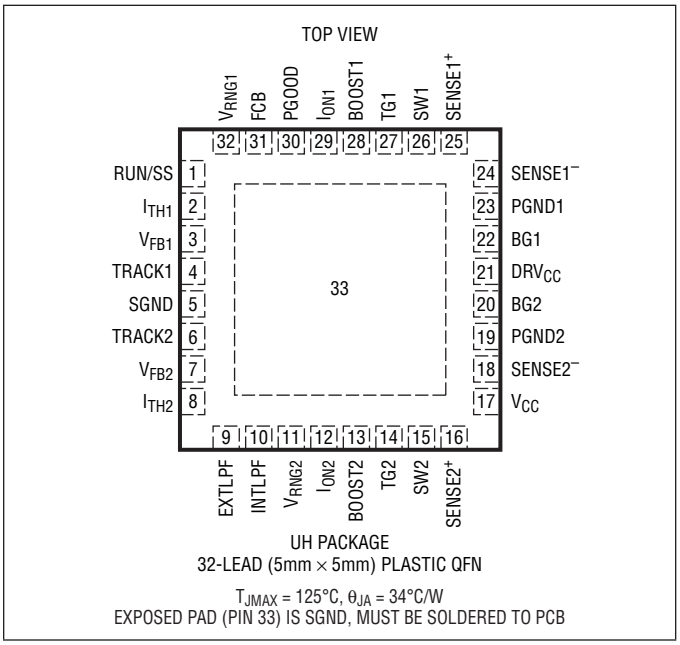
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{CC}, DRV_{CC})..... 7V to –0.3V
Boosted Topside Driver Supply Voltage
BOOST1, 2 ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... 36V to –5V
$SENSE1^+$, $SENSE2^+$ Voltages..... 36V to –5V
$SENSE1^–$, $SENSE2^–$ Voltages ..... 10V to –0.3V
I_{ON1}, I_{ON2} Voltages..... 21V to –0.3V
(BOOST – SW) Voltages ..... 7V to –0.3V
RUN/SS, PGOOD Voltages ..... 7V to –0.3V
PGOOD DC Current 5mA
TRACK1, TRACK2 Voltages.....V_{CC} + 0.3V to –0.3V
V_{RNG1}, V_{RNG2} Voltages..... V_{CC} + 0.3V to –0.3V
I_{TH1}, I_{TH2} Voltages ..... 2.7V to –0.3V
V_{FB1}, V_{FB2} Voltages..... 2.7V to –0.3V
INTLPF, EXTLPF Voltages ..... 2.7V to –0.3V
FCB Voltages..... 7V to –0.3V
Operating Temperature Range (Note 5) ...–40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range .....–65°C to 125°C
Reflow Peak Body Temperature ..... 260°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3708#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3708EUH#PBF	LTC3708EUH#TRPBF	3708	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3708EUH	LTC3708EUH#TR	3708	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/ . Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, DRV_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Shutdown				 2.4 250	 3 400	 mA µA
$I_{FB1,2}$	Feedback Pin Input Current	I_{TH} = 1.2V (Notes 3, 4)			–50	–100	nA
V_{REF}	Internal Reference Voltage	I_{TH} = 1.2V, 0°C to 85°C (Notes 3, 4) I_{TH} = 1.2V (Notes 3, 4)	 ●	0.594 0.591	0.600 0.600	0.606 0.609	V V
$V_{FB1,2}$	Feedback Voltage	I_{TH} = 1.2V (Note 3)		0.594	0.600	0.606	V
$\Delta V_{FB(LINEREG)1,2}$	Feedback Voltage Line Regulation	V_{CC} = 4.5V to 6.5V (Note 3)			0.02		%/V
$\Delta V_{FB(LOADREG)1,2}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 1.9V (Note 3)			–0.05	–0.2	%
$g_{m(EA)1,2}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 3)	●	1.2	1.45	1.7	mS
$t_{ON1,2}$	On-Time	I_{ON} = 60µA, V_{FCB} = 0V I_{ON} = 30µA, V_{FCB} = 0V		94 186	116 233	138 280	ns ns
$t_{ON(MIN)1,2}$	Minimum On-Time	I_{ON} = 180µA			50	85	ns
$t_{OFF(MIN)1,2}$	Minimum Off-Time	I_{ON} = 30µA			270	350	ns
$V_{SENSE(MAX)1,2}$	Maximum Current Sense Threshold	V_{RNG} = 1V, V_{FB} = 0.565V V_{RNG} = 0V, V_{FB} = 0.565V V_{RNG} = VCC, V_{FB} = 0.565V		125 90 180	143 100 200	160 110 220	mV mV mV
$V_{SENSE(MIN)1,2}$	Minimum Current Sense Threshold	V_{RNG} = 1V, V_{FB} = 0.635V V_{RNG} = 0V, V_{FB} = 0.635V V_{RNG} = V_{CC}, V_{FB} = 0.635V			–62 –42 –88		mV mV mV
$\Delta V_{FB(OV)1,2}$	Overvoltage Fault Threshold			8.5	10	11.5	%
$\Delta V_{FB(UV)1,2}$	Undervoltage Fault Threshold			–380	–420	–460	mV
$V_{RUN/SS(ON)}$	RUN Pin Start Threshold		●	0.8	1.3	1.8	V
$V_{RUN/SS(LE)}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising		2.6	3	3.3	V
$V_{RUN/SS(LT)}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling		2.2	2.5	2.8	V
$I_{RUN/SS(C)}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 0V		–0.5	–1.2	–2	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current	$V_{RUN/SS}$ = $V_{RUN/SS(LE)}$, V_{FB1} or V_{FB2} = 0V		0.8	2	3	µA
$V_{CC(UVLO)}$	Undervoltage Lockout	V_{CC} Falling			3.2	3.6	V
$V_{CC(UVLOR)}$	Undervoltage Lockout Release	V_{CC} Rising			3.5	3.8	V
TG $R_{UP1,2}$	TG Driver Pull-Up On-Resistance	TG High (Note 6)			2		Ω
TG $R_{DOWN1,2}$	TG Driver Pull-Down On-Resistance	TG Low (Note 6)			2		Ω
BG $R_{UP1,2}$	BG Driver Pull-Up On-Resistance	BG High (Note 6)			3		Ω
BG $R_{DOWN1,2}$	BG Driver Pull-Down On-Resistance	BG Low (Note 6)			1		Ω
Tracking							
$I_{TRACK1,2}$	TRACK Pin Input Current	I_{TH} = 1.2V, V_{TRACK} = 0.2V (Note 3)			–100	–150	nA
$V_{FB(TRACK1,2)}$	Feedback Voltage at Tracking	V_{TRACK} = 0V, I_{TH} = 1.2V (Note 3) V_{TRACK} = 0.2V, I_{TH} = 1.2V (Note 3) V_{TRACK} = 0.4V, I_{TH} = 1.2V (Note 3)		–10 190 390	0 200 400	–10 210 410	mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, DRV_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Output							
$\Delta V_{FBH1,2}$	PGOOD Upper Threshold	Either V_{FB} Rising		8.5	10	11.5	%
$\Delta V_{FBL1,2}$	PGOOD Lower Threshold	Either V_{FB} Falling		–8.5	–10	–11.5	%
$\Delta V_{FB(HYS)1,2}$	PGOOD Hysteresis	V_{FB} Returning			3	5	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.1	0.4	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 7V				±1	µA
PG Delay	PGOOD Delay	V_{FB} Falling		100			µs
Phase-Locked Loops							
$V_{FCB(DC)}$	Forced Continuous Threshold	Measured with a DC Voltage at FCB Pin		1.9	2.1	2.3	V
$V_{FCB(AC)}$	Clock Input Threshold	Measured with a AC Pulse at FCB Pin		1	1.5	2	V
I_{EXTLPF}	External Phase Detector Output Current Sourcing Capability Sinking Capability	 $f_{FCB} < f_{SW1}$, V_{EXTLPF} = 0V $f_{FCB} > f_{SW1}$, V_{EXTLPF} = 2.4V			 20 –20		 µA µA
I_{INTLPF}	Internal Phase Detector Output Current Sourcing Capability Sinking Capability	 $f_{SW1} < f_{SW2}$, V_{INTLPF} = 0V $f_{SW1} > f_{SW2}$, V_{INTLPF} = 2.4V			 20 –20		 µA µA
$t_{ON(PLL)1}$	t_{ON1} Modulation Range by External PLL Up Modulation Down Modulation	 I_{ON1} = 60µA, V_{EXTLPF} = 1.8V I_{ON1} = 60µA, V_{EXTLPF} = 0.6V		 186	 233 58	 80	 ns ns
$t_{ON(PLL)2}$	t_{ON2} Modulation Range by Internal PLL Up Modulation Down Modulation	 I_{ON1} = 60µA, V_{EXTLPF} = 1.8V I_{ON1} = 60µA, V_{EXTLPF} = 0.6V		 186	 233 58	 80	 ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliabilty and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$T_J = T_A + (P_D \bullet 34°C/W)$

Note 3: The LTC3708 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

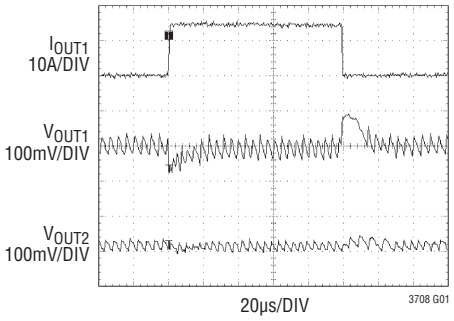
Note 4: Internal reference voltage is tested indirectly by extracting error amplifier offset from the feedback voltage.

Note 5: The LTC3708E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

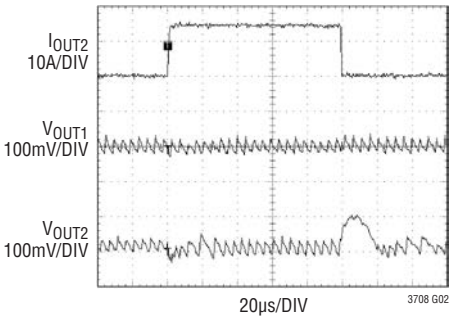
Note 6: $R_{DS(ON)}$ limit is guaranteed by design and/or correlation to static test.

TYPICAL PERFORMANCE CHARACTERISTICS

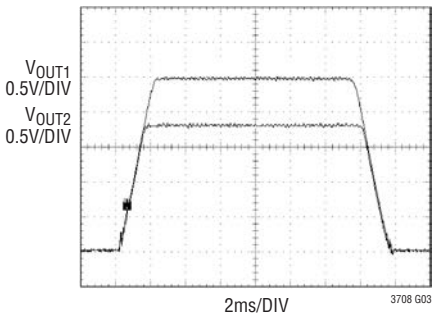
Load Transient on Channel 1



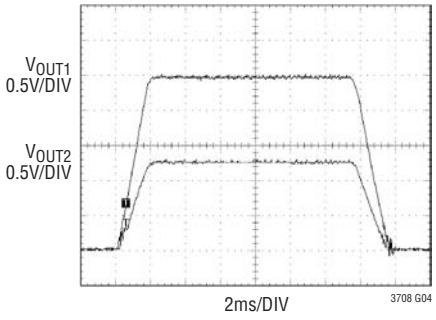
Load Transient on Channel 2



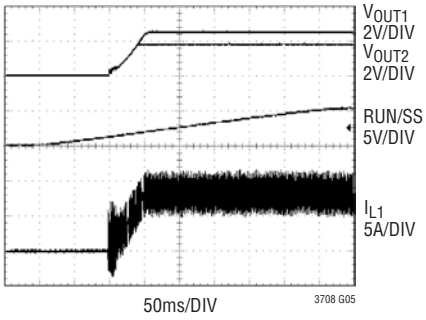
Coincident Tracking



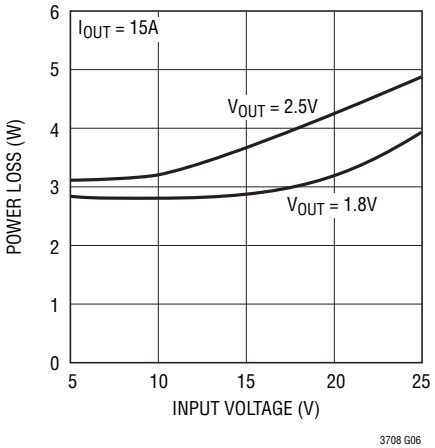
Ratiometric Tracking



Soft-Start

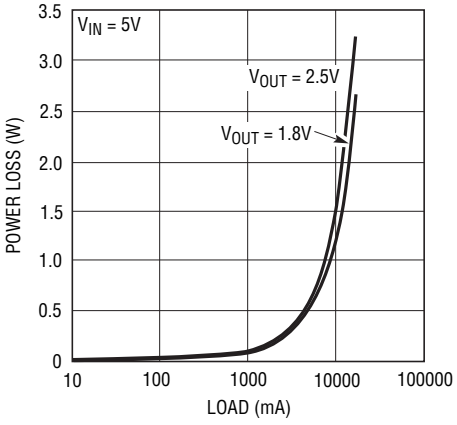


Power Loss vs Input Voltage



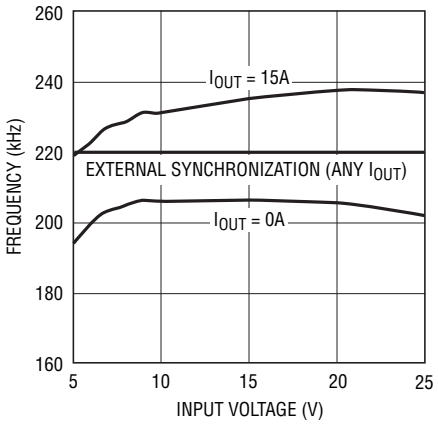
TYPICAL PERFORMANCE CHARACTERISTICS

Power Loss vs Load Current



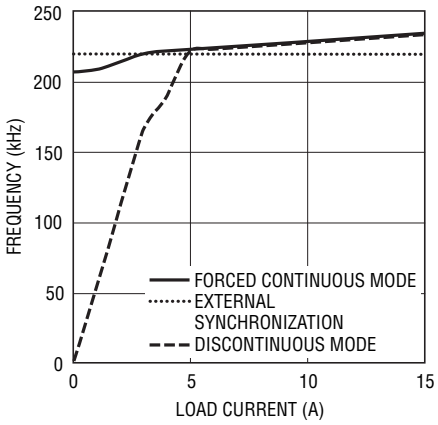
3707 G07

Frequency vs Input Voltage



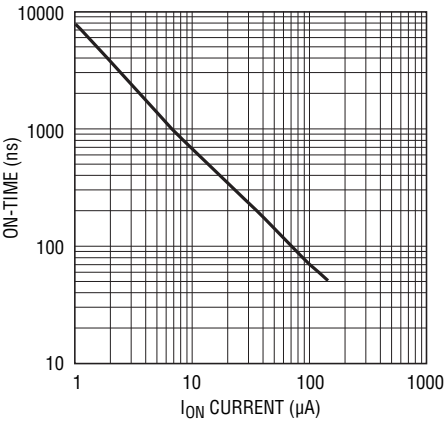
3708 G08

Frequency vs Load Current



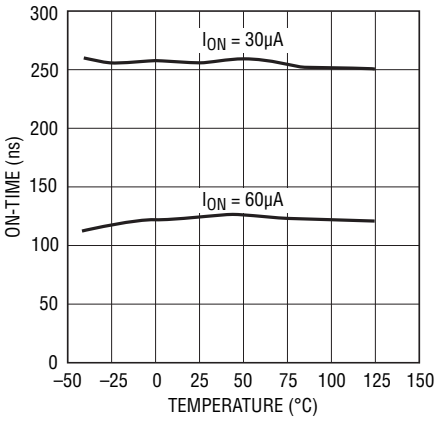
3708 G09

On-Time vs I_{ON} Current



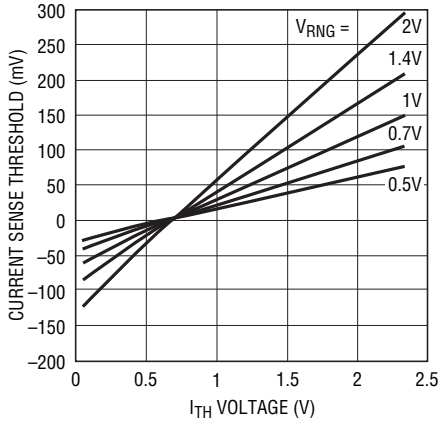
3708 G10

On-Time vs Temperature



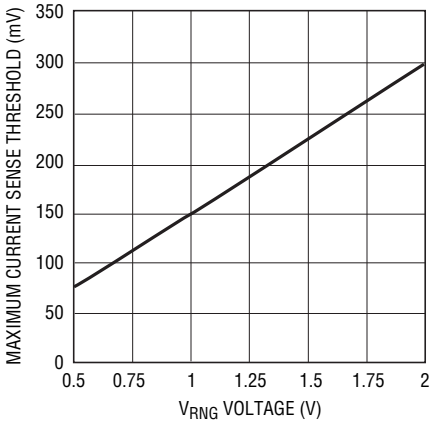
3708 G11

Current Sense Threshold vs I_{TH} Voltage



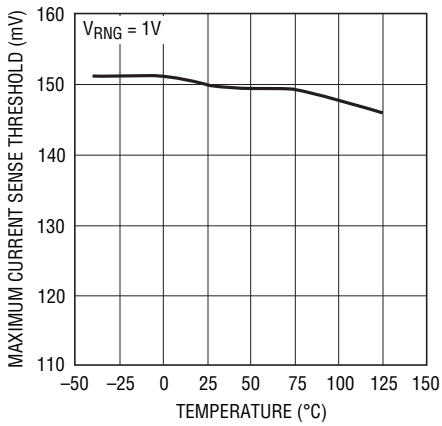
3708 G12

Maximum Current Sense Threshold vs V_{RNG} Voltage



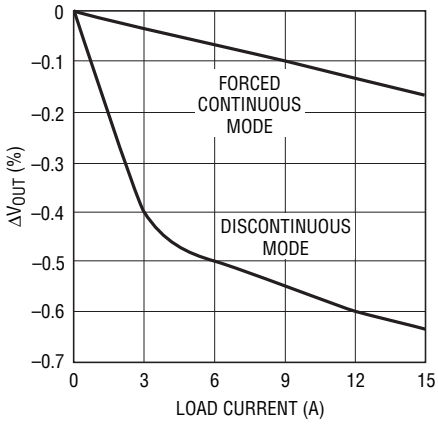
3708 G13

Maximum Current Sense Threshold vs Temperature



3708 G14

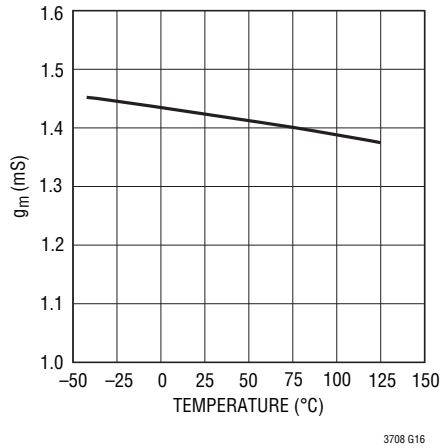
Load Regulation (Figure 13 Circuit)



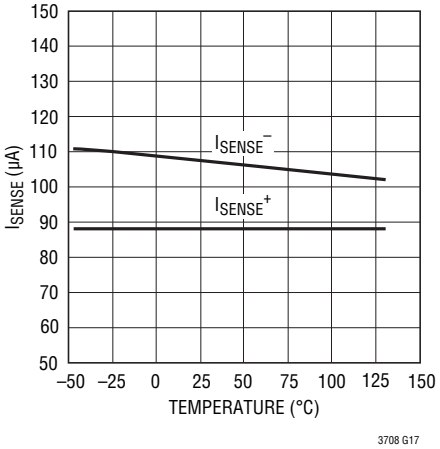
3708 G15

TYPICAL PERFORMANCE CHARACTERISTICS

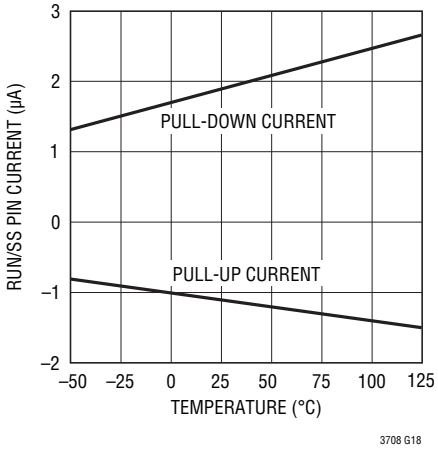
Error Amplifier g_m vs Temperature



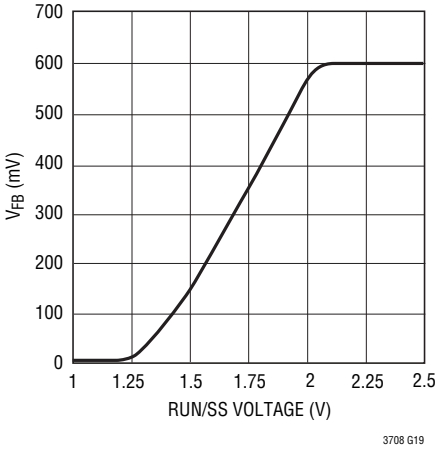
SENSE Pin Input Current vs Temperature



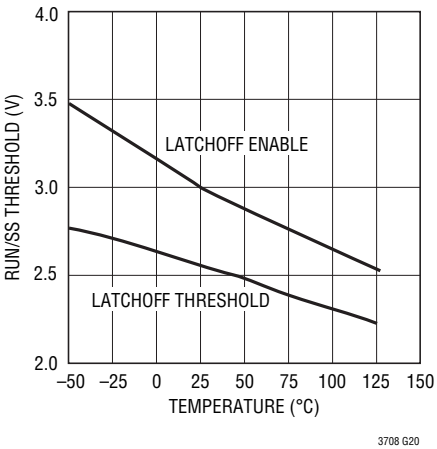
RUN/SS Pin Current vs Temperature



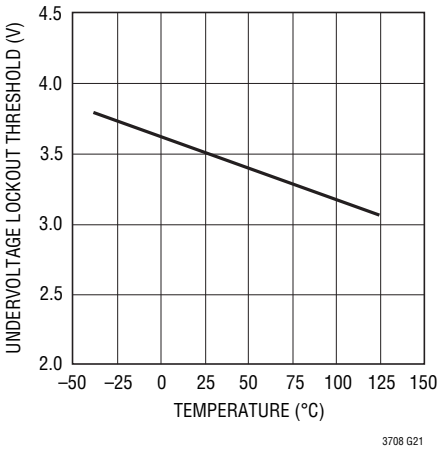
Feedback Voltage vs RUN/SS (Soft-Start)



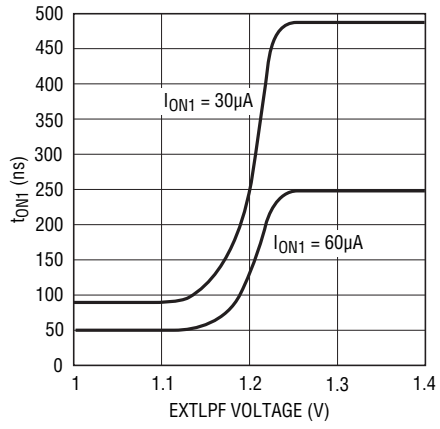
RUN/SS Latch-Off Thresholds vs Temperature



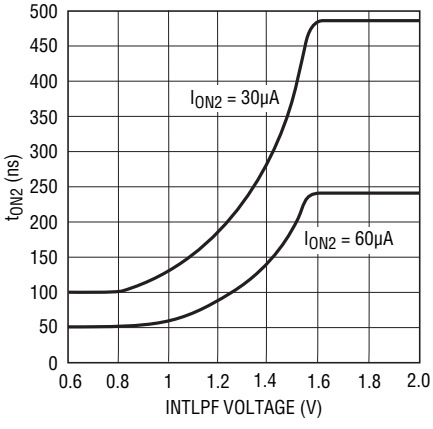
Undervoltage Lockout Threshold vs Temperature



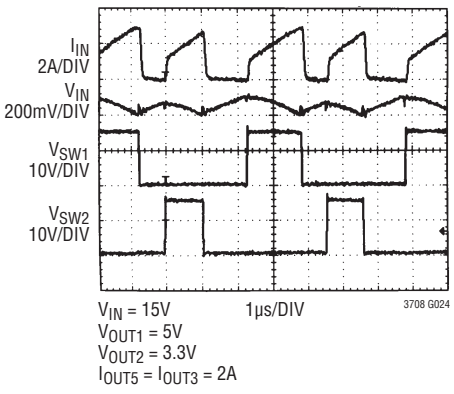
On-Time vs EXTLPF Voltage



On-Time vs INTLPF Voltage

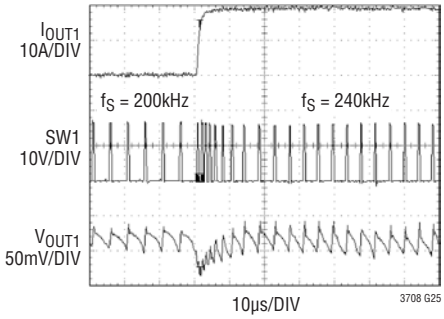


2-Phase Operation

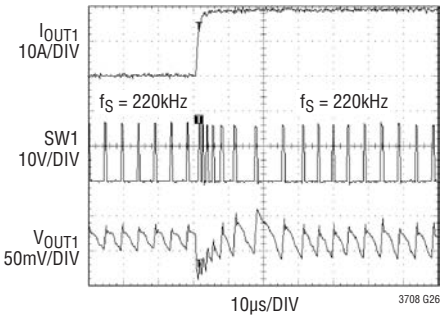


TYPICAL PERFORMANCE CHARACTERISTICS

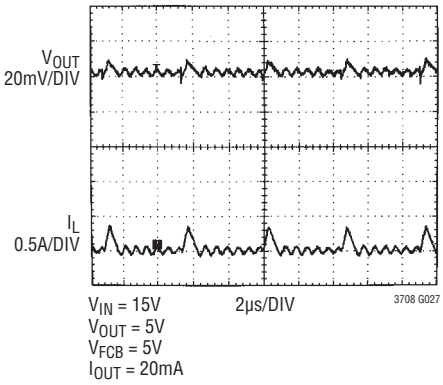
Load Transient Response Without External Synchronization



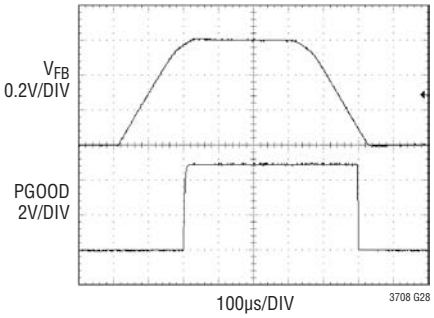
Load Transient Response with External Synchronization



Discontinuous Mode Operation



Power Good Mask



PIN FUNCTIONS

RUN/SS (Pin 1): Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 0.5s/µF) and the time delay for overcurrent latchoff (see Applications Information). Forcing this pin below 0.8V shuts down the LTC3708.

I_{TH1}, I_{TH2} (Pins 2, 8): Error Amplifier Compensation Point and Current Control Threshold. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

V_{FB1}, V_{FB2} (Pins 3, 7): Error Amplifier Feedback Input. This pin connects the error amplifier input to an external resistive divider from V_{OUT}. Additional compensation can be implemented, if desired, using this pin.

TRACK1, TRACK2 (Pins 4, 6): Tie TRACK2 pin to a resistive divider connected to the output of channel 1 for either coincident or ratiometric output tracking. TRACK1 is used in the same manner between multiple LTC3708s (see Applications Information). To disable this feature, tie the pins to V_{CC}. *Do Not Float These Pins.*

SGND (Pins 5, 33): Signal Ground. All small-signal components and compensation components should connect to this ground and eventually connect to PGND at one point. The Exposed Pad of the LTC3708EUH must be soldered to the PCB.

EXTLPF (Pin 9): Filter Connection for the External PLL. This PLL is used to synchronize the LTC3708 to an external clock. If external clock is not used, leave this pin floating.

INTLPF (Pin 10): Filter Connection for the Internal PLL. This PLL is used to phase shift the second channel to the first channel by 180°.

V_{CC} (Pin 17): Main Input Supply. Decouple this pin to SGND with an RC filter (10Ω, 1µF for example).

DRV_{CC} (Pin 21): Driver Supply. Provides supply to the drivers for the bottom gates. Also used for charging the bootstrap capacitors.

BG1, BG2 (Pins 22, 20): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and DRV_{CC}.

PGND1, PGND2 (Pins 23, 19): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{DRVCC} and the (–) terminal of C_{IN}.

SENSE1–, SENSE2– (Pins 24, 18): Current Sense Comparator Input. The (–) input to the current comparator is used to accurately Kelvin sense the bottom side of the sense resistor or MOSFET.

$SENSE1^+$, $SENSE2^+$ (Pins 25, 16): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor (See Applications Information).

SW1, SW2 (Pins 26, 15): Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a Schottky diode voltage drop below ground up to V_{IN}.

TG1, TG2 (Pins 27, 14): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

BOOST1, BOOST2 (Pins 28, 13): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below DRV_{CC} up to V_{IN} + DRV_{CC}.

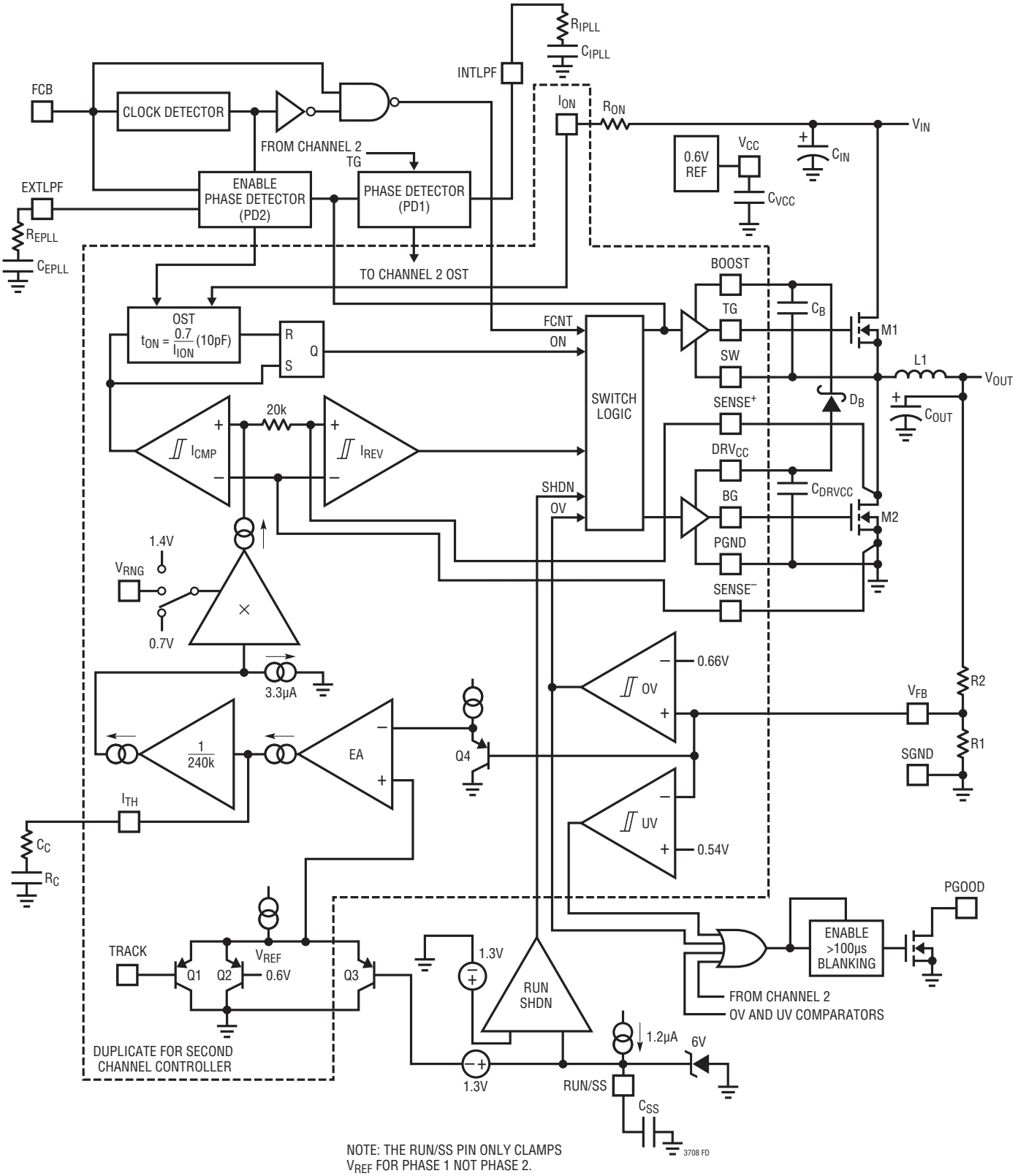
I_{ON1}, I_{ON2} (Pins 29, 12): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

PGOOD (Pin 30): Power Good Output. Open-drain logic output that is pulled to ground when either or both output voltages are not within ±10% of the regulation point. The output voltage must be out of regulation for at least 100µs before the power good output is pulled to ground.

FCB (Pin 31): Forced Continuous and External Clock Input. Tie this pin to ground to force continuous synchronous operation or to V_{CC} to enable discontinuous mode operation at light load. Feeding an external clock signal into this pin will synchronize the LTC3708 to the external clock and enable forced continuous mode.

V_{RNG1}, V_{RNG2} (Pins 32, 11): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be programmed from 0.5V to 2V. The sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to V_{CC}.

FUNCTIONAL DIAGRAM



NOTE: THE RUN/SS PIN ONLY CLAMPS V_{REF} FOR PHASE 1 NOT PHASE 2.

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3708 uses a constant on-time, current mode step-down architecture with two control channels operating at 180 degrees out of phase. In normal operation, each top MOSFET is turned on for a fixed interval determined by its own one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and repeating the cycle. The trip level of the current comparator is set by the I_{TH} voltage which is the output of each error amplifier, EA. Inductor current is determined by sensing the voltage between the $SENSE^-$ and $SENSE^+$ pins using either the bottom MOSFET on-resistance or a separate sense resistor. At low load currents, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV}, which then shuts off M2 resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled when the FCB pin is brought below 1.9V, forcing continuous synchronous operation.

The main control loop is shut down by pulling the RUN/SS pin low, turning off both M1 and M2. Releasing the pin allows an internal 1.2µA current source to charge an external soft-start capacitor, C_{SS}. When this voltage reaches 1.3V, the controller turns on and begins switching, but with the effective reference voltage clamped at 0V. As C_{SS} continues to charge, the effective reference ramps up at the same rate and controls the rise rate of the output voltage.

Operating Frequency

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

When the LTC3708 is synchronized to an external clock, the operating frequency will then be solely determined by the external clock.

Output Overvoltage Protection

An overvoltage comparator OV guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In this condition, M1 is turned off and M2 is turned on and held on until the condition is cleared.

Short-Circuit Detection and Protection

After the controller has been started and given adequate time to charge the output capacitors, the RUN/SS capacitor is used as the short-circuit time-out capacitor. If either one of the output voltages falls to less than 70% of its nominal output voltage, the RUN/SS capacitor begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period, as determined by the size of the RUN/SS capacitor, both controllers will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overridden by providing >5µA pull-up at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during an overcurrent and/or short-circuit condition.

Power Good (PGOOD) Pin

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exceeds a ±10% window around the regulation point. In addition, the output feedback voltage must be out of this window for a continuous duration of at least 100µs before PGOOD is pulled low. This is to prevent any glitch on the feedback voltage from creating a false power bad signal. The PGOOD will indicate high immediately when the feedback voltage is in regulation.

OPERATION (Refer to Functional Diagram)

DRV_{CC}

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The top MOSFET driver is powered from a floating bootstrap capacitor, C_B. This capacitor is normally recharged from DRV_{CC} through an external Schottky diode, D_B, when the top MOSFET is turned off.

2-Phase Operation

For the LTC3708 to operate optimally as a 2-phase controller, the resistors connected to the I_{ON} pins must be selected such that the free-running frequency of each channel is close to that of the other. An internal phase-locked loop (PLL) will then ensure that channel 2 operates at the same frequency as channel 1, but phase shifted by 180°. The loop filter connected to the INTLPF pin provides stability to the PLL. For external clock synchronization, a second PLL is incorporated to adjust the on-time of channel 1 until its frequency is the same as the external clock. Compensation for the external PLL is through the EXTLPF pin.

The loop filter components tied to the INTLPF and EXTLPF pins are used to compensate the internal PPL and external PLL respectively. The typical value ranges are:

INTLPF: R_{IPLL} = 2kΩ to 10kΩ, C_{IPLL} = 10nF to 100nF

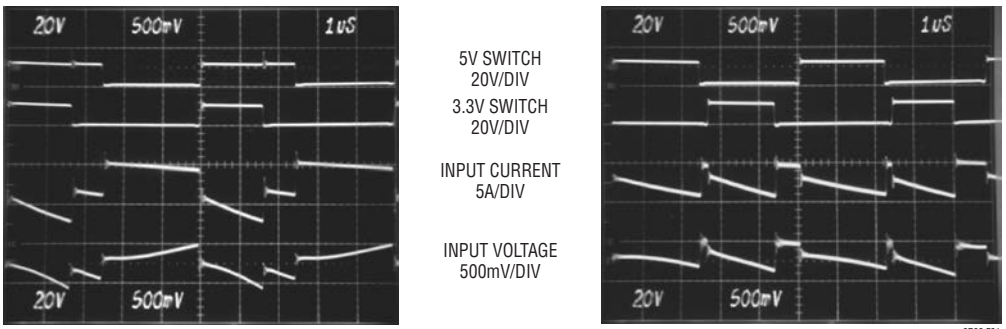
EXTLPF: $R_{EPLL} \leq$ 1kΩ, C_{EPLL} = 10nF to 100nF

For noise suppression, a capacitor with a value of 1nF or less should be placed from INTLPF to ground and EXTLPF to ground.

The LTC3708's 2-phase operation brings considerable benefits to portable applications and automatic electronics. It lowers the input filtering requirement, reduces electromagnetic interference (EMI) and increases the power conversion efficiency. Until the introduction of the 2-phase operation, dual switching regulators operated both channels in phase (i.e., single phase operation). This means that both controlling switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor or battery. Such operation results in higher input RMS current, larger and/or more expensive input capacitors, more power loss and worse EMI in the input source (whether a wall adapter or a battery).

In contrast to single phase operation, the two channels of a 2-phase switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.

Figure 1 compares the input waveforms for a representative single phase dual switching regulator to the 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase dropped the input current from 2.53A_{RMS} to 1.55A_{RMS}.



$I_{IN(MEAS)}$ = 2.53A_{RMS} (1a)

$I_{IN(MEAS)}$ = 1.55A_{RMS} (1b)

Figure 1. Input Waveforms Comparing Single Phase (1a) and 2-Phase (1b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each

OPERATION (Refer to Functional Diagram)

While this is an impressive reduction in itself, remember that the power losses are proportional to I^2_{RMS}, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple current also means that less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage, V_{IN}. Figure 2 shows how the RMS input current varies for single phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitance requirement to that for just one channel operating at maximum current and 50% duty cycle.

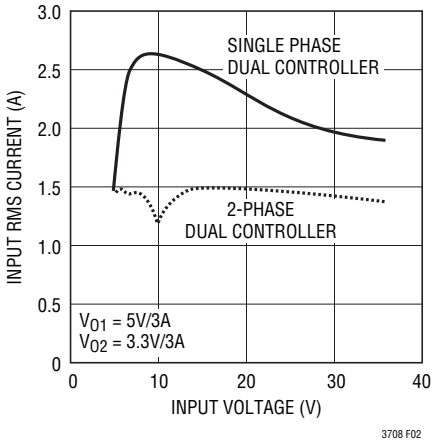


Figure 2. RMS Input Current Comparison

APPLICATIONS INFORMATION

The basic LTC3708 application circuit is shown on the first page of this data sheet. External component selection is primarily determined by the maximum load current and begins with the selection of the power MOSFET switches and/or sense resistor. For the LTC3708, the inductor current is determined by the $R_{DS(ON)}$ of the synchronous MOSFET or by a sense resistor when the user opts for more accurate current sensing. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across the $R_{DS(ON)}$ of the synchronous MOSFET or through a sense resistor that appears between the SENSE$^+$ and SENSE$^-$ pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately $V_{RNG}/7$. The current mode control loop will not allow the inductor current valleys to exceed $V_{RNG}/(7 \bullet R_{SENSE})$. In practice, one should allow some margin for variations in the LTC3708 and external component values. A good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

The voltage of the V_{RNG} pin can be set using an external resistive divider from V_{CC} between 0.5V and 2V, resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to ground or V_{CC}, in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.4 times this nominal value.

Connecting the SENSE$^+$ and SENSE$^-$ Pins

The LTC3708 provides the user with an optional method to sense current through a sense resistor instead of using the $R_{DS(ON)}$ of the synchronous MOSFET. When using a sense resistor, it is placed between the source of the synchronous MOSFET and ground. To measure the voltage across this resistor, connect the SENSE$^+$ pin to the source of the synchronous MOSFET and the SENSE$^-$ pin to the other end of the resistor. The SENSE$^+$ and SENSE$^-$ pins provide the Kelvin connections, ensuring accurate voltage measurement across the resistor. Using a sense resistor provides a well-defined current limit, but adds cost and reduces efficiency. Alternatively, one can use the synchronous MOSFET as the current sense element by simply connecting the SENSE$^+$ pin to the switch node SW and the SENSE$^-$ pin to the source of the synchronous MOSFET, eliminating the sense resistor. This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed below.

Power MOSFET Selection

Each output stage of the LTC3708 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance, C_{RSS}, and maximum current, $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V DRV_{CC} supply. Consequently, logic-level threshold MOSFETs must be used in LTC3708 applications. If the driver's voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. Additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C. For a maximum junction temperature of 100°C, using a value $\rho_{100°C} = 1.3$ is reasonable (see Figure 3).

APPLICATIONS INFORMATION

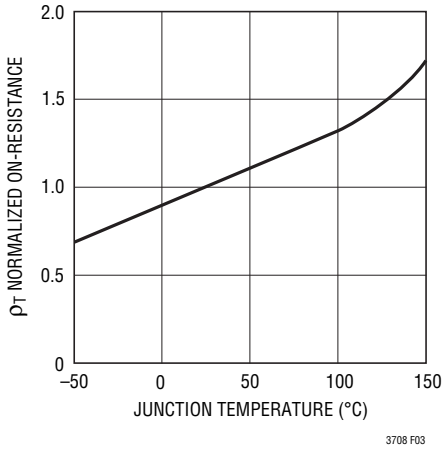


Figure 3. $R_{DS(ON)}$ vs Temperature

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. When the LTC3708 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_{T(TOP)} \bullet R_{DS(ON)} + (0.5) \bullet V_{IN}{}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f \bullet R_{DR} \bullet \left(\frac{1}{(DRV_{CC} - V_{GS(TH)})} + \frac{1}{V_{GS(TH)}} \right)$$

$$P_{BOT} = D_{BOT} \bullet I_{OUT(MAX)}{}^2 \bullet \rho_{T(BOT)} \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short circuit or at high input voltage.

Operating Frequency

The choice of operating frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching and driving losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of LTC3708 applications is determined implicitly by the one-shot timer that controls the on time, t_{ON}, of the top MOSFET switch. The on time is set by the current into the I_{ON} pin according to:

$$t_{ON} = \frac{0.7}{I_{ION}}(10pF)$$

Tying a resistor, R_{ON}, from V_{IN} to the I_{ON} pin yields an on time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{0.7 \bullet R_{ON}(10pF)}$$

Figure 4 shows how R_{ON} relates to switching frequency for several common output voltages.

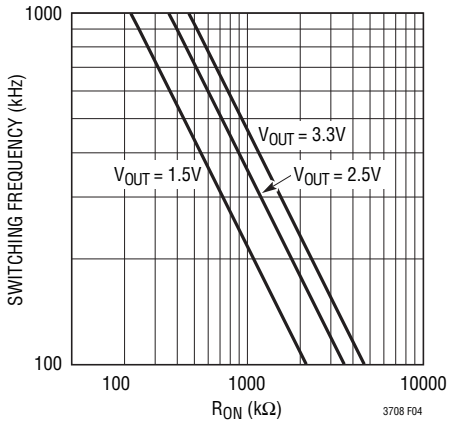


Figure 4. Switching Frequency vs R_{ON}

APPLICATIONS INFORMATION

PLL and Frequency Synchronization

In the LTC3708, there are two onboard phase-locked loops (PLL). One PLL is used to achieve frequency locking and 180° phase shift between the two channels while the second PLL locks onto the rising edge of an external clock. Since the LTC3708 uses a constant on-time architecture, the error signal generated by the phase detector of the PLL is used to vary the on time to achieve frequency locking and phase separation. The variable on-time range is from $0.5 \bullet t_{ON}$ to $2 \bullet t_{ON}$, where t_{ON} is the initial on time set by the R_{ON} resistor.

To fully utilize the frequency synchronization range of the PLL, it is advisable to set the initial on time properly so that the two channels have close free-running frequencies. Frequencies far apart may exceed the synchronization capability of the PLL. If the two output voltages are V_{OUT1} and V_{OUT2}, for example, R_{ON} resistors should then be selected proportionally:

$$\frac{R_{ON1}}{R_{ON2}} = \frac{V_{OUT1}}{V_{OUT2}}$$

Similarly, if the external PLL is engaged to synchronize to an external frequency of f_{EXT}, R_{ON1} should be selected close to:

$$R_{ON1} = \frac{V_{OUT1}}{0.7 \bullet f_{EXT} \bullet 10pF}$$

$$\text{hence, } \left(R_{ON2} = \frac{V_{OUT2}}{0.7 \bullet f_{EXT} \bullet 10pF} \right)$$

In this case, channel 1 will first be synchronized to the external frequency and channel 2 will then be synchronized to channel 1 with 180° phase separation.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L} \right) \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and ripples in the output voltage. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size and efficiency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}} \right) \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida and Panasonic.

Schottky Diode Selection

The Schottky diodes in parallel with both bottom MOSFETs conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which causes a modest (about 1%) efficiency loss. The diodes can be rated for about one-half to one-fifth of the full load current since they are on for only a fraction of the duty cycle. In order for the diodes to be effective, the inductance between them and the bottom MOSFETs must be as small as possible, mandating that these components be placed as close as possible in the circuit board layout. The diodes can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case RMS current occurs when only one controller is operating. The controller with the

APPLICATIONS INFORMATION

highest (V_{OUT})(I_{OUT}) product needs to be used in the formula below to determine the maximum RMS current requirement. Increasing the output current, drawn from the other out-of-phase controller, will actually decrease the input RMS ripple current from this maximum value (see Figure 2).

The type of input capacitor, value and ESR rating have efficiency effects that need to be considered in the selection process. The capacitance value chosen should be sufficient to store adequate charge to keep pulsating input currents down. 20µF to 40µF is usually sufficient for a 25W output supply operating at 200kHz. The ESR of the capacitor is important for capacitor power dissipation as well as overall efficiency. All of the power (RMS ripple current^2 • ESR) not only heats up the capacitor but wastes power from the battery.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramic voltage coefficients are very high and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface-mount applicability; electrolytics' higher ESR and dryout possibility require several to be used. 2-phase systems allow the lowest amount of capacitance overall. As little as one 22µF or two to three 10µF ceramic capacitors are an ideal choice in a 20W to 35W power supply due to their extremely low ESR. Even though the capacitance at 20V is substantially below their rating at zero-bias, very low ESR loss makes ceramics an ideal candidate for highest efficiency battery operated systems. Also consider parallel ceramic and high quality electrolytic capacitors as an effective means of achieving ESR and bulk capacitance goals.

In continuous mode, the current of the top N-channel MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN}-V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The benefit of the LTC3708 2-phase operation can be calculated by using the equation above for the higher power channel and then calculating the loss that would have resulted if both controller channels switch on at the same time. The total RMS power lost is lower when both controllers are operating due to the interleaving of current pulses through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Remember that input protection fuse resistance, battery resistance and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. *The overall benefit of a 2-phase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.* The drains of the two top MOSFETS should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

The selection of C_{OUT} is driven by the effective series resistance (ESR) required to minimize voltage ripple and load step transients. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance, and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

APPLICATIONS INFORMATION

Manufacturers such as Nichicon, United Chemi-Con and Sanyo can be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest (ESR) (size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductance effects.

In surface mount applications multiple capacitors may need to be used in parallel to meet the ESR, RMS current handling and load step requirements of the application. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower storage capacity per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors can be used in cost-driven applications providing that consideration is given to ripple current ratings, temperature and long term reliability. A typical application will require several to many aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, Sanyo POSCAP, NEC Neocap, Cornell Dubilier ESRE and Sprague 595D series. Consult manufacturers for other specific recommendations.

Top MOSFET Driver Supply (C_B, D_B in the Functional Diagram)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from DRV_{CC} when the switch node is low. Note that the average voltage across C_B is approximately DRV_{CC}. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $V_{IN} + DRV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF is adequate.

Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 2.3V threshold (typically to V_{CC}) enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and the ripple current depends on the choice of inductor value and operating frequency as well as the input and output voltages.

Tying the FCB pin below 1.9V forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

Besides providing a logic input to force continuous operation, the FCB pin acts as the input for external clock synchronization. Upon detecting the presence of an external clock signal, channel 1 will lock on to this external clock and this will be followed by channel 2 (see PLL and Frequency Synchronization).

The LTC3708 defaults to forced continuous mode when sychronized to an external clock or when the PGOOD signal is low.

Fault Conditions: Current Limit

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3708, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)} \bullet \rho_T} + \frac{1}{2} \bullet \Delta I_L$$

APPLICATIONS INFORMATION

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions which cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed junction temperature and the resulting value of I_{LIMIT}, which heats the junction.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

For a more accurate current limiting, a sense resistor can be used. Sense resistors in the 1W power range can be easily available in the 5%, 2% or 1% tolerance. The temperature coefficient of these resistors is very low, ranging from ±250ppm/°C to ±75ppm/°C. In this case, the ($R_{DS(ON)} \bullet \rho_T$) product in the above equation can simply be replaced by the R_{SENSE} value.

Minimum Off Time and Dropout Operation

The minimum off time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3708 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 270ns. The minimum off time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

A plot of maximum frequency vs duty cycle is shown in Figure 5.

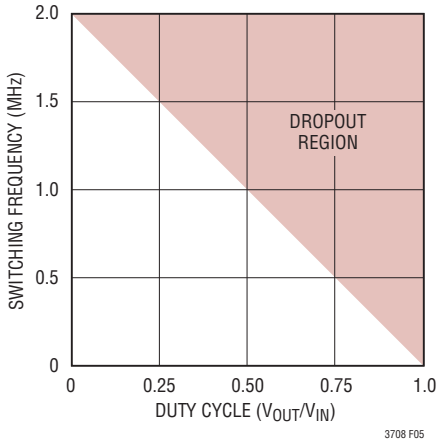


Figure 5. Maximum Switching Frequency vs Duty Cycle

Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC3708 as well as a timer for soft-start and overcurrent latchoff.

Pulling the RUN/SS pin below 0.8V shuts down the LTC3708. Releasing the pin allows an internal 1.2µA internal current source to charge the external capacitor, C_{SS}. If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.3V}{1.2\mu A} \bullet C_{SS} = (1.1s/\mu F)C_{SS}$$

When the RUN/SS voltage reaches the ON threshold (typically 1.3V), the LTC3708 begins operating with a clamp on channel 1's reference voltage. The clamp level is one threshold voltage below RUN/SS. As the voltage on RUN/SS continues to rise, channel 1's reference is raised at the same rate, achieving monotonic output voltage soft-start (Figure 6). When RUN/SS rises 0.6V above the ON threshold, the reference clamp is invalidated and the internal precision reference takes over. When channel 2 is tracked to channel 1, soft-start on channel 2 is automatically achieved (see Output Voltage Tracking).

APPLICATIONS INFORMATION

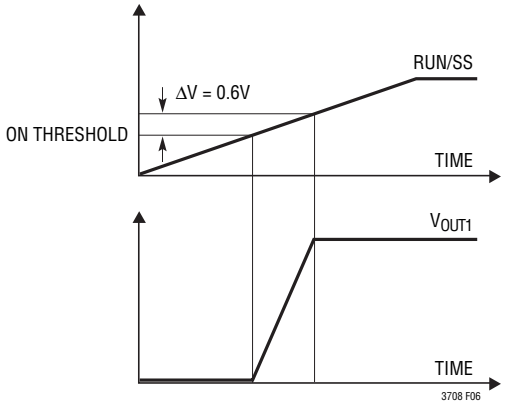


Figure 6. Monotonic Soft-Start Waveforms

Controlled soft-start requires that the timing capacitor, C_{SS}, be made large enough to guarantee that the output can track the voltage rise on the RUN/SS pin. The minimum C_{SS} capacitance can be calculated:

$$C_{SS} > \frac{R1+R2}{R1} \bullet \frac{30\mu A \bullet R_{SENSE}}{V_{RNG}} \bullet C_{OUT}$$

where R1 and R2 are the feedback resistive dividers (Functional Diagram), C_{OUT} is the output capacitance and R_{SENSE} is the current sense resistance. When bottom MOSFET $R_{DS(ON)}$ is used for current sensing, R_{SENSE} should be replaced with the worst-case $R_{DS(ON)(MAX)}$. Generally, 0.1µF is more than sufficient for C_{SS}.

After the controller has been started and given adequate time to charge the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 3V and if either output voltage falls below 70% of its regulated value, a short-circuit fault is assumed. A 2µA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 2.5V, the controller turns off all power MOSFETs, shutting down both channels. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

Overcurrent latchoff operation is not always needed or desired and can prove annoying during troubleshooting. This feature can be overridden by adding a pull-up current of >5µA to the RUN/SS pin (Figure 7). The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period.

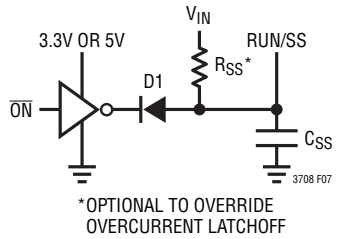


Figure 7. RUN/SS Pin Interfacing with Latchoff Defeated

Output Voltage Tracking

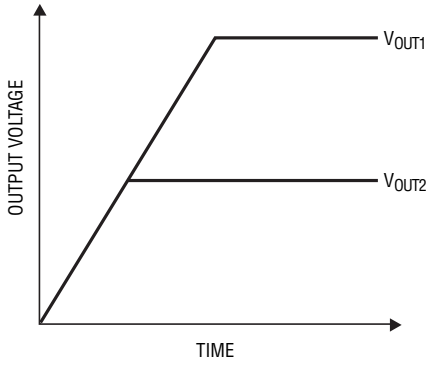
The LTC3708 allows the user to program how the second channel output ramps up and down by means of the TRACK2 pin. Through this pin, the second channel output can be set up to either coincidently or ratiometrically track the channel 1 output, as shown in Figure 8.

Similar to RUN/SS, the TRACK2 pin acts as a clamp on channel 2's reference voltage. V_{OUT2} is referenced to the TRACK2 voltage when the TRACK2 < 0.6V and to the internal precision reference when TRACK2 > 0.6V.

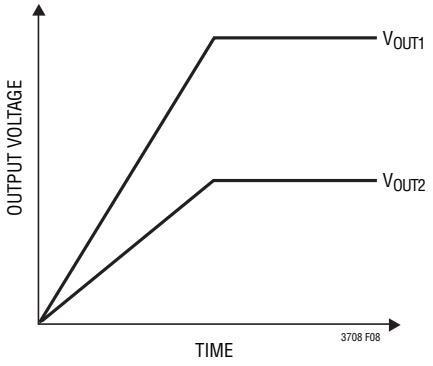
To implement the tracking in Figure 8a, connect an extra resistive divider to the output of channel 1 and connect its midpoint to the TRACK2 pin. The ratio of this divider should be selected the same as that of channel 2's feedback divider (Figure 9a). **In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}.** To implement the ratiometric tracking in Figure 8b, no extra divider is needed; simply connect the TRACK2 pin to the V_{FB1} pin (Figure 9b).

By selecting different resistors, the LTC3708 can achieve different modes of tracking including the two in Figure 8. So which mode should be programmed? While either mode in Figure 8 satisfies most practical applications, there does exist some trade-off. The ratiometric mode saves a pair of resistors but the coincident mode offers better output regulation. This can be better understood with the help of Figure 10. At the input stage of channel 2's error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRACK2 voltage is substantially higher than 0.6V at steady state and effectively turns off

APPLICATIONS INFORMATION

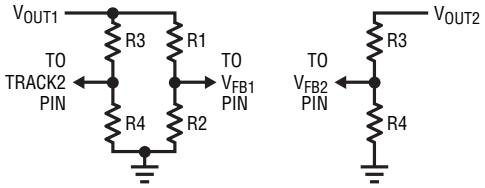


(8a) Coincident Tracking

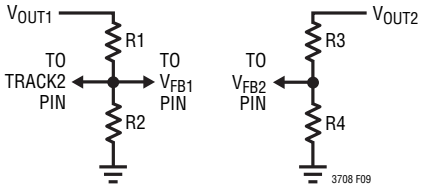


(8b) Ratiometric Tracking

Figure 8. Two Different Modes of Output Voltage Tracking



(9a) Coincident Tracking Setup



(9b) Ratiometric Tracking Setup

Figure 9. Setup for Coincident and Ratiometric Tracking

$$\left(\frac{R1}{R2}=\frac{V_{OUT1}}{0.6}-1,\frac{R3}{R4}=\frac{V_{OUT2}}{0.6}-1\right)$$

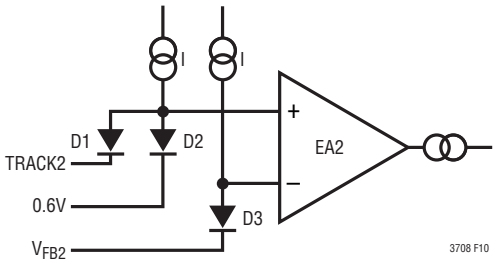


Figure 10. Equivalent Input Circuit of Error Amplifier of Channel 2

D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.6V reference. In the ratiometric mode, however, TRACK2 equals 0.6V even at steady state. D1 will divert part of the bias current and make V_{FB2} slightly lower than 0.6V. Although this error is minimized by the exponential I-V characteristic of the diodes, it does impose a finite amount of output voltage deviation. Further, when channel 1's output experiences dynamic excursions (under load transient, for example), channel 2 will be affected as well. *For better output regulation, use the coincident tracking mode instead of ratiometric.*

The number of resistors in Figure 9a can be further reduced with the scheme in Figure 11.

In a system that requires more than two tracked supplies, multiple LTC3708s can be daisy-chained through the TRACK1 pin. TRACK1 clamps channel 1's reference in the same manner TRACK2 clamps channel 2. To eliminate the possibility of multiple LTC3708s coming on at different times, only the master LTC3708's RUN/SS pin should be

APPLICATIONS INFORMATION

connected to a soft-start capacitor. All other LTC3708s should have their RUN/SS pins pulled up to V_{CC} with a resistor between 50k and 300k. Figure 12 shows the circuit with four outputs. Three of them are programmed in the coincident mode while the fourth one tracks ratiometrically. If output tracking is not needed, connect the TRACK pins to V_{CC}. *Do Not Float These Pins.*

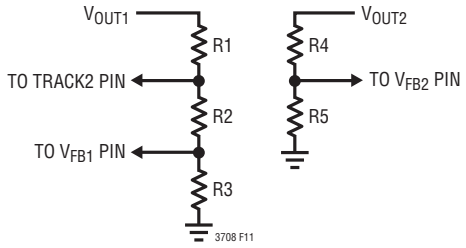


Figure 11. Alternative Setup for Coincident Tracking

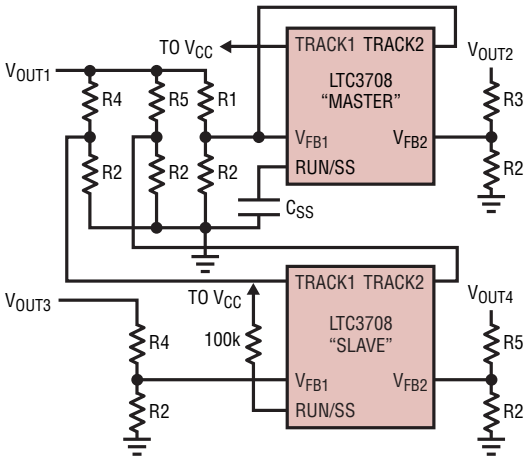
$$\left(\frac{R1+R2}{R3}=\frac{V_{OUT1}}{0.6}-1,\frac{R1}{R2+R3}=\frac{R4}{R5}=\frac{V_{OUT2}}{0.6}-1\right)$$

Efficiency Considerations

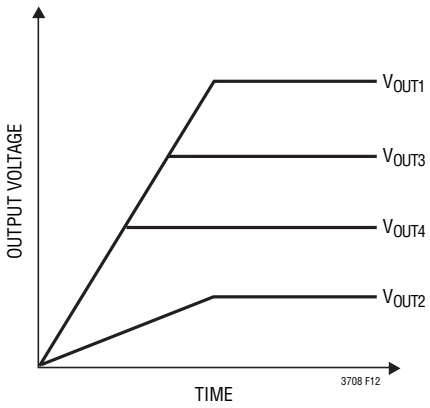
The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement.

Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3708 circuits:

1. DC I^2R Losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode, the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)}$ = 0.01Ω and R_L = 0.005Ω, the loss will range from 15mW up to 1.5W as the output current varies from 1A to 10A.



(12a) Circuit Setup



(12b) Output Voltage

Figure 12. Four Outputs with Tracking and Ratiometric Sequencing

$$\left(\frac{R1}{R2}=\frac{V_{OUT1}}{0.6}-1,\frac{R3}{R2}=\frac{V_{OUT2}}{0.6}-1,\frac{R4}{R2}=\frac{V_{OUT3}}{0.6}-1,\frac{R5}{R2}=\frac{V_{OUT4}}{0.6}-1\right)$$

APPLICATIONS INFORMATION

2. Transition Loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \approx (0.5) \bullet V_{IN}^2 \bullet I_{OUT} \bullet C_{RSS} \bullet f \bullet R_{DS(ON)\_DRV} \left(\frac{1}{DRV_{CC} - V_{GS(TH)}} + \frac{1}{V_{GS(TH)}} \right)$$

3. DRV_{CC} and V_{CC} Current. This is the sum of the MOSFET driver and control currents. The driver current supplies the gate charge Q_G required to switch the power MOSFETs. This current is typically much larger than the control circuit current. In continuous mode operation:

$$I_{GATECHG} = f(Q_{G(TOP)} + Q_{G(BOT)})$$

4. C_{IN} Loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries. The LTC3708 2-phase architecture typically halves this C_{IN} loss over the single phase solutions.

Other losses, including C_{OUT} ESR loss, Schottky conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making any adjustments to improve efficiency, the final arbiter is the total input current for the regulator at your operating point. If you make a change and the input current decreases, then you improve the efficiency. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problems. The I_{TH} pin external components shown in Figure 13 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Linear Technology Application Note 76.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 7V to 28V (15V nominal), V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, $I_{OUT1(MAX)}$ = $I_{OUT2(MAX)}$ = 10A, f = 500kHz and V_{OUT2} to track V_{OUT1}.

First calculate the timing resistor:

$$R_{ON1} = \frac{2.5V}{(0.7V)(500kHz)(10pF)} = 714k$$

Select a standard value of 715k.

$$R_{ON2} = \frac{1.8V}{(0.7V)(500kHz)(10pF)} = 514k$$

Select a standard value of 511k.

Next, choose the feedback resistors:

$$\frac{R1}{R2} = \frac{2.5V}{0.6V} - 1 = 3.17$$

Select R1 = 31.6k, R2 = 10k.

$$\frac{R3}{R4} = \frac{1.8V}{0.6V} - 1 = 2$$

Select R3 = 20k, R4 = 10k.

For V_{OUT2} to coincidently track V_{OUT1} at start-up, connect an extra pair of R3 and R4 across V_{OUT1} with its midpoint tied to the TRACK2 pin.

APPLICATIONS INFORMATION

Third, design the inductors for about 40% ripple current at the maximum V_{IN}:

$$L1=\frac{2.5V}{(500kHz)(0.4)(10A)}\left(1-\frac{2.5V}{28V}\right)=1.1\mu H$$

A standard 1µH inductor will result in 45% of ripple current (4.5A) at worst case.

$$L2=\frac{1.8V}{(500kHz)(0.4)(10A)}\left(1-\frac{1.8V}{28V}\right)=0.8\mu H$$

L2 can also use 1µH to save some BOM (Bill of Material) cost; the resulting ripple current is 3.4A.

The selection of MOSFETs is simplified by the fact that both channels have the same maximum output current. Select the top and bottom MOSFETs for one channel and the same MOSFETs can be used for the other. Take channel 1 for calculation and begin with the bottom synchronous MOSFET. As stated previously in the Power MOSFET Selection section, the major criterion in selecting the bottom MOSFET is low $R_{DS(ON)}$. Choose an Si4874 for example: $R_{DS(ON)}$ = 0.0083Ω (nom) 0.010Ω (max), θ_{JA} = 40°C/W. The nominal sense voltage is:

$V_{SNS(NOM)}$ = (10A)(1.3)(0.0083) = 108mV

Tying V_{RNG1} to 1.1V will set the current sense voltage range for a nominal value of 110mV with the current limit occurring at 146mV. To check if the current limit is acceptable, assume a junction temperature of about 80°C above a 70°C ambient with $\rho_{150°C}$ = 1.5:

$$I_{LIMIT}\geq\frac{146mV}{(1.5)(0.010\Omega)}+\frac{1}{2}(4.1A)=11.8A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT}=\frac{28V-2.5V}{28V}(11.8A)^2(1.5)(0.010\Omega)=1.9W$$

T_J = 70°C + (1.90W)(40°C/W) = 146°

Because the top MOSFET is on for only a short time, an Si4884 will be sufficient: $R_{DS(ON)}$ = 0.0165Ω (max), C_{RSS} = 190pF, $V_{GS(TH)}$ = 1V, θ_{JA} = 42°C/W. Checking its power dissipation at current limit with $\rho_{130°C}$ = 1.6:

$$P_{TOP}=\frac{2.5V}{28V}(11.8A)^2(1.6)(0.0165\Omega)+(0.5)(28V)^2(11.8A)(190pF)(500kHz)(2\Omega)\left(\frac{1}{5V-1V}+\frac{1}{1V}\right)$$

$$=0.33W+1.10W=1.43W$$

T_J = 70°C + (1.43W)(42°C/W) = 130°

The junction temperatures for both top and bottom MOSFETs will be significantly less at nominal current, but the above analysis shows that careful attention to PCB layout and heat sinking will be necessary in this circuit. The same MOSFETs (Si4874 and Si4884) can be used for channel 2.

Finally, an input capacitor is chosen for an RMS current rating of about 5A at 85°C and the output capacitors are chosen for a low ESR of 0.013Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT1(RIPPLE)}=\Delta I_{L1}\bullet\left(ESR+\frac{1}{8\bullet f\bullet C_{OUT}}\right)$$

$$=4.5A\bullet\left(0.013\Omega+\frac{1}{8\bullet 500kHz\bullet 470\mu F}\right)$$

$$=60mV$$

$$\Delta V_{OUT2(RIPPLE)}=\Delta I_{L2}\bullet\left(ESR+\frac{1}{8\bullet f\bullet C_{OUT}}\right)$$

$$=3.4A\bullet\left(0.013\Omega+\frac{1}{8\bullet 500kHz\bullet 470\mu F}\right)$$

$$=46mV$$

However, a 0A to 10A load step will cause an output change of up to:

$\Delta V_{OUT(STEP)} = \Delta I_{LOAD(ESR)}$ = (10A)(0.013Ω) = 130mV

An optional 22µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 13.

APPLICATIONS INFORMATION

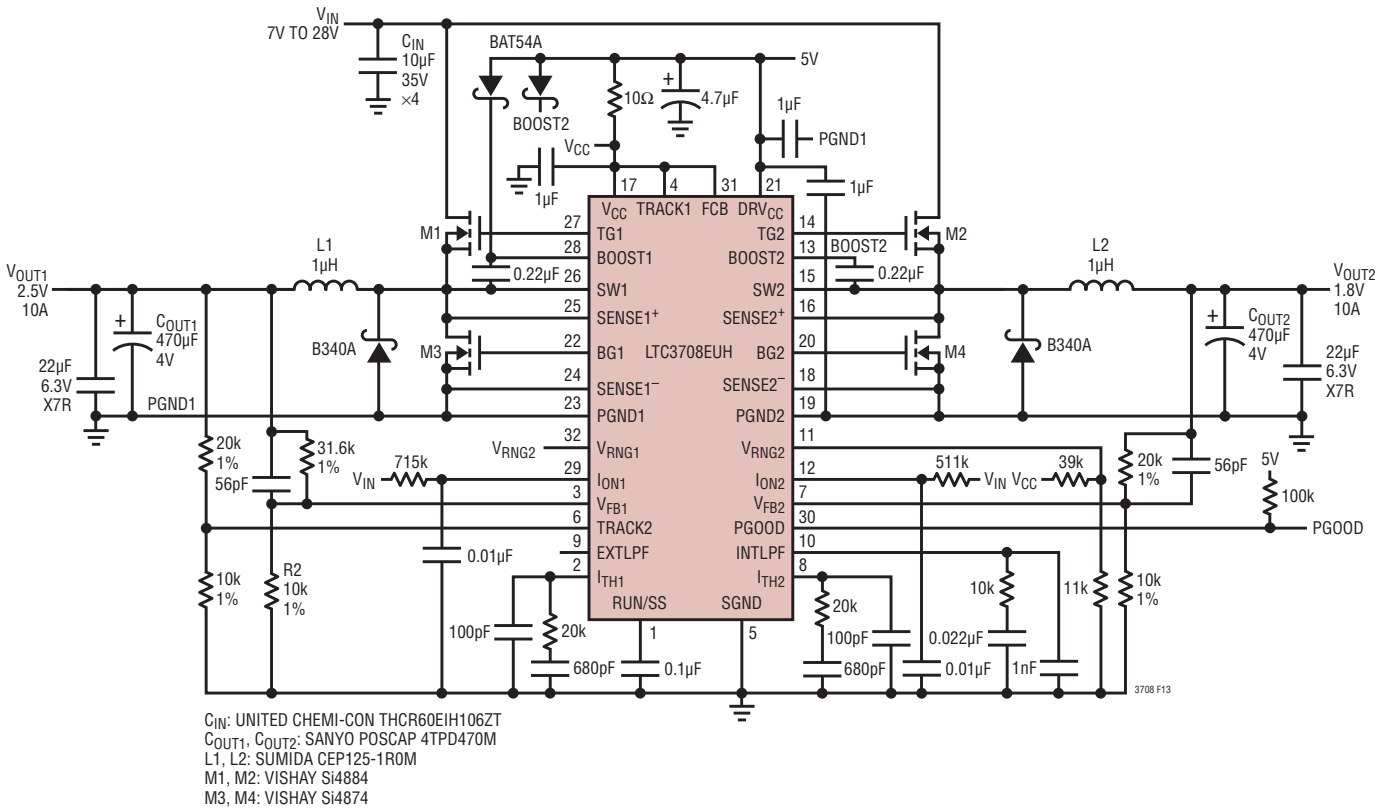


Figure 13. Design Example: 2.5V/10A and 1.8V/10A at 500kHz with Output Tracking

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3708. These items are also illustrated graphically in Figure 14. Figure 15 further shows the current waveforms present in the various branches of the 2-phase synchronous Buck regulators operating in the continuous mode.

- Place the loop of M1, M3 and C_{IN1} in a compact area. This loop conducts high pulsating current and its area needs to be minimized. Place M2, M4 and C_{IN2} in the same way.
- Place C_{IN1} and C_{IN2} within the distance of 1cm. Longer distance may cause a large resonant loop.
- Connect the negative plates of C_{OUT1} and C_{DR1} to PGND1 before it joins PGND2 at the ground plane. Connect C_{OUT2} and C_{DR2} in the same way so that power grounds are separated before they meet at a single point.
- Cover the board area under the LTC3708 with a SGND plane. For the LTC3708EUH, solder the back of the IC to this plane. Separate SGND from the power ground and connect all signal components (I_{TH}, V_{FB}, I_{ON}, V_{CC}, EXTLPF, INTLPF, V_{RNG}, TRACK and RUN/SS) to the SGND plane before it joins PGND. Connect SGND to the gound plane at a single point.
- Run SENSE$^+$ and SENSE$^-$ across the bottom MOSFET (or R_{SENSE} when a separate current sensing resistor is used) with Kelvin connection (Figure 16). Route SENSE$^+$ and SENSE$^-$ together with minimum PC trace separation. The filter capacitor (when used) between SENSE$^+$ and SENSE$^-$ should be as close to the LTC3708 as possible.
- Keep the high dV/dt nodes SW, TG and BOOST away from sensitive small-signal nodes.

APPLICATIONS INFORMATION

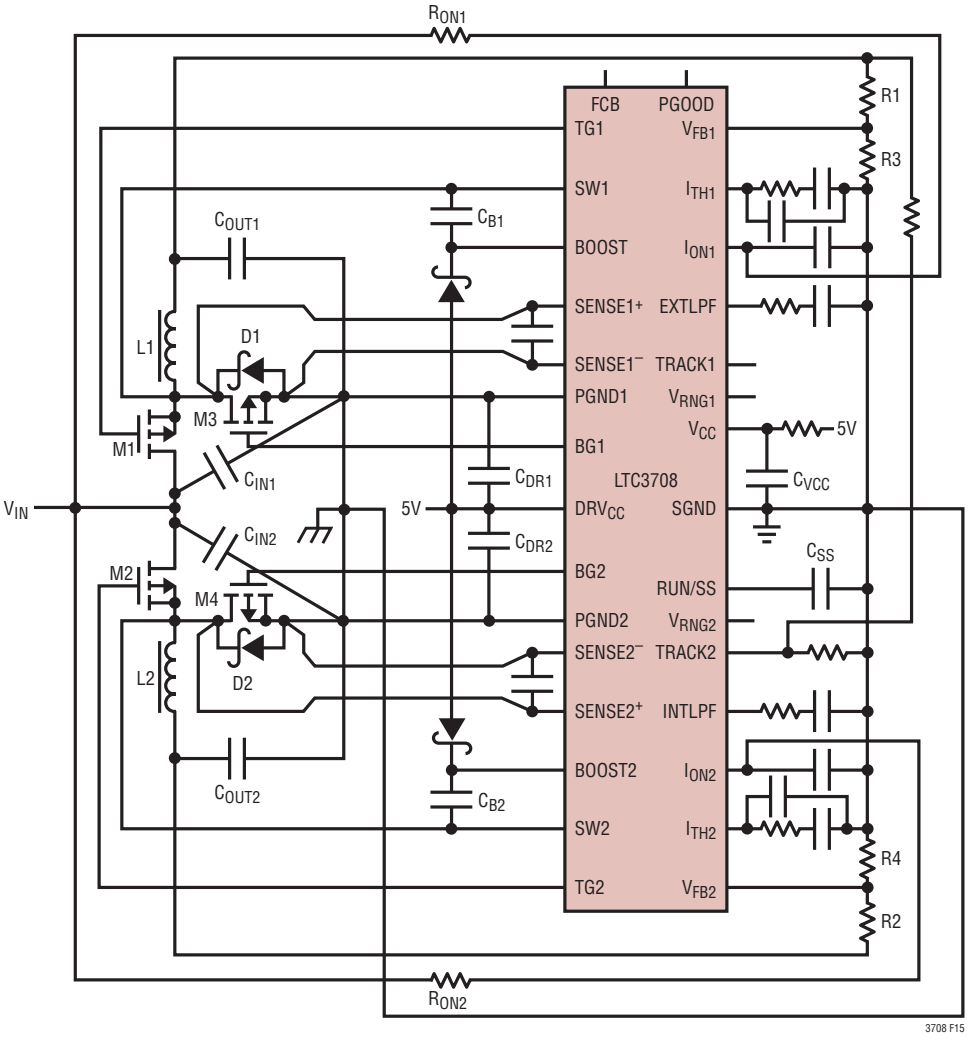


Figure 14. LTC3708 Layout Diagram

- Connect the decoupling capacitors C_{DR1} and C_{DR2} close to the DRV_{CC} and PGND pins. Connect C_{B1} and C_{B2} close to the BOOST and SW pins.
- Connect the decoupling capacitor C_{VCC} right across the V_{CC} pin and SGND plane. Connect the EA compensation components close to the I_{TH} pins. Connect the PLL loop filter close to the EXTLPF and INTLPF pins. Connect the I_{ON} decoupling capacitor close to the I_{ON} pins.
- Flood all unused areas on all layers with copper. Flooding will reduce the temperature rise of the power components. You can connect the copper area to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

APPLICATIONS INFORMATION

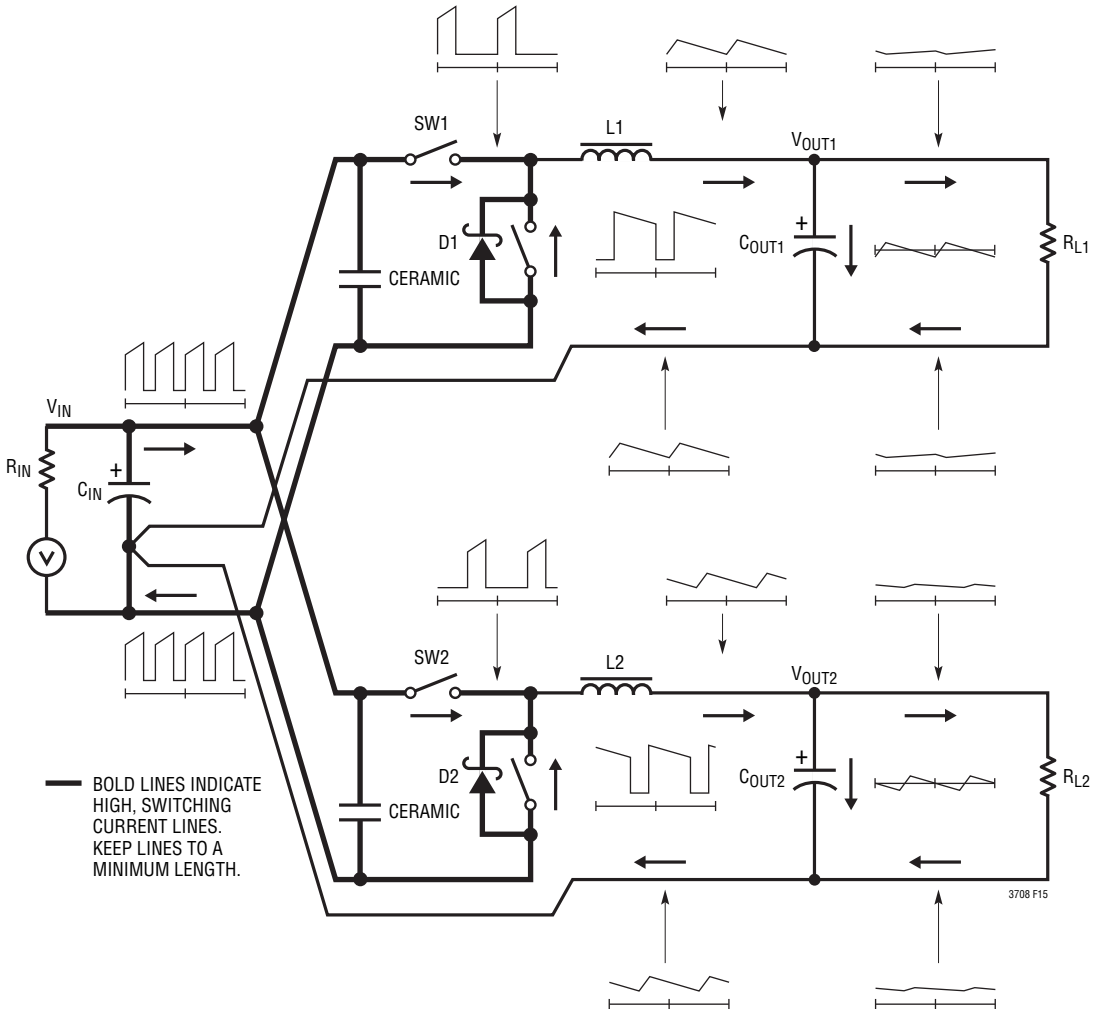
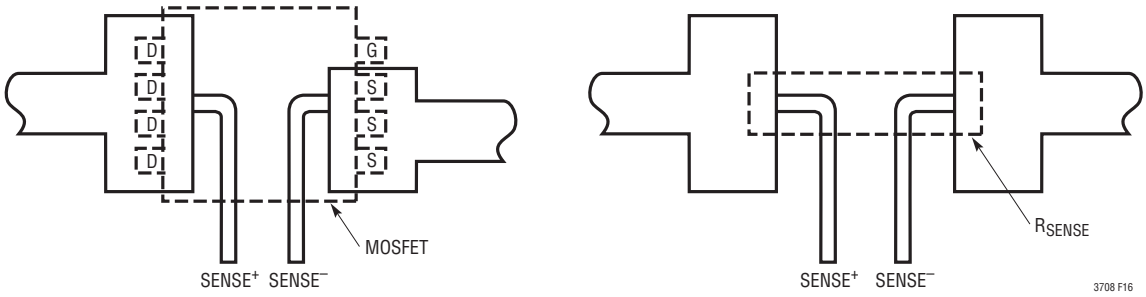


Figure 15. Branch Current Waveforms

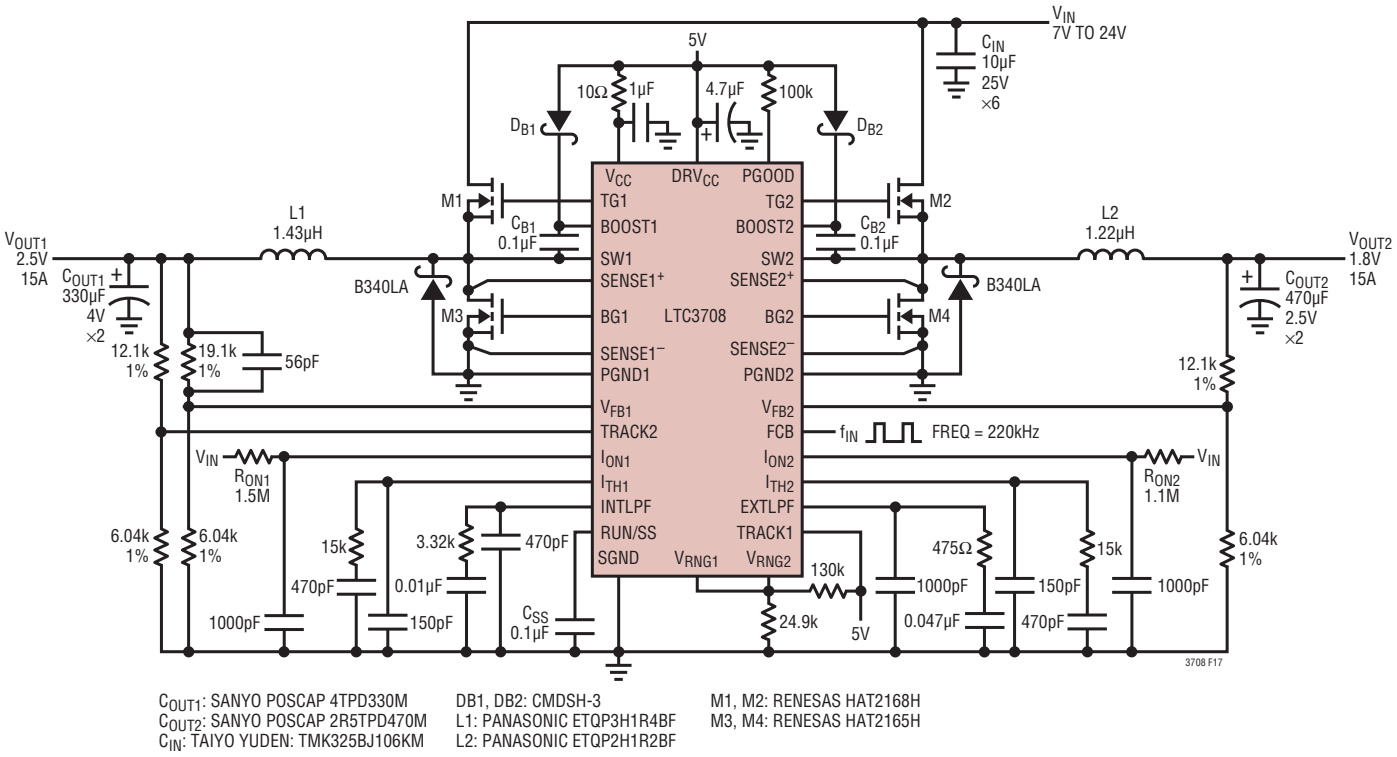


(16a) Sensing the Bottom MOSFET

(16b) Sensing a Resistor

Figure 16. Kelvin Sensing

APPLICATIONS INFORMATION



COUT1: SANYO POSCAP 4TPD330M
COUT2: SANYO POSCAP 2R5TPD470M
CIN: TAIYO YUDEN: TMK325BJ106KM

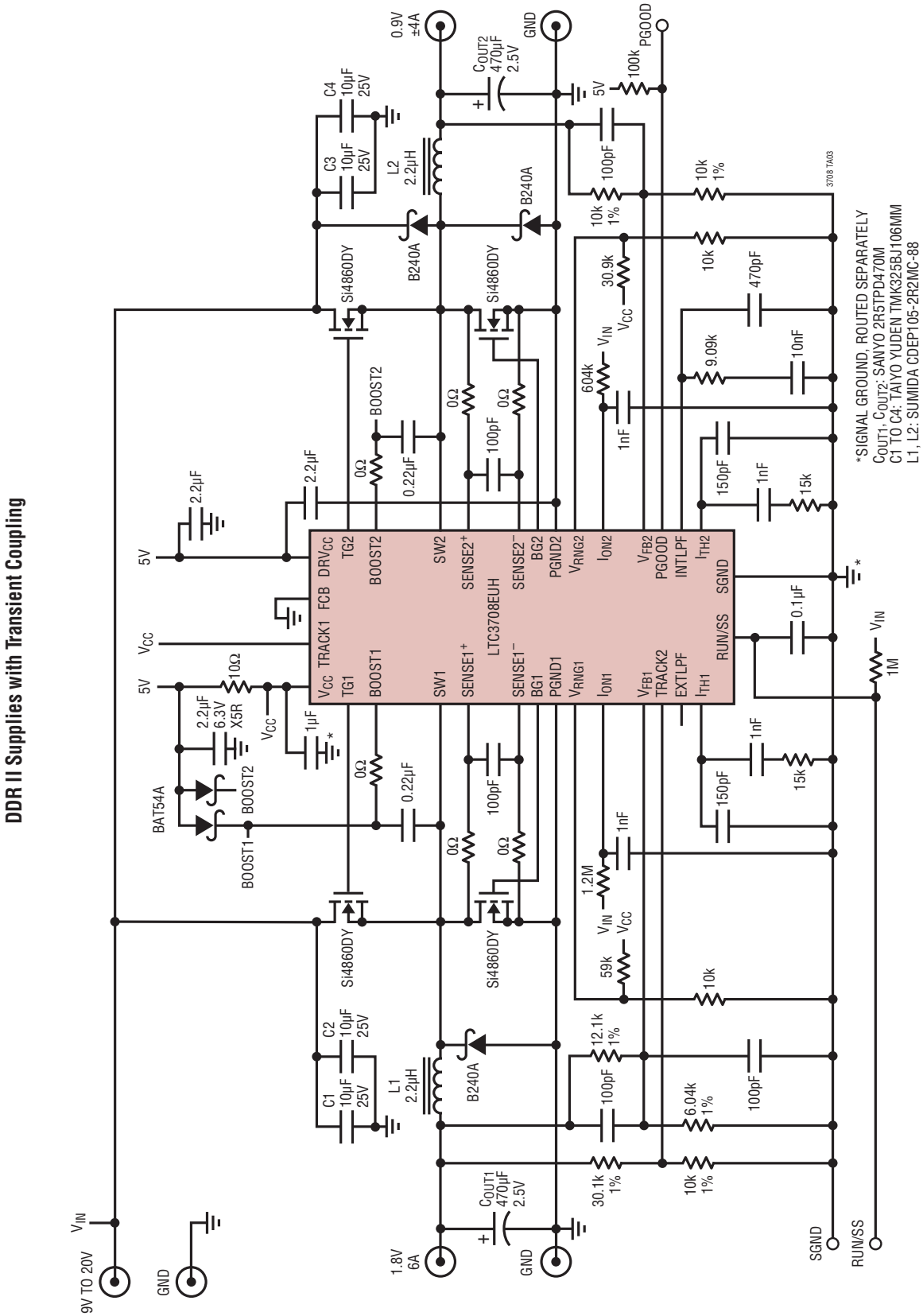
DB1, DB2: CMDSH-3
L1: PANASONIC ETQP3H1R4BF
L2: PANASONIC ETQP2H1R2BF

M1, M2: RENESAS HAT2168H
M3, M4: RENESAS HAT2165H

Figure 17. High Efficiency, Dual Output Power Supply with External Frequency Synchronization

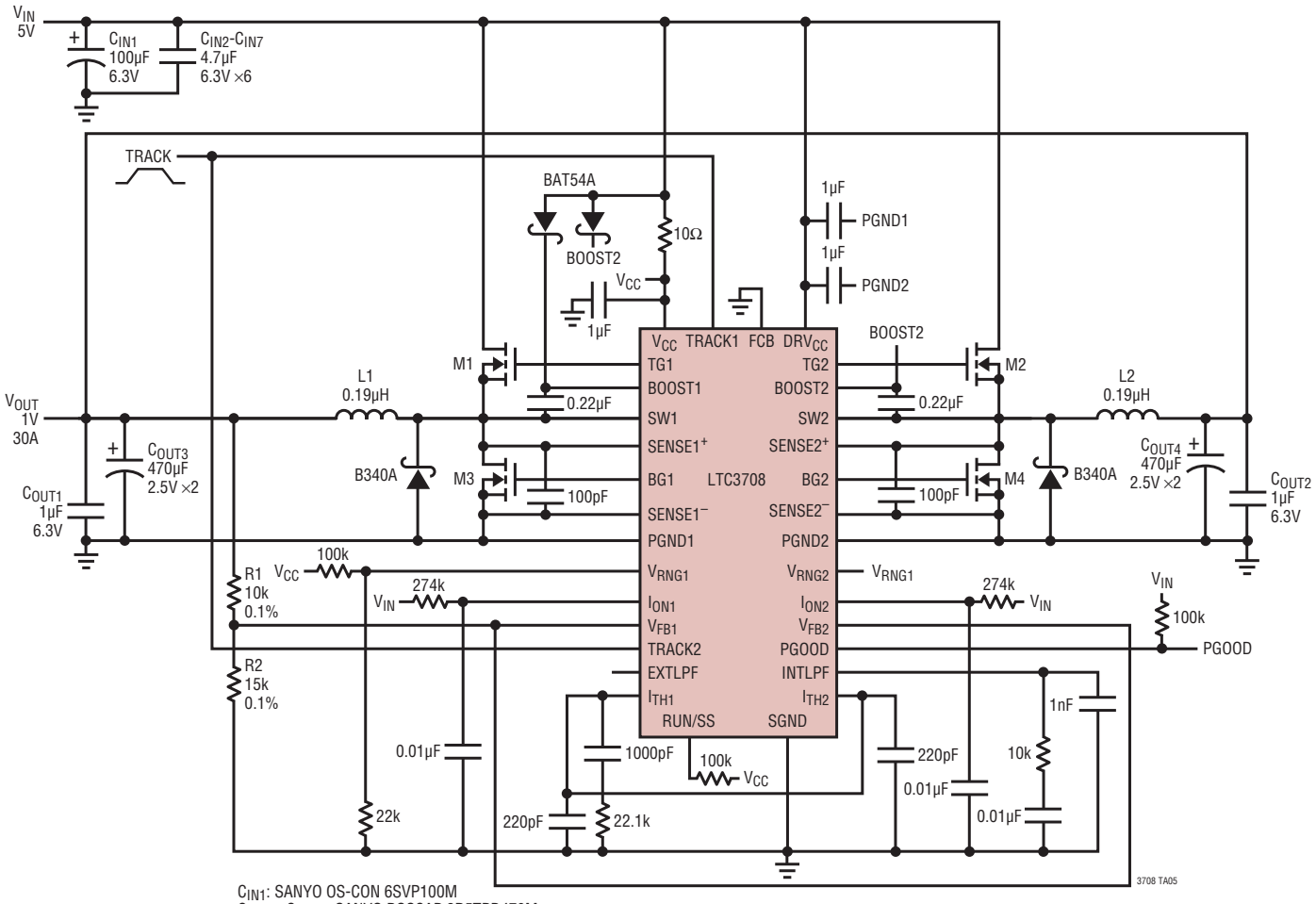
TYPICAL APPLICATIONS

DDR II Supplies with Transient Coupling



TYPICAL APPLICATIONS

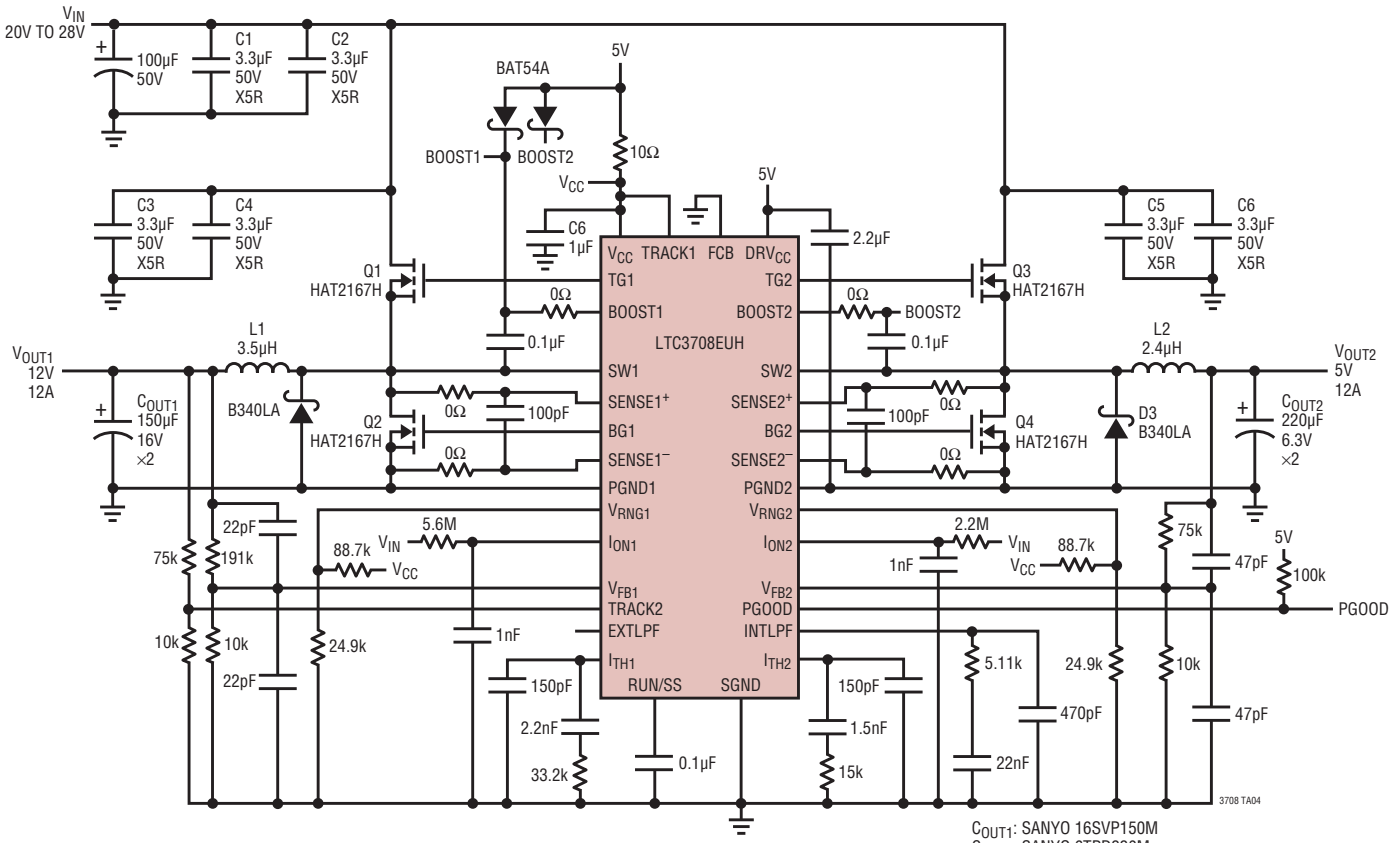
Dual-Phase, 30A Power Supply with 10mV Output Ripple



CIN1: SANYO OS-CON 6SVP100M
COUT3, COUT4: SANYO POSCAP 2R5TPD470M
L1, L2: PANASONIC ETQP4LR19
M1 TO M4: RENESAS HAT2165

TYPICAL APPLICATIONS

12V/12A and 5V/12A at 300kHz Application

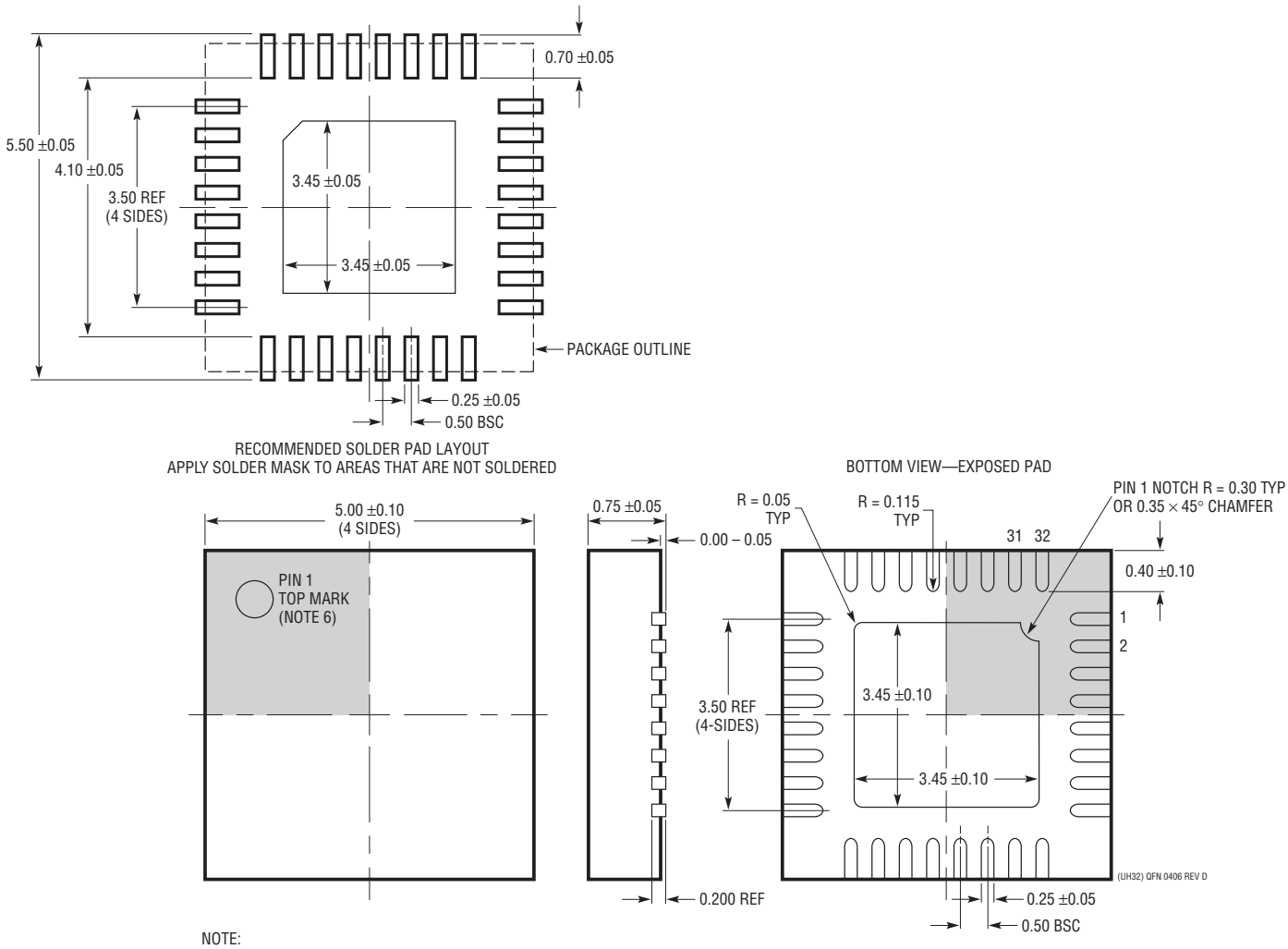


C_{OUT1}: SANYO 16SVP150M
C_{OUT2}: SANYO 6TPD220M
C1 TO C6: TDK C4532X5R1H335M
L1: SUMIDA CDEP147-3R5MC-H
L2: SUMIDA CDEP147-2R4MC

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3708#packaging for the most recent package drawings.

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



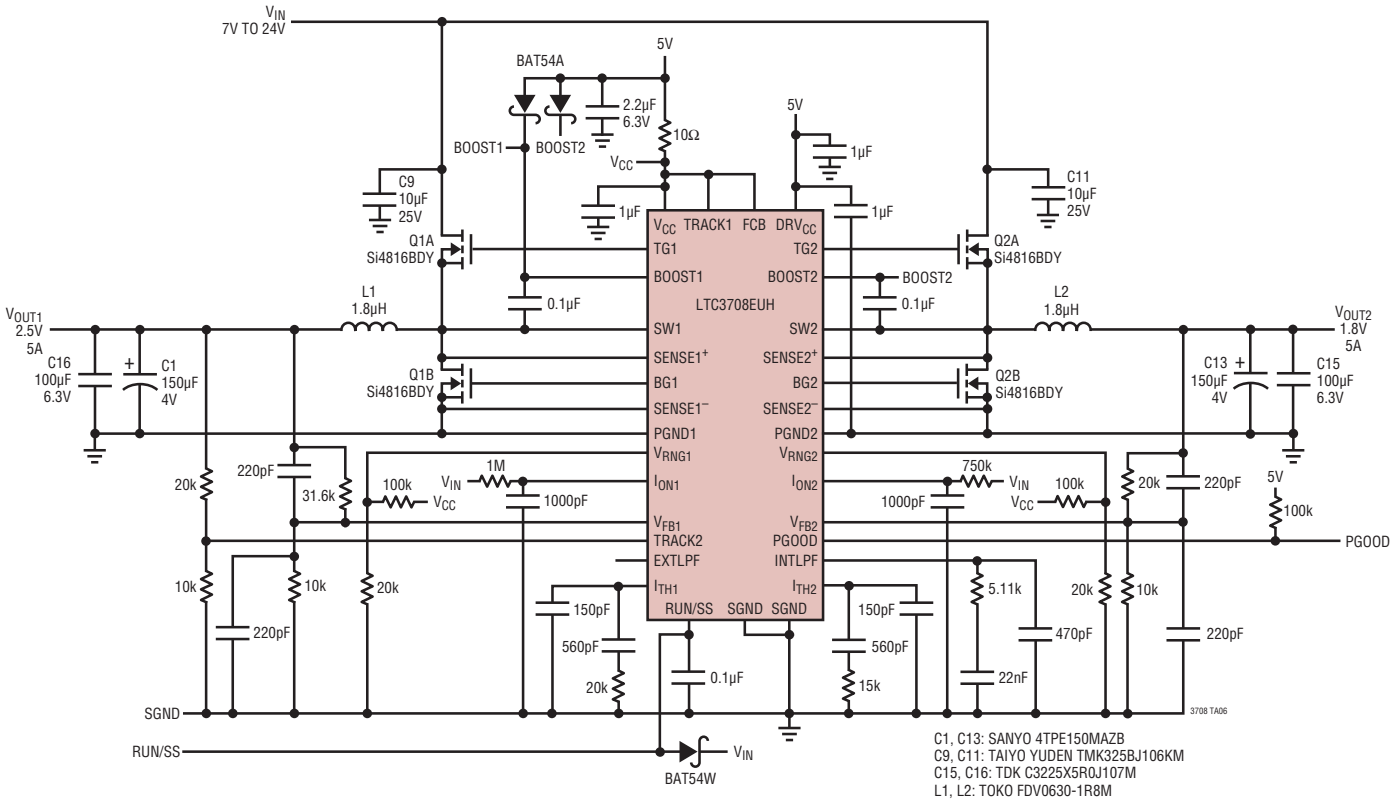
NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	09/16	Minor typographical changes.	3, 4, 25, 27, 30

TYPICAL APPLICATION

Area = 650mm^2, Height = 3mm



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1778	Wide Operating Range, No R_{SENSE} Step-Down Controller	Single Channel, GN16 Package
LTC3709	2-Phase, No R_{SENSE} Step-Down Controller with Tracking/Sequencing	Single Output, Remote Sensing
LTC3728	Dual, 550kHz, 2-Phase Synchronous Step-Down Switching Regulator	Fixed Frequency, Dual Output
LTC3729	550kHz, PolyPhase®, High Efficiency, Synchronous Step-Down Switching Regulator	Fixed Frequency, Single Output, Up to 12-Phase Operation
LTC3731	3-Phase, 600kHz, Synchronous Buck Switching Regulator Controller	3-Phase, Single Output
LTC3778	Wide Operating Range, No R_{SENSE} Step-Down Controller	Single Channel, Separate V_{ON} Programming

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