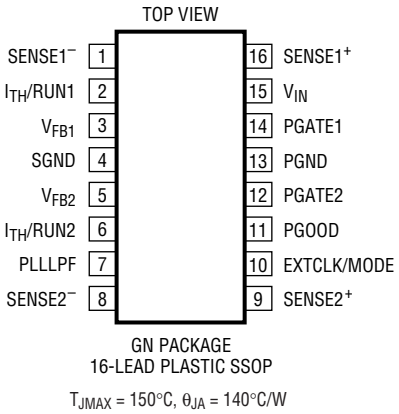
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 10V
SENSE1$^-$, SENSE2$^-$, PGATE1, PGATE2,
PLLLPF, SENSE1$^+$, SENSE2$^+$,
EXTCLK/MODE Voltages ..... –0.3V to (V_{IN} + 0.3V)
V_{FB1}, V_{FB2}, I_{TH}/RUN1,
I_{TH}/RUN2 Voltages ..... –0.3V to 2.4V
PGOOD Voltage ..... –0.3V to 10V
PGATE1, PGATE2 Peak Output Current (<10µs) 1A
Operating Ambient Temperature Range
(Note 2) .....–40°C to 85°C
Storage Ambient Temperature Range ... –65°C to 150°C
Junction Temperature (Note 3) ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC3701EGN
GN PART MARKING
3701

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 4.2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current	(Note 4)					
Normal Operation	2.5V < V_{IN} < 9.8V			460	780	µA
Sleep Mode	2.5V < V_{IN} < 9.8V			305	470	µA
Shutdown	2.5V < V_{IN} < 9.8V, I_{TH}/RUN1 = I_{TH}/RUN2 = 0V			9	28	µA
UVLO	V_{IN} < UVLO Threshold			18	30	µA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.55	2.00	2.50	V
	V_{IN} Rising	●	1.70	2.12	2.55	V
Shutdown Threshold at I_{TH}/RUN1, 2			0.2	0.35	0.5	V
Start-Up Current Source on I_{TH}/RUN1, 2	V_{ITH}/RUN1, 2 = 0V		0.25	0.5	0.85	µA
Regulated Feedback Voltage	0°C to 70°C (Note 5), I_{TH}/RUN = 1.3V	●	0.784	0.8	0.816	V
	–40°C to 85°C (Note 5)	●	0.774	0.8	0.826	V
Output Voltage Line Regulation	2.5V < V_{IN} < 9.8V (Note 5)			0.05	0.20	mV/V
Output Voltage Load Regulation	I_{TH}/RUN = 0.9V (Note 5)			0.2	0.8	%
	I_{TH}/RUN = 1.6V			–0.2	–0.8	%
$V_{FB1, 2}$ Input Current	(Note 5)			10	50	nA
Output Overvoltage Protect Threshold	Measured at V_{FB}		0.835	0.88	0.930	V
Output Overvoltage Protect Hysteresis				20		mV
Gate Drive 1, 2 Rise Time	C_L = 3000pF			40		ns
Gate Drive 1, 2 Fall Time	C_L = 3000pF			40		ns
Maximum Current Sense Voltage (SENSE$^+$ – SENSE$^-$)	(Note 6)		95	120	145	mV
Soft-Start						
Current Sense Voltage Step				30		mV
Time to Maximum Sense Voltage				2048		Cycles

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 4.2V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop					
Oscillator Frequency	V_{PLLLPF} = 1.2V or Floating	500	550	600	kHz
	V_{PLLLPF} = 0V	230	280	320	kHz
	V_{PLLLPF} ≥ 2.4V	690	775	890	kHz
Phase Detector Output Current					
Sinking	$f_{EXTCLK/MODE} < f_{OSC}$		–5		µA
Sourcing	$f_{EXTCLK/MODE} > f_{OSC}$		5		µA
PGOOD Output					
PGOOD Voltage Low	I_{PGOOD} = 500µA		70	150	mV
PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage				
	V_{FB} Ramping Positive	–15	–8	–2.5	%
	V_{FB} Ramping Negative	2.5	8	15	%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3701E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: TJ is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

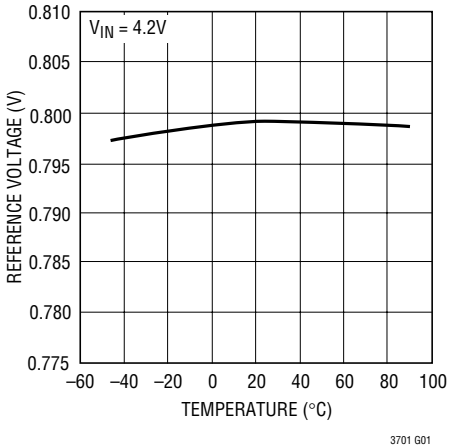
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3701 is tested in a feedback loop that servos $I_{TH/RUN}$ to a specified voltage and measures the resultant V_{FB} voltage.

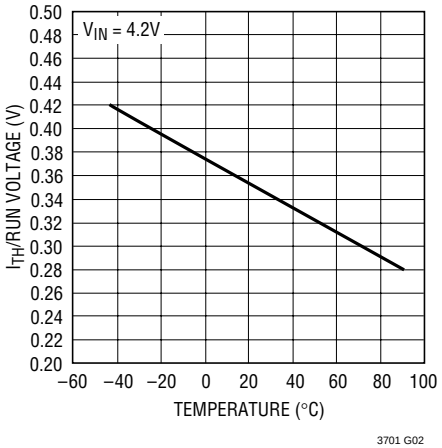
Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as given in Figure 2.

TYPICAL PERFORMANCE CHARACTERISTICS

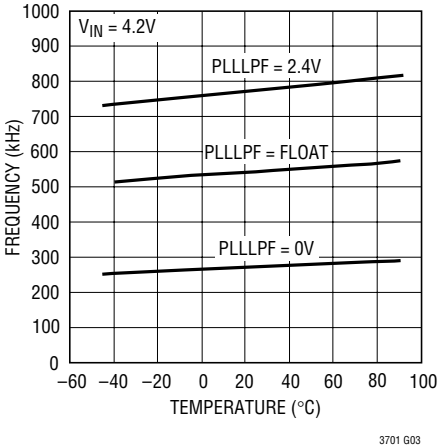
Reference Voltage vs Temperature



Shutdown Threshold vs Temperature

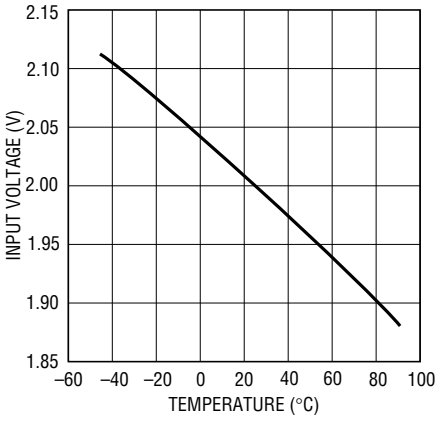


Oscillator Frequency vs Temperature

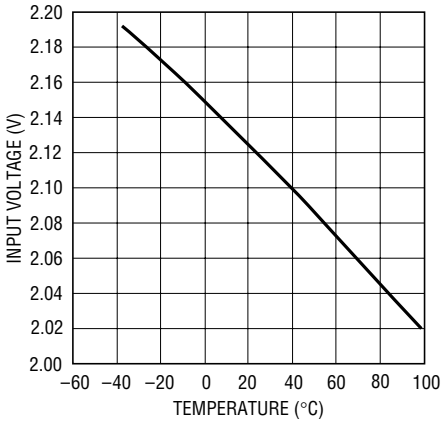


TYPICAL PERFORMANCE CHARACTERISTICS

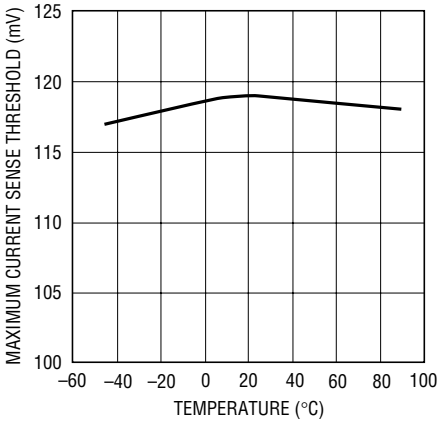
Undervoltage Lockout Trip Voltage (Falling) vs Temperature



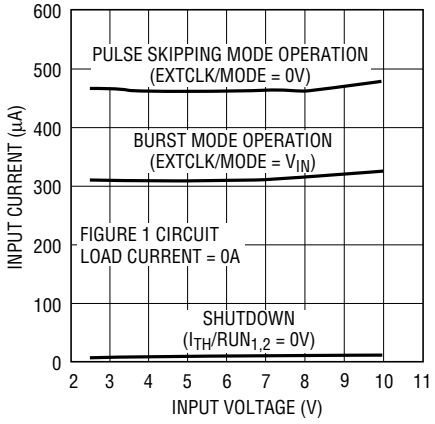
Undervoltage Lockout Trip Voltage (Rising) vs Temperature



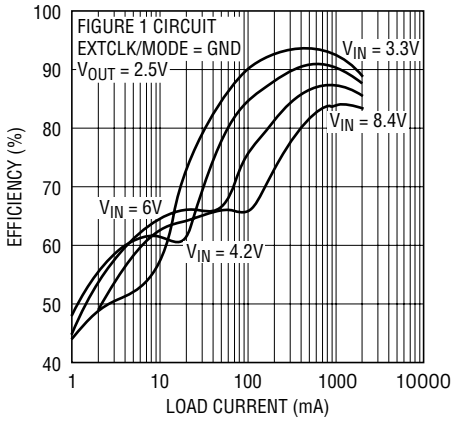
Maximum Current Sense Threshold vs Temperature



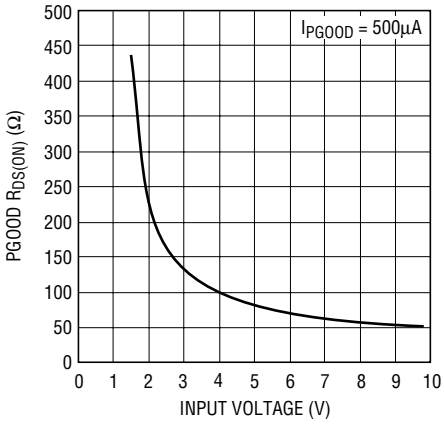
Input and Shutdown Currents vs Input Voltage



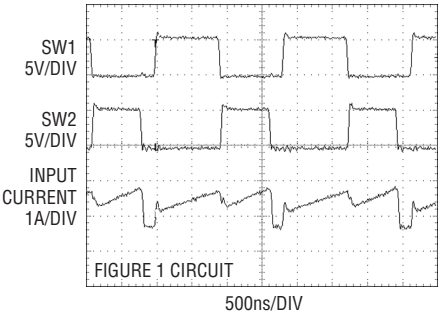
Efficiency vs Load Current (Pulse Skipping Mode)



PGOOD R_{ON} vs Input Voltage



2-Phase Operation



PIN FUNCTIONS

SENSE1$^-$, SENSE2$^-$ (Pins 1, 8): The (–) Inputs to the Differential Current Comparators.

I_{TH}/RUN1, I_{TH}/RUN2 (Pins 2, 6): These pins each serve two functions. Each pin serves as the error amplifier compensation point as well as the run control input for the respective controller. Forcing one pin below 0.35V causes the functions associated with that controller to be shut down. Forcing both $I_{TH/RUN}$ pins below 0.35V causes the device to be shut down. Nominal operating voltage range on these pins is from 0.7V to 1.9V.

V_{FB1}, V_{FB2} (Pins 3, 5): Each receives the remotely sensed feedback voltage for each controller from an external resistive divider across the output.

SGND (Pin 4): Signal Ground.

PLLLPF (Pin 7): Serves as the lowpass filter point for the PLL and as the voltage control input to the internal oscillator. Normally, a series RC is connected between this pin and ground when synchronizing to an external clock. Nominal voltage range is from 0V to 2.4V. Frequency can be set by forcing this pin with a voltage. Tying this pin to GND selects 300kHz. Tying to V_{IN} or a voltage ≥ 2.4V selects 750kHz. Floating this pin selects 550kHz operation.

SENSE2$^+$ (PV_{IN2}), SENSE1$^+$ (PV_{IN1}) (Pins 9, 16): The (+) Inputs to the Differential Current Comparators. These pins also power the gate drivers.

EXTCLK/MODE (Pin 10): External Clock Input. Applying a clock to this pin causes the internal oscillator to phase-lock to the external clock (nominal lock frequency range between 300kHz and 750kHz). This also disables Burst Mode operation but allows pulse-skipping at low load currents.

Forcing this pin high enables Burst Mode operation. Forcing this pin low enables pulse-skipping mode. In these cases, the frequency of the internal oscillator is set by the voltage on the PLLLPF pin. If the PLLLPF voltage is not set externally, the frequency internally defaults to 550kHz.

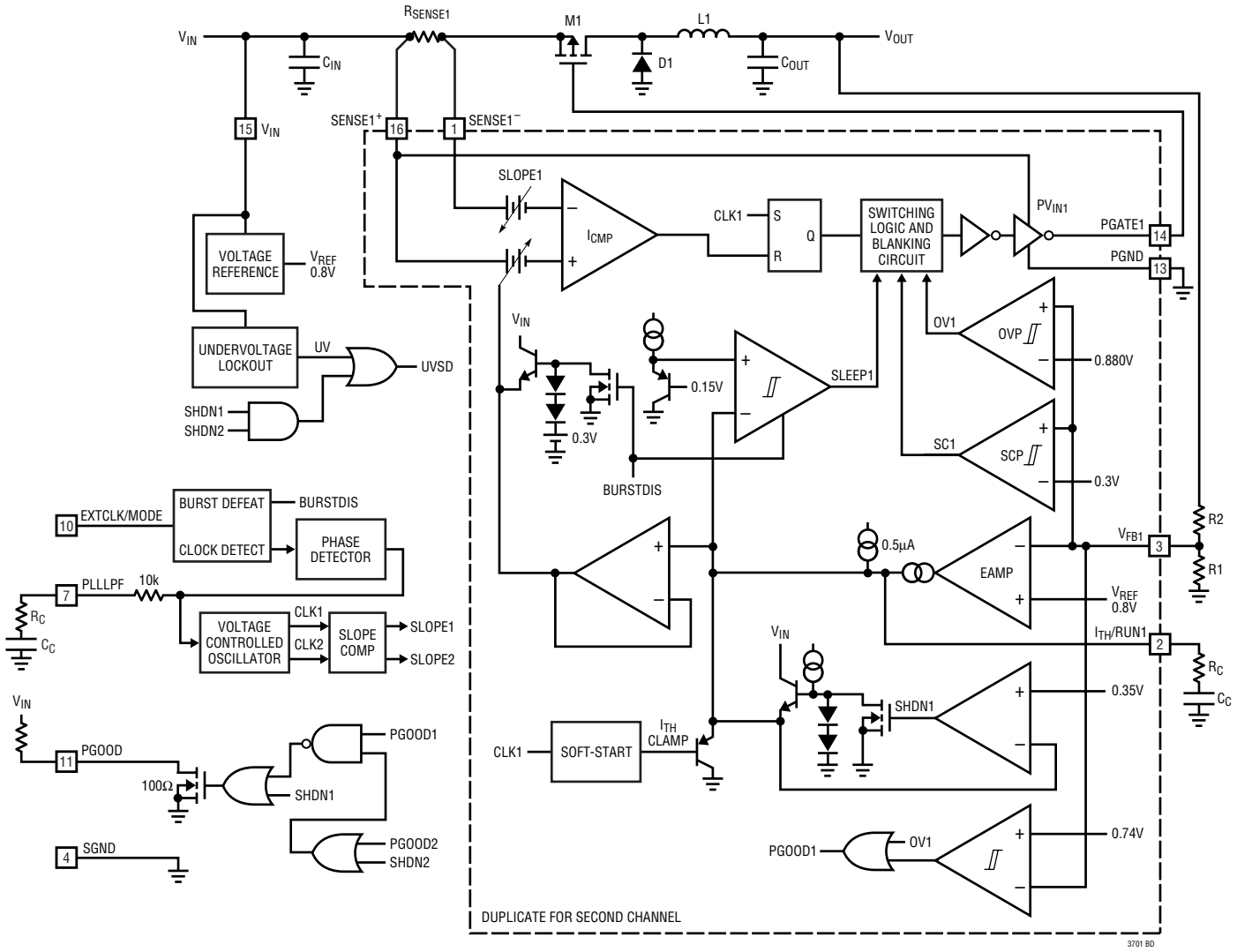
PGOOD (Pin 11): Power Good Output Voltage Monitor Open-Drain Logic Output. This pin is pulled to ground when the voltage on either feedback pin (V_{FB1}, V_{FB2}) is not within ±8% of its nominal set point. PGOOD is pulled low when channel 1 or both channels are shut down. When channel 2 is shut down and channel 1 enabled, the PGOOD output indicates the state of V_{FB1} only.

PGATE2, PGATE1 (Pins 12, 14): Gate Drivers for the External P-Channel MOSFETs. These pins swing from 0 to SENSE$^+$ (PV_{IN}).

PGND (Pin 13): Ground Pin for Gate Drivers.

V_{IN} (Pin 15): Chip Signal Power Supply Input. This pin powers the entire chip except for the gate drivers.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3701 uses a constant frequency, current mode architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each external P-channel power MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the current comparator (I_{CMP}) resets the latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of each error amplifier, EAMP. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn, causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

Each main control loop is shut down by pulling the respective I_{TH}/RUN pin low. When both I_{TH}/RUN1 and I_{TH}/RUN2 are low, all LTC3701 controller functions are shut down. Releasing I_{TH}/RUN allows an internal 0.5µA current source to charge up the external compensation network. When the I_{TH}/RUN pin reaches 0.35V, the main control loop is enabled with the I_{TH}/RUN voltage then pulled up to its zero current level of approximately 0.7V. After the loop is enabled, an internal soft-start begins. During this soft-start time of 2048 clock cycles, the I_{TH}/RUN voltage is clamped such that the maximum peak current sense voltage ($V_{SENSE}^+ - V_{SENSE}^-$) is held to approximately 0%, 25%, 50% and 75%, respectively, of its maximum value of 120mV for four equally timed intervals. After soft-start is completed, full current operation is allowed. As the external compensation network continues to charge, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient output voltage overshoots greater than 10% by turning off the external P-channel power MOSFET and keeping it off until the fault is removed.

Burst Mode Operation

The LTC3701 can be enabled to enter Burst Mode operation at low load currents by tying the EXTCLK/MODE pin to V_{IN} or to a voltage of at least 2V. To disable Burst Mode operation and enable PWM pulse skipping mode, connect the EXTCLK/MODE pin to ground. In this mode, the efficiency is lower at light loads. However, pulse skipping mode has the advantages of lower output ripple and less interference to audio circuitry.

When a controller is in Burst Mode operation, the peak current of the inductor is set as if V_{ITH}/RUN = 1V, even though the voltage at the I_{TH}/RUN pin is at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH}/RUN pin will drop. When the I_{TH}/RUN voltage goes below 0.85V, the sleep signal goes high, turning off the external MOSFET. The sleep signal goes low when the I_{TH}/RUN voltage goes above 0.925V and that controller channel resumes normal operation. The next oscillator cycle will turn the external MOSFET on and the switching cycle repeats.

Frequency Synchronization

A phase-locked loop (PLL) is available on the LTC3701 to allow the internal oscillator to be synchronized to an external clock source connected to the EXTCLK/MODE pin. The output of the phase detector at the PLLLPF pin operates over a 0V to 2.4V range corresponding to approximately 300kHz to 750kHz. When locked, the PLL aligns the turn-on of the external MOSFET of controller channel 1 to the rising edge of the synchronizing signal. The turn-on of the external MOSFET of controller channel 2 is 180 degrees out of phase with the rising edge of the external clock source.

When the LTC3701 is clocked by an external source, Burst Mode operation is disabled and the LTC3701 operates in PWM pulse skipping mode. In this mode, when the output load is very low, the current comparator I_{CMP} may remain tripped for several cycles and force the external MOSFET to stay off for the same number of cycles. Increasing the output load slightly allows constant frequency PWM operation to resume. This mode exhibits low output ripple as well as low audio noise and reduced RF interference while providing reasonable low current efficiency.

OPERATION (Refer to Functional Diagram)

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of the inductor current during the ON cycle decreases. This reduction means that the external P-channel MOSFET will remain on for more than one oscillator cycle if the inductor current has not ramped up to the threshold set by EAMP on the I_{TH}/RUN pin. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the LTC3701. When the input supply voltage drops below 2V, the P-channel MOSFET and all circuitry are turned off except the undervoltage block, which draws only several microamperes.

Short-Circuit Protection

When an output is shorted to ground (V_{FB} < 0.3V), the switching frequency of that channel is reduced to 1/5 of the normal operating frequency. The other controller channel is unaffected and maintains normal operation. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The switching frequency will return to its normal value when the feedback voltage rises above 0.3V. During the first 64 cycles (nonzero-current cycles) of soft-start, however, the controller operates at its full frequency.

Output Overvoltage Protection

As a further protection, the overvoltage comparator in the LTC3701 will turn the external MOSFET off when the feedback voltage has risen 10% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

Slope Compensation and Peak Inductor Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH/RUN} - 0.7V}{10 \bullet R_{SENSE}}$$

when the LTC3701 is operating below 20% duty cycle. However, once the duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curve in Figure 2.

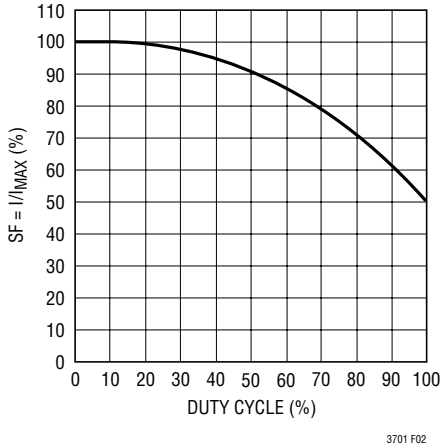


Figure 2. Maximum Peak Current vs Duty Cycle

Power Good (PGOOD) Pin

A window comparator monitors both output voltages and the open-drain PGOOD output is pulled low when the divided down output voltages are not within ±8% of the reference voltage of 0.8V. PGOOD is pulled low when channel 1 or both channels are shut down. When channel 2 is shut down and channel 1 enabled, the PGOOD output indicates the state of channel 1 only.

2-Phase Operation

The LTC3701 dual switching controller offers the considerable benefits of using 2-phase operation. Circuit benefits include lower input filtering requirements, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

OPERATION (Refer to Functional Diagram)

Why the need for 2-phase operation? Until recently, constant frequency dual switching regulators operated both channels in phase (i.e., single phase operation). This means that both topside MOSFETs are turned on at the same time, causing current pulses of up to twice the amplitude of those from a single regulator to be drawn from the input capacitor. These large amplitude pulses increase the total RMS current flowing into the input capacitor, requiring the use of more expensive input capacitors, and increasing both EMI and losses in the input capacitor and input power supply.

With 2-phase operation, the two channels of the LTC3701 are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in the total RMS input current, which in turn allows for use of less expensive input capacitors, reduces shielding requirements for EMI and improves real world operating efficiency.

Figure 3 shows example waveforms for a single switching regulator channel versus a 2-phase LTC3701 system with both channels switching. A single phase dual regulator system with both sides switching would exhibit twice the single side numbers. In this example, 2-phase operation reduced the RMS input current from $1.79A_{RMS}$ to $0.91A_{RMS}$. While this is an impressive reduction in itself, remember that power losses are proportional to I_{RMS}^2, meaning that actual power wasted is reduced by a factor of 3.86. The reduced input ripple current also means that less power is lost in the input power path, which could include batteries, switches, trace/connector resistances, and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles, which in turn are dependent upon the input voltage V_{IN}. Figure 4 shows how the RMS input current varies for 1-phase and 2-phase operation for 2.5V and 1.8V regulators over a wide input voltage range.

It can be readily seen that the advantages of 2-phase operation are not limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

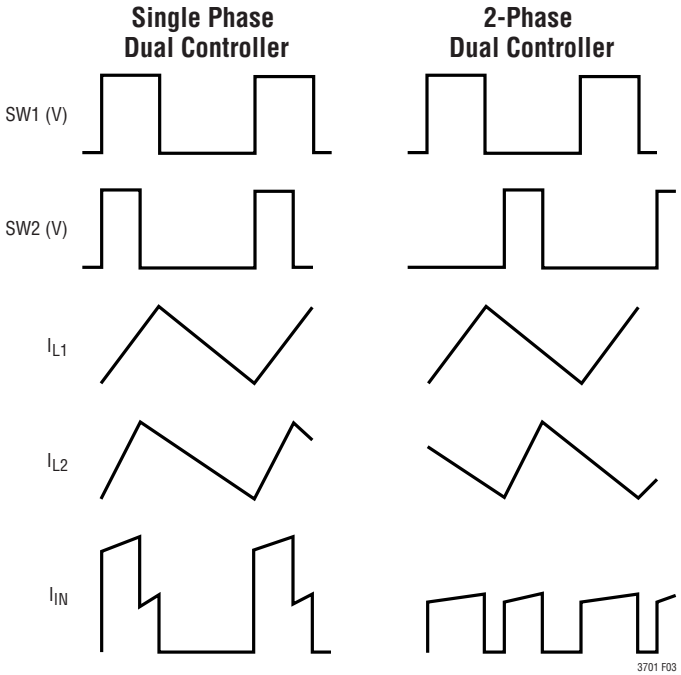


Figure 3. Example Waveforms for a Single Switching Regulator Channel vs 2-Phase LTC3701 System with Both Channels Switching

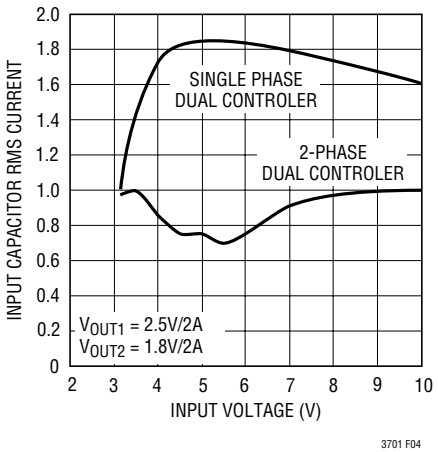


Figure 4. RMS Input Current Comparison

APPLICATIONS INFORMATION

The basic LTC3701 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L and R_{SENSE}. Next, the power MOSFET M1 and the output diode D1 are selected. Finally C_{IN} (C1) and C_{OUT} (C2) are chosen.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. Since the current comparator monitors the voltage developed across R_{SENSE}, the threshold of the comparator determines the inductor's peak current. The output current that the LTC3701 can provide is given by:

$$I_{OUT} = \frac{0.095}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation).

A reasonable starting point for setting ripple current is $I_{RIPPLE} = (0.4)(I_{OUT})$. Rearranging the above equation yields:

$$R_{SENSE} = \frac{1}{12.7 \bullet I_{OUT}} \text{ for Duty Cycle} < 20\%$$

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of R_{SENSE} to provide the required amount of current. Using Figure 2, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(12.7)(I_{OUT})(100)}$$

For noise sensitive applications, a 1nF capacitor placed between the $SENSE^+$ and $SENSE^-$ pins very close to the chip is suggested.

Inductor Value Calculation

The inductor selection will depend on the operating frequency of the LTC3701. The internal nominal frequency is 550kHz, but can be externally synchronized or set from approximately 300kHz to 750kHz.

The operating frequency and inductor selection are interrelated in that higher frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge and switching losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE}, decreases with higher inductance or frequency. The inductor's peak-to-peak ripple current is:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f \bullet L}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where f is the operating frequency and V_D is the forward voltage drop of the external Schottky diode. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. The maximum I_{RIPPLE} occurs at the maximum input voltage.

With Burst Mode operation selected on the LTC3701, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \leq (0.03)/R_{SENSE}$$

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f\left(\frac{0.03}{R_{SENSE}}\right)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

$$\left(\text{Use } V_{IN} = V_{IN(MAX)}\right)$$

A smaller value than L_{MIN} could be used in the circuit, however, the inductor current will not be continuous during burst periods.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. Actual core loss is independent of core

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when several layers of wire can be used, while inductors wound on bobbins are generally easier to surface mount. However, new designs for surface mount that do not increase the height significantly are available from Coiltronics, Coilcraft, Dale and Sumida.

Power MOSFET Selection

An external P-channel MOSFET must be selected for use with each channel of the LTC3701. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$, "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and the total gate charge.

Since the LTC3701 is designed for operation down to low input voltages, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC3701 is less than the absolute maximum MOSFET V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC3701 in dropout, i.e., 100% duty cycle, the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)DC=100\%} = \frac{P_P}{\left(I_{OUT(MAX)}\right)^2(1+\delta p)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. (1 + δp) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δp = 0.005/°C can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC3701 is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC)I_{OUT}{}^2(1+\delta p)}$$

where DC is the maximum operating duty cycle for that channel of the LTC3701.

Output Diode Selection

The catch diode carries load current during the switch off-time. The average diode current is therefore dependent on the P-channel MOSFET duty cycle. At high input voltages, the diode conducts most of the time. As V_{IN} approaches V_{OUT}, the diode conducts for only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition, the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode's ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{PEAK}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

A Schottky diode is a good choice for low forward drop and fast switching time. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

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C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}+V_D}\left[(V_{OUT}+V_D)(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT} + V_D$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3701, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3701 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the P-channel MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3701, is also suggested. A 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Low Supply Operation

Although the LTC3701 can function down to approximately 2V, the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 5 shows the amount of change as the supply is reduced down to 2V. Also shown is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

Setting Output Voltage

The LTC3701 output voltages are each set by an external feedback resistive divider carefully placed across the output capacitor (see Figure 6). The resultant feedback signal is compared with an internal 0.8V reference by the

APPLICATIONS INFORMATION

error amplifier. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 close to the LTC3701.

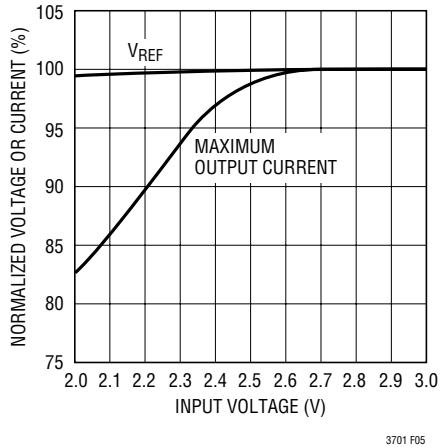


Figure 5. Line Regulation of V_{REF} and Maximum Output Current

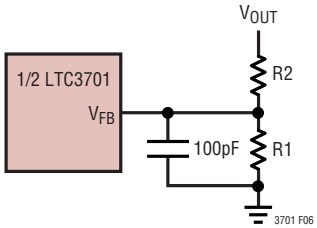


Figure 6. Setting Output Voltage

Phase-Locked Loop and Frequency Synchronization

The LTC3701 has a phase-locked loop comprised of an internal voltage-controlled oscillator and phase detector. This allows the turn-on of the external P-channel MOSFET of controller 1 to be locked to the rising edge of an external frequency source. The turn-on of controller 2's external P-channel MOSFET is thus 180 degrees out of phase to the external clock. The nominal frequency range of the voltage-controlled oscillator is 280kHz to 775kHz. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external oscillator.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency is shown in Figure 7 and specified in the electrical characteristics table. Note that the LTC3701 can only be synchronized to an external clock whose frequency is within the frequency range of the LTC3701's internal oscillator, which is specified in the electrical characteristics table. A simplified block diagram of the PLL is shown in Figure 8.

If the external frequency ($V_{EXTCLK/MODE}$) is greater than the internal oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLLPF pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the external oscillators are identical. At the stable operating point, the phase comparator output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components R_{LP} and C_{LP} determine how fast the loop acquires lock. Typically, R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF. When not synchronized to an external clock, the

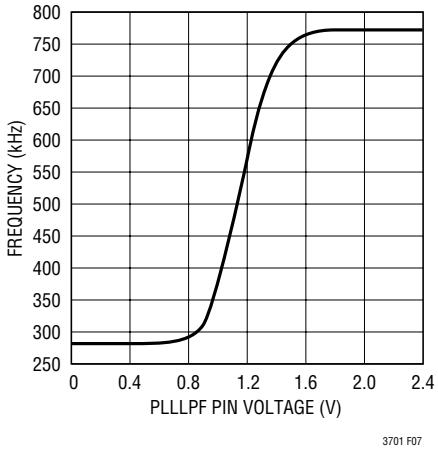


Figure 7. Relationship Between Oscillator Frequency and Voltage at PLLLPF Pin

APPLICATIONS INFORMATION

internal oscillator frequency may be set by applying a DC voltage to the PLLLPF pin. 550kHz operation can be selected by floating the PLLLPF pin. The PLLLPF pin may be connected to voltages as high as V_{IN}.

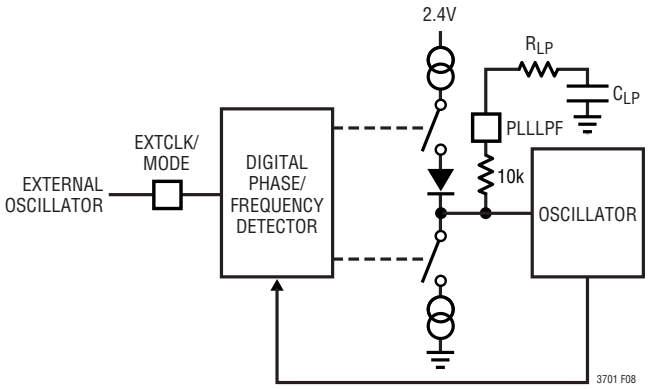


Figure 8. Phase-Locked Loop Block Diagram

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3701 circuits: 1) LTC3701 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, 4) voltage drop of the output diode and 5) transition losses.

1) The V_{IN} (pin) current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN}.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from PV_{IN} to ground. The resulting dQ/dt is a current out of PV_{IN}, which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f \bullet Q_P$.

3) I^2R losses are calculated from the DC resistances of the MOSFET, inductor and sense resistor. In continuous mode, the average output current flows through L but is "chopped" between the P-channel MOSFET in series with R_{SENSE} and the output diode. The MOSFET $R_{DS(ON)}$ plus R_{SENSE} multiplied by duty cycle can be summed with the resistance of L to obtain I^2R losses.

4) The output diode is a major source of power loss at high currents and is worse at high input voltages. The diode loss is calculated by multiplying the forward voltage times the load current times the diode duty cycle.

5) Transition losses apply to the external MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

Transition Loss = 2 $(V_{IN})^2 I_{O(MAX)} C_{RSS}(f)$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Foldback Current Limiting

As described in the Output Diode Selection, the worst-case diode dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously. To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 9. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

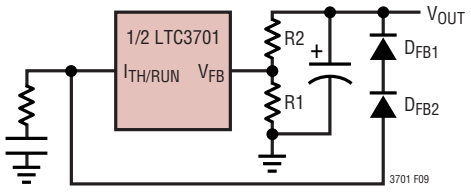


Figure 9. Foldback Current Limiting

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C, and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3701 is capable of turning the top MOSFET on and then off. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC3701 is about 250ns. Low duty cycle and high frequency applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3701 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3701. These items are illustrated graphically in the layout diagram of Figure 10. Figure 11 illustrates the current waveforms present in the various branches of the 2-phase regulators. Check the following in your layout:

1) Are the sense resistors and P-channel MOSFETs for the two channels located within 1cm of each other with a common connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

APPLICATIONS INFORMATION

2) Are the signal and power grounds kept separate? The LTC3701 signal ground consists of the feedback resistor divider, the I_{TH}/RUN compensation network, and Pin 4. The power ground consists of the (–) terminal of C_{IN}, the (–) terminals of $C_{OUT1,2}$, the anodes of the Schottky diodes, and Pin 13 of the LTC3701. The power ground traces should be kept short, direct, and wide. Connect the anode of the Schottky diodes directly to the input capacitor ground.

3) Do the V_{FB} pins connect directly to the feedback resistors? Put the feedback resistors close to the V_{FB} pins. The traces connecting the top feedback resistors to the corresponding output capacitor should to be Kelvin traces.

4) Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The (optional) filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.

5) Keep the switching nodes (SW1, SW2) and top gate nodes (PGATE1, PGATE2) away from small-signal nodes, especially the opposite channel's voltage and current sensing feedback pins. All of these nodes have large and fast moving signals and therefore should be keep on the "output side" of the LTC3701 and occupy minimum PC trace area.

Design Example

As a design example for one channel, assume V_{IN} will be operating from a maximum of 4.2V down to a minimum of 2.7V. Load current requirement is a maximum of 1.5A , but most of the time it will be in a standby mode requiring only 2mA. Efficiency at both low and high load currents is important. Burst Mode operation at light loads is desired. Output voltage is 2.5V.

$$\text{Maximum Duty Cycle} = \left(\frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_D}\right) = 93\%$$

From Figure 2, SF = 57%.

$$R_{SENSE} = \frac{SF}{12.7 \bullet I_{OUT} \bullet 100} = \frac{0.57}{12.7 \bullet 1.5} = 0.03\Omega$$

In the application, a 0.03Ω resistor is used. The PLLLPF pin will be left floating, so the LTC3701 will operate at its default frequency of 550kHz. For continuous operation in Burst Mode, the required minimum inductor value is:

$$L_{MIN} = \frac{4.2V - 2.5V}{550kHz\left(\frac{0.03V}{0.03\Omega}\right)}\left(\frac{2.5V + 0.3V}{4.2V + 0.3V}\right) = 2.00\mu H$$

For the selection of the external MOSFET, the $R_{DS(ON)}$ must be guaranteed at 2.5V since the LTC3701 has to work down to 2.7V. Let's assume that the MOSFET dissipation is to be limited to P_P = 250mW and its thermal resistance is 50°C/W. Hence, the junction temperature at T_A = 25°C will be 37.5°C and δp = 0.005 • (37.5 – 25) = 0.0625. The required $R_{DS(ON)}$ is then given by:

$$R_{DS(ON)} \approx \frac{P_P}{DC \bullet I_{OUT}{}^2(1 + \delta p)} = 0.11\Omega$$

The P-channel MOSFET requirement can be met by an Si3443DV.

The requirement for the Schottky diode is the most stringent when V_{OUT} = 0V, i.e., short circuit. With a 0.03Ω R_{SENSE} resistor, the short-circuit current through the Schottky is 0.1/0.03 = 3.3A. An MBRS340T3 Schottky diode is chosen. With 3.3A flowing through, the diode is rated with a forward voltage of 0.4V. Therefore, the worst-case power dissipated by the diode is 1.32W. The addition of D_{FB1} and D_{FB2} (Figure 6) will reduce the diode dissipation to approximately 0.66W

The input capacitor requires an RMS current rating of at least 0.75A at temperature, and C_{OUT} will require an ESR of 0.1Ω for optimum efficiency.

APPLICATIONS INFORMATION

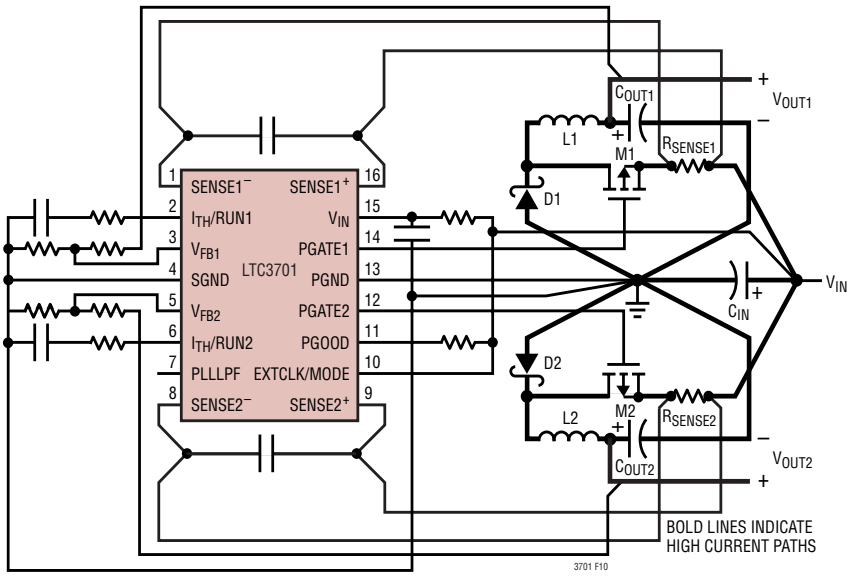


Figure 10. LTC3701 Layout Diagram

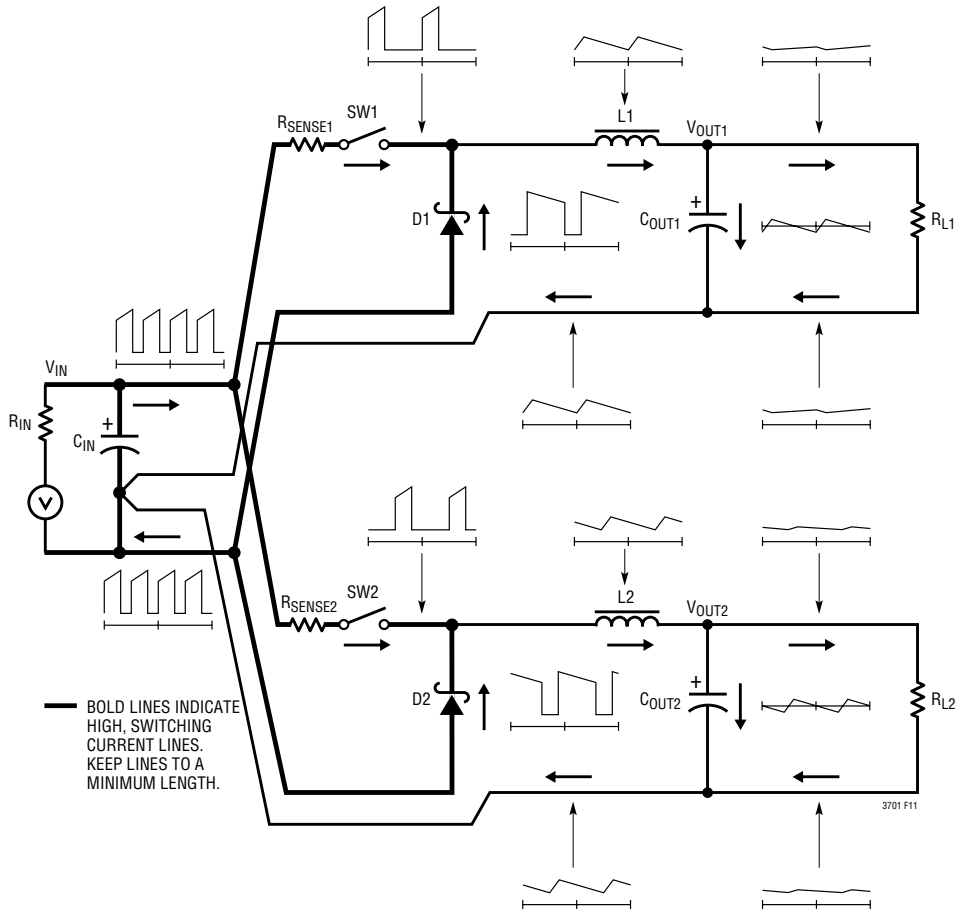
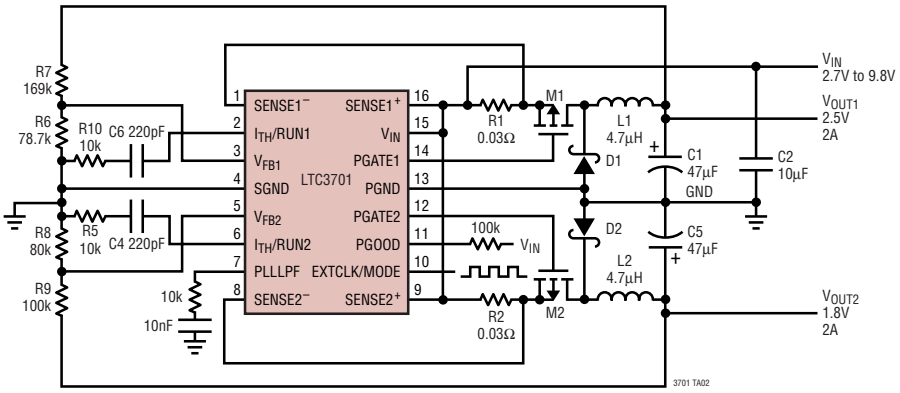


Figure 11. Branch Current Waveforms

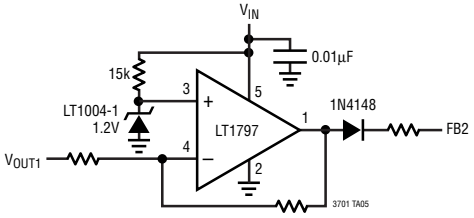
TYPICAL APPLICATIONS

2-Phase, Synchronizable Dual Output Step-Down DC/DC Converter

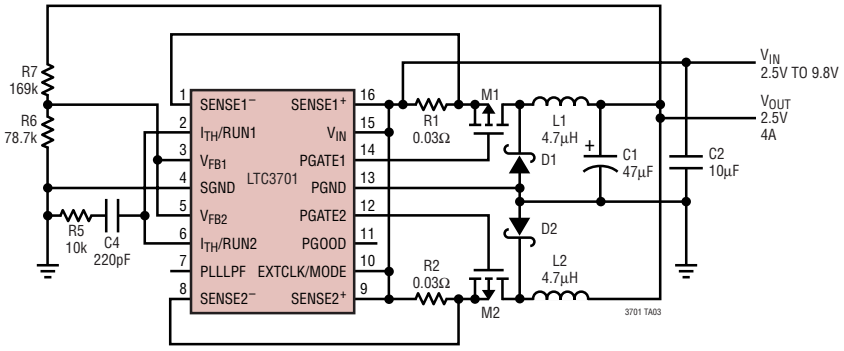


C1, C5: SANYO 6TPA47M
C2: TAIYO YUDEN LMK325BJ106K-T
D1, D2: IR10BQ015
L1, L2: MURATA LQN6C-4R7
M1, M2: Si3443DV
R1, R2: DALE 0.25W

Optional Output Sequencing Circuit

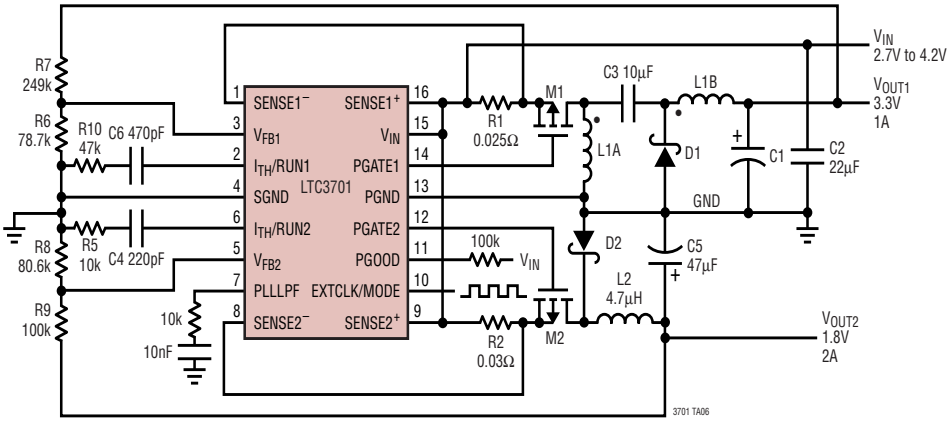


2-Phase, 550kHz Single Output Step-Down DC/DC Converter



C1: SANYO 6TPA47M
C2: TAIYO YUDEN LMK325BJ106K-T
D1, D2: IR10BQ015
L1, L2: MURATA LQN6C-4R7
M1, M2: Si3443DV
R1, R2: DALE 0.25W

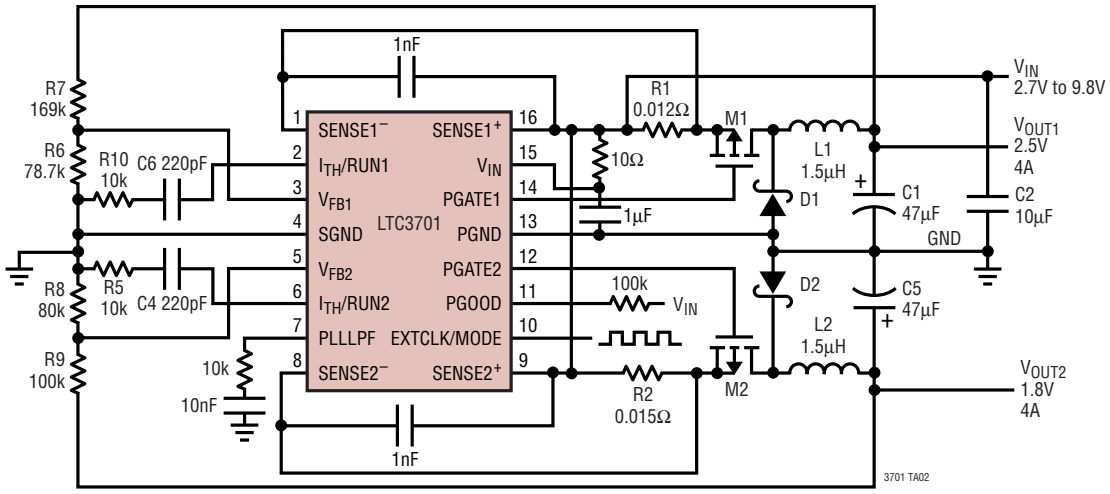
Single Cell Li-Ion to 3.3V (Zeta Converter) and 1.8V (Buck Converter)



C1, C5: SANYO 6TPA47M
C2: TAIYO YUDEN JMK325BJ226MM
C3: TAIYO YUDEN JMK316BJ106ML
D1, D2: IR10BQ015
L1A, L1B: COILTRONICS CTX5-2
L2: MURATA LQN6C-4R7
M1, M2: Si3443DV
R1, R2: DALE 0.25W

TYPICAL APPLICATIONS

2-Phase, Synchronizable Dual Output Step-Down DC/DC Converter with 4A Output Currents



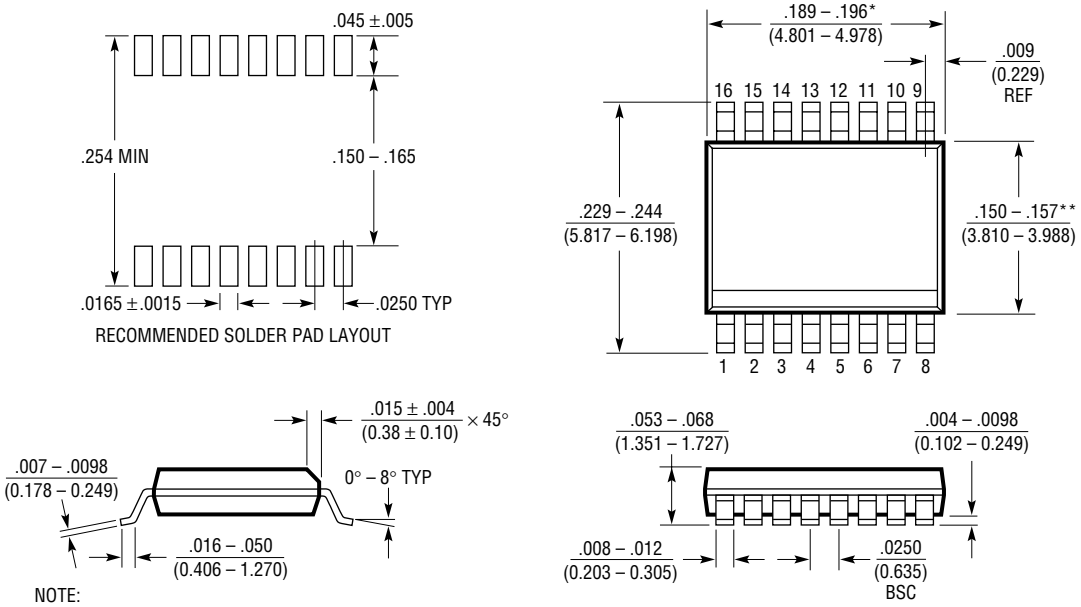
C1, C5: SANYO 6TPA47M
C2: TAIYO YUDEN LMK325BJ106K-T

D1, D2: IR30BQ015
L1, L2: COILCRAFT DO3316P-152

M1, M2: Si9803DY
R1, R2: DALE 0.25W

PACKAGE DESCRIPTION

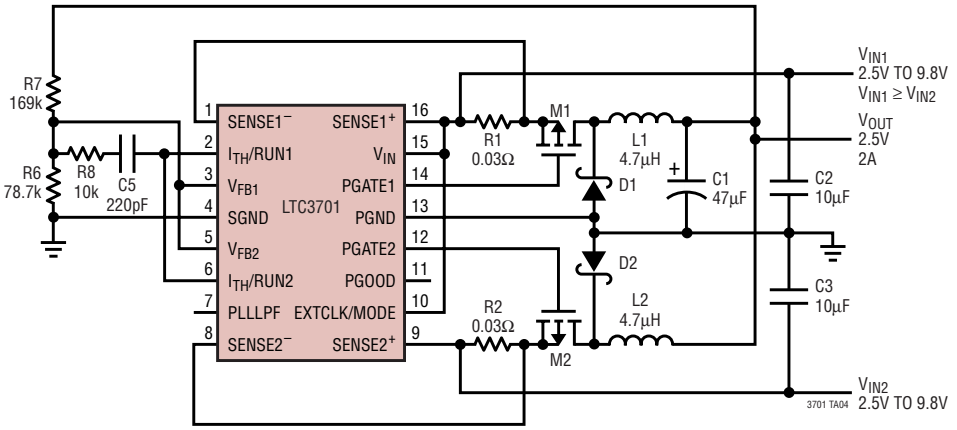
GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Dual Input Voltage Single Output, 2-Phase, 550kHz, Step-Down DC/DC Converter



C1: SANYO 6TPA47M
C2, C3: TAIYO YUDEN LMK325BJ106K-T
D1, D2: IR10BQ015

L1, L2: MURATA LQN6C-4R7
M1, M2: Si3443DV
R1, R2: DALE 0.25W

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1622	Synchronizable Low Input Voltage Current Mode Step-Down DC/DC Controller	V_{IN} 2V to 10V, Burst Mode Operation, 8-Lead MSOP
LTC1628/ LTC1628-PG	Dual High Efficiency, 2-Phase Synchronous Step Down Controllers	Constant Frequency, Standby, 5V and 3.3V LDOs, V_{IN} to 36V, 28-Lead SSOP
LTC1629/ LTC1629-PG	20A TO 200A PolyPhase™ High Efficiency Controllers	Expandable Up to 12 Phases, No Heat Sinks, V_{IN} to 36V, 28-Lead SSOP
LTC1702A	No R_{SENSE}™ 2-Phase Dual Synchronous Controller	550kHz, No Sense Resistor, GN24, V_{IN} to 7V
LTC1708-PG	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulators	1.3V≤ V_{OUT} ≤ 3.5V, Current Mode, 3.5V ≤ V_{IN} ≤ 36V
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, 3.5V ≤ V_{IN} ≤ 36V
LTC1767	1.2A I_{OUT}, 1.25MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, V_{OUT} = 1.2V, I_Q = 1mA, I_{SD} = 6µA, MS8E Package
LTC1772	Constant Frequency Current Mode Step-Down DC/DC Controller	2.5V ≤ V_{IN} ≤ 9.8V, I_{OUT} Up to 4A, SOT-23 Package, 550kHz
LTC1773	Synchronous Step-Down Controller	2.65V ≤ V_{IN} ≤ 8.5V, I_{OUT} Up to 4A, 10-Lead MSOP
LTC1778	No R_{SENSE} Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, 4V ≤ V_{IN} ≤ 36V
LTC1872	Constant Frequency Current Mode Step-Up Controller	2.5V ≤ V_{IN} ≤ 9.8V, SOT-23 Package, 550kHz
LTC1929	Constant Frequency Current Mode 2-Phase Synchronous Controller	Up to 42A, No Heat Sink, 3.5V ≤ V_{IN} ≤ 36V
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3700	Constant Frequency Step-Down Controller with LDO Regulator	2.65≤ V_{IN} ≤ 9.8V, 550kHz, 10-Lead SSOP
LTC3728/LTC3728L	Dual, 550kHz, 2-Phase Synchronous Step-Down Switching Regulator	Constant Frequency, V_{IN} to 36V, 5V and 3.3V LDOs, 5mm × 5mm QFN or 28-Lead SSOP

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