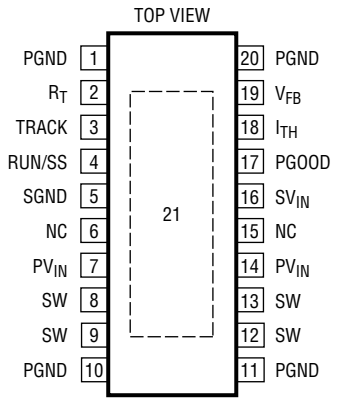
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 6V
I_{TH}, RUN, V_{FB} Voltages ..... –0.3V to V_{IN}
TRACK Voltage ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Notes 5, 6) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD IS GND (PIN 21)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3416EFE

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range			2.25		5.5	V
V_{FB}	Regulated Feedback Voltage	(Note 3)	●	0.784	0.800	0.816	V
I_{FB}	Feedback Input Current					0.2	µA
I_{TRACK}	TRACK Input Current					0.2	µA
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 3)			0.04	0.2	%/V
V_{TRACK}	Tracking Voltage Offset Tracking Voltage Range	V_{TRACK} = 0.4V		 0		30 0.8	mV V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop, V_{ITH} = 0.36V Measured in Servo Loop, V_{ITH} = 0.84V			0.02 –0.02	0.2 –0.2	% %
ΔV_{PGOOD}	Power Good Range				±7.5	±9	%
R_{PGOOD}	Power Good Resistance				120	200	Ω
I_Q	Input DC Bias Current Active Current Shutdown	(Note 4) V_{FB} = 0.7V, V_{ITH} = 1.2V V_{RUN} = 0V			 300 0.02	 350 1	 µA µA
f_{OSC}	Switching Frequency Switching Frequency Range	R_{OSC} = 294kΩ (Note 4)		0.88 0.30	1	1.12 4.00	MHz MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 300mA			67	100	mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –300mA			50	100	mΩ
I_{LIMIT}	Peak Current Limit			6	8		A
V_{UVLO}	Undervoltage Lockout Threshold			1.75	2	2.25	V
I_{LSW}	SW Leakage Current	V_{RUN} = 0V, V_{IN} = 5.5V			0.1	1	µA
V_{RUN}	RUN Threshold			0.5	0.65	0.8	V

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. The voltage should never exceed 6.0V for any pin.

Note 2: The LTC3416E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3416 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: This parameter is guaranteed by design and characterization.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

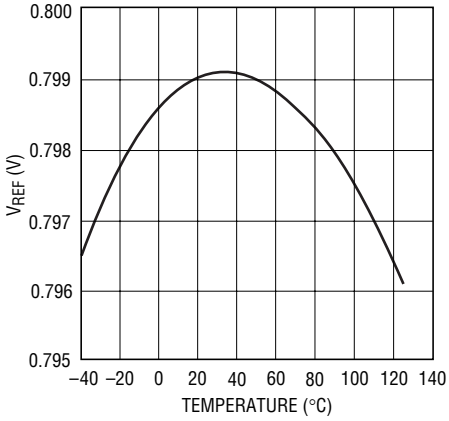
Note 6: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC3416E: $T_J = T_A + (P_D)(38°C/W)$

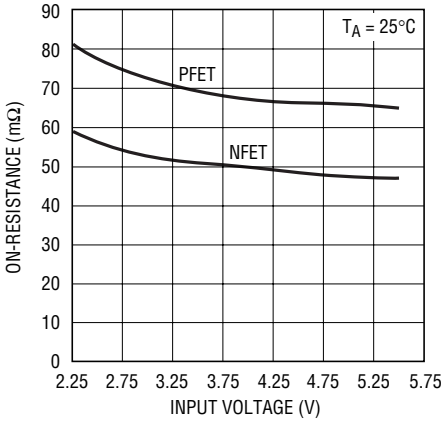
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

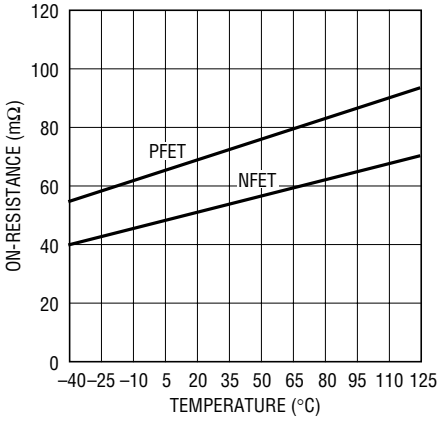
V_{REF} vs Temperature, V_{IN} = 3.3V



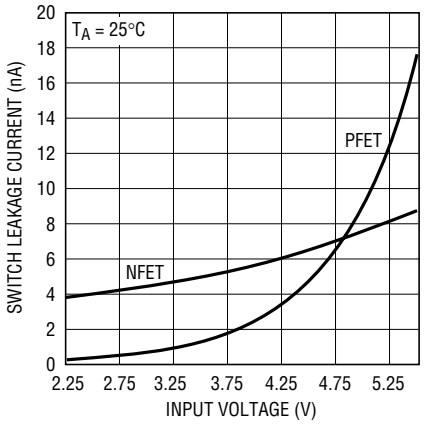
Switch On-Resistance vs Input Voltage



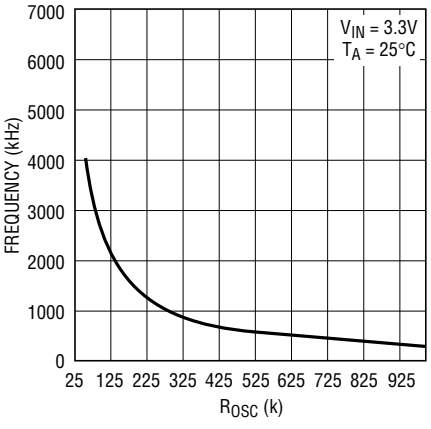
Switch On-Resistance vs Temperature, V_{IN} = 3.3V



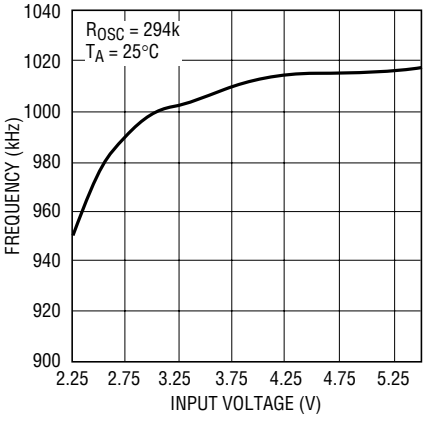
Switch Leakage vs Input Voltage



Frequency vs R_{OSC}

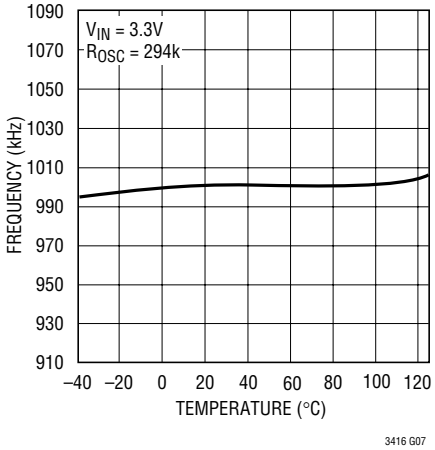


Frequency vs Input Voltage

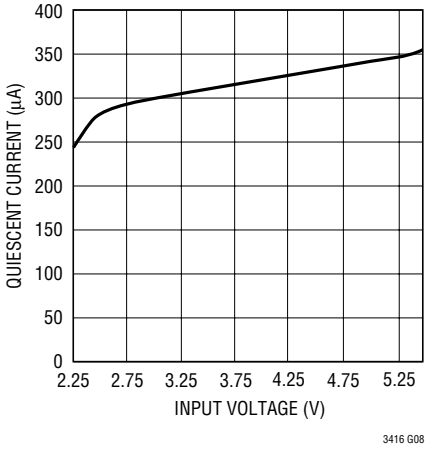


TYPICAL PERFORMANCE CHARACTERISTICS

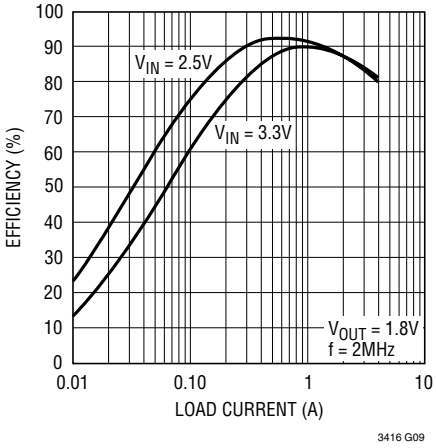
Frequency vs Temperature



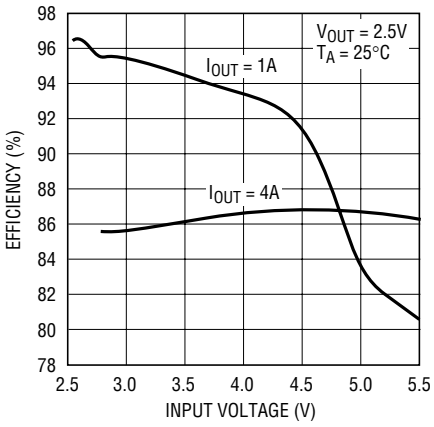
DC Supply Current vs Input Voltage



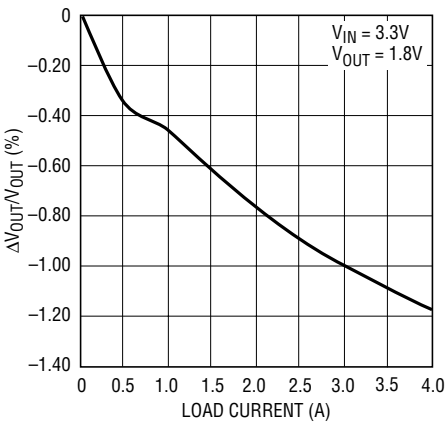
Efficiency vs Load Current, Forced Continuous



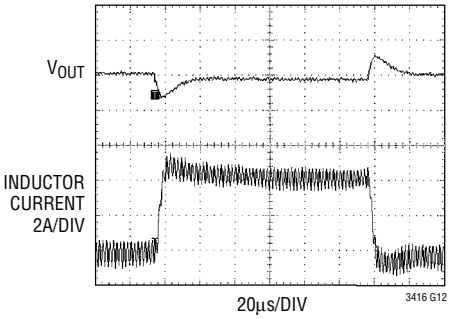
Efficiency vs Input Voltage



Load Regulation

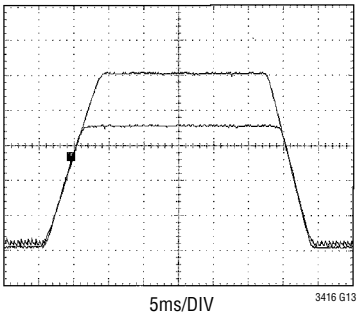


Load Step Transient



V_{IN} = 3.3V, V_{OUT} = 1.8V
f = 2MHz
LOAD STEP = 0A TO 4A

Tracking: Start-Up and Shutdown



V_{IN} = 3.3V, V_{OUT} = 1.8V
TRACKING 2.5V

PIN FUNCTIONS

PGND (Pins 1, 10, 11, 20): Power Ground. Connect this pin closely to the (–) terminal of C_{IN} and C_{OUT}.

R_T (Pin 2): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

TRACK (Pin 3): Tracking Voltage Input. Applying a voltage that is less than 0.8V to this pin enables tracking. During tracking, the V_{FB} pin will regulate to the voltage on this pin. Do not float this pin.

RUN/SS (Pin 4): Run Control and Soft-Start Input. Forcing this pin below 0.5V shuts down the LTC3416. In shutdown all functions are disabled, drawing <1µA of supply current. A capacitor to ground from this pin sets the ramp time to full output current.

SGND (Pin 5): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

NC (Pins 6, 15): No Connect.

PV_{IN} (Pins 7, 14): Power Input Supply. Decouple this pin to PGND with a capacitor.

SW (Pins 8, 9, 12, 13): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

SV_{IN} (Pin 16): Signal Input Supply. Decouple this pin to the SGND capacitor.

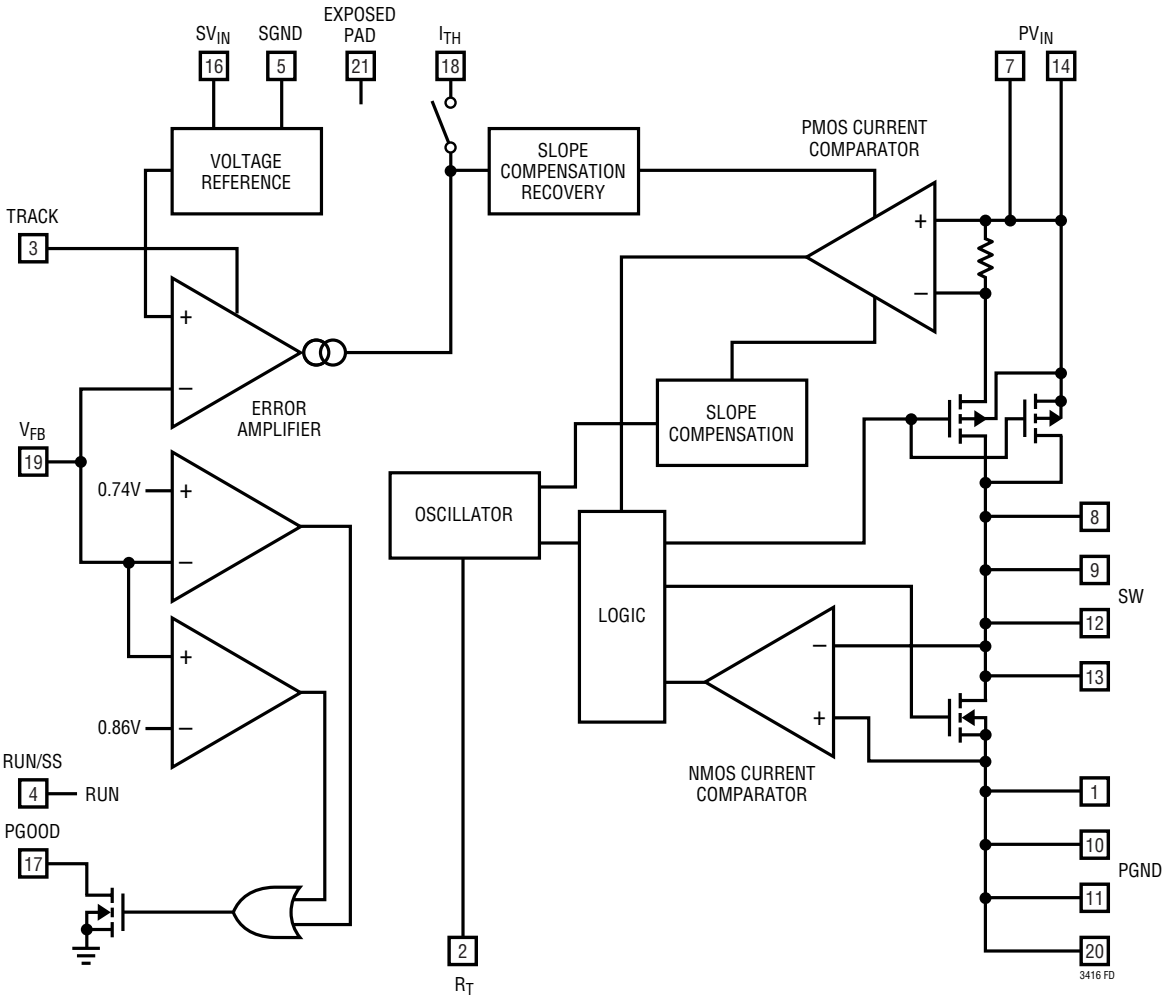
PGOOD (Pin 17): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

I_{TH} (Pin 18): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.2V to 1.4V with 0.4V corresponding to the zero-sense voltage (zero current).

V_{FB} (Pin 19): Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output.

Exposed Pad (Pin 21): Ground. Connect to SGND.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3416 is a monolithic, constant frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the I_{TH} pin. The error amplifier adjusts the voltage on the I_{TH} pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the I_{TH} voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –5A.

The operating frequency is externally set by an external resistor connected between the R_T pin and ground. The practical switching frequency can range from 300kHz to 4MHz.

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±7.5%. In an overvoltage condition, the top

OPERATION

power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

Voltage Tracking

Some microprocessors, ASIC and DSP chips need two power supplies with different voltage levels. These systems often require voltage sequencing between the core power supply and the I/O power supply. Without proper sequencing, latch-up failure or excessive current draw may occur that could result in damage to the processor's I/O ports or the I/O ports of supporting system devices such as memory, FPGAs or data converters. To ensure that the I/O loads are not driven until the core voltage is properly biased, tracking of the core supply voltage and the I/O supply voltage is necessary.

Voltage tracking is enabled by applying a voltage to the TRACK pin. When the voltage on the TRACK pin is below 0.8V, the feedback voltage will regulate to this tracking voltage. When the tracking voltage exceeds 0.8V, tracking control over the feedback voltage is gradually released. Full release of tracking control over the feedback voltage is achieved when the tracking voltage exceeds 1.05V.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3416 is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3416 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3416, however, slope compensation recovery is implemented to keep the maximum inductor peak current constant throughout the range of duty cycles. This keeps the maximum output current relatively constant regardless of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current exceeds 7.8A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

APPLICATIONS INFORMATION

The basic LTC3416 application circuit is shown in Figure 1a. External component selection is determined by the maximum load current and begins with the selection of the operating frequency and inductor value followed by C_{IN} and C_{OUT}.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3416 is determined by an external resistor that is connected between the R_T pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{OSC} = \frac{3.08 \bullet 10^{11}}{f}(\Omega) - 10k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3416 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 • 110ns • f(Hz).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} or lower V_{OUT} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the source of the top MOSFET. To

APPLICATIONS INFORMATION

prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V \left(1 + \frac{R2}{R1} \right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 2.

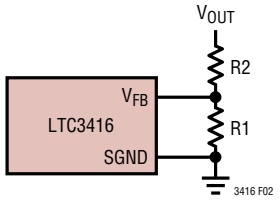


Figure 2. Setting the Output Voltage

Voltage Tracking

The LTC3416 allows the user to program how its output voltage ramps during start-up by means of the TRACK pin. Through this pin, the output voltage can be set up to either

APPLICATIONS INFORMATION

coincidentally or ratiometrically track another output voltage as shown in Figure 3.

If the voltage on the TRACK pin is less than 0.8V, voltage tracking is enabled. During voltage tracking, the output voltage regulates to the tracking voltage through a resistor divider network. The output voltage during tracking can be calculated with the following equation:

$$V_{OUT} = V_{TRACK}\left(1+\frac{R2}{R1}\right),\ V_{TRACK} < 0.8V$$

Voltage tracking can be accomplished by sensing a fraction of the output voltage from another regulator. This is typically done by using a resistor divider to attenuate the output voltage that is being tracked. Setting this attenuation factor equal to the reciprocal of the gain factor provided by the feedback resistors will force the regulator outputs to be equal to each other during tracking. If tracking is not desired, connect the TRACK pin to SV_{IN}.

To implement the coincident tracking shown in Figure 3a, connect an extra resistor divider to the output of V_{OUT2} and connect its midpoint to the TRACK pin of the LTC3416 as shown in Figure 4. The ratio of this divider should be selected the same as that of V_{OUT1}'s resistor divider. To implement the ratiometric sequencing in Figure 3b, the extra resistor divider's ratio should be set so that the TRACK pin voltage exceeds 1.05V by the end of the start-up period. The LTC3416 utilizes a method in which the TRACK pin's control over the output voltage is gradually released as the TRACK pin voltage approaches 0.8V. With this technique, some overdrive will be required on the TRACK pin to ensure that the tracking function is completely disabled at the end of the start-up period.

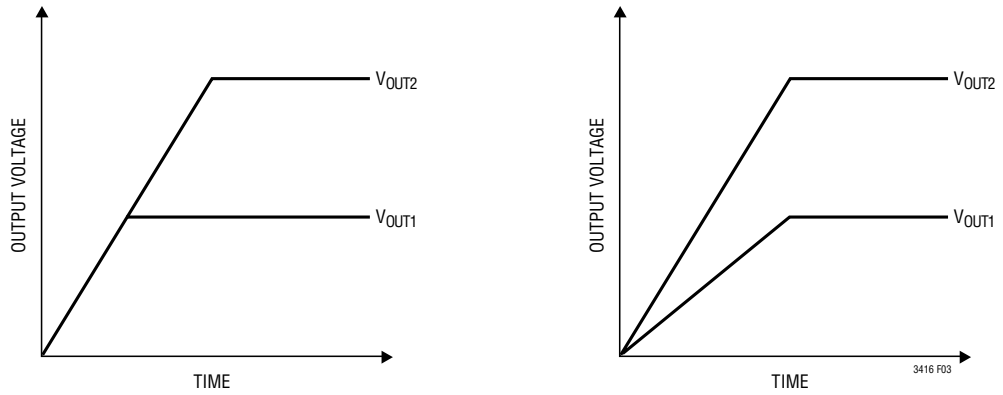
For coincident tracking, the following condition should be satisfied to ensure that tracking is disabled at the end of start-up.

$$V_{OUT2} \geq 1.32\ V_{OUT1}$$

For ratiometric tracking, the following equation can be used to calculate the resistor values:

$$R4 = R3\left(\frac{V_{OUT2}}{V_{TRACK}} - 1\right)$$

$$V_{TRACK} \geq 1.05V$$



(3a) Coincident Tracking **(3b) Ratiometric Sequencing**

Figure 3. Two Different Modes of Output Voltage Sequencing

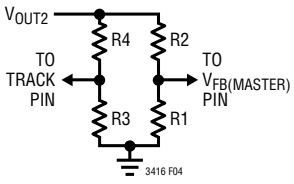


Figure 4. Setup for Tracking and Ratiometric Sequencing

APPLICATIONS INFORMATION

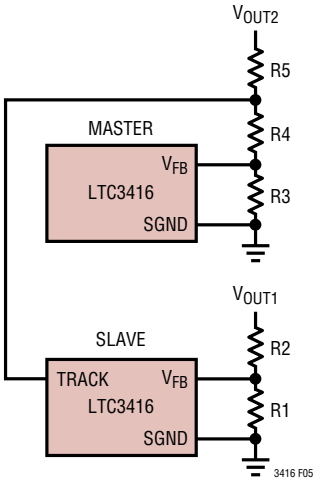


Figure 5. Dual Voltage System with Tracking

An alternative method of tracking is shown in Figure 5. For the circuit of Figure 5, the following equations can be used to determine the resistor values:

$$V_{OUT1} = 0.8V\left(1+\frac{R2}{R1}\right)$$

$$V_{OUT2} = 0.8V\left(1+\frac{R4+R5}{R3}\right)$$

$$R4 = R3\left(\frac{V_{OUT2}}{V_{OUT1}}-1\right)$$

Soft-Start

The RUN/SS pin provides a means to shut down the LTC3416 as well as a timer for soft-start. Pulling the RUN/SS pin below 0.5V places the LTC3416 in a low quiescent current shutdown state (I_Q < 1µA).

The soft-start gradually raises the clamp on I_{TH}. The full current range becomes available on I_{TH} after the voltage on I_{TH} reaches approximately 2V. The clamp on I_{TH} is set externally with a resistor and capacitor on the RUN/SS pin. The soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS}C_{SS}\ln\left(\frac{V_{IN}}{V_{IN}-1.8V}\right)(\text{Seconds})$$

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses.

The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

APPLICATIONS INFORMATION

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

In most applications, the LTC3416 does not dissipate much heat due to its high efficiency. But in applications where the LTC3416 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3416 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. For the 20-lead exposed TSSOP package, the θ_{JA} is 38°C/W.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$). To maximize the thermal performance of the LTC3416, the Exposed Pad should be soldered to a ground plane.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current.

When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD}(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components and output capacitor shown in figure 1a will provide adequate compensation for most applications.

Design Example

As a design example, consider using the LTC3416 in an application with the following specifications: V_{IN} = 3.3V, V_{OUT1} = 1.8V, V_{OUT2} = 2.5V, $I_{OUT1(MAX)}$ = $I_{OUT2(MAX)}$ = 4A, f = 1MHz. V_{OUT1} and V_{OUT2} must track when powering up and powering down.

First, calculate the timing resistor:

$$R_{OSC} = \frac{3.08 \bullet 10^{11}}{1 \bullet 10^{6}} - 10k = 298k$$

Use a standard value of 294kΩ. Next, calculate the inductor values for about 40% ripple current:

$$L1 = \left(\frac{1.8V}{1MHz \bullet 1.6A}\right)\left(1 - \frac{1.8V}{3.3V}\right) = 0.51\mu H$$

$$L2 = \left(\frac{2.5V}{1MHz \bullet 1.6A}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 0.38\mu H$$

Using a 0.47µH inductor for both results in maximum ripple currents of:

$$\Delta I_{L1} = \left(\frac{1.8V}{1MHz \bullet 0.47\mu H}\right)\left(1 - \frac{1.8V}{3.3V}\right) = 1.74A$$

$$\Delta I_{L2} = \left(\frac{2.5V}{1MHz \bullet 0.47\mu H}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 1.29A$$

C_{OUT1} and C_{OUT2} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100µF ceramic capacitors will be used at each output.

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C_{IN1} and C_{IN2} should be sized for a maximum current rating of:

$$I_{RMS1} = 4A\left(\frac{1.8V}{3.3V}\right)\sqrt{\frac{3.3V}{1.8V}-1} = 1.99A_{RMS}$$

$$I_{RMS2} = 4A\left(\frac{2.5V}{3.3V}\right)\sqrt{\frac{3.3V}{2.5V}-1} = 1.71A_{RMS}$$

Decoupling the PV_{IN} and SV_{IN} pins with two 100µF capacitors on both switching regulators is adequate for most applications.

The resitor values for the voltage divider on V_{OUT1} can be calculated by using the following equation:

$$1.8V = 0.8V\left(1+\frac{R2}{R1}\right)$$

Setting R1 to 200k results in a value of 255k for R2. To calculate the resistor values for the voltage divider on V_{OUT2}, we can use the following equations:

$$R4 = R3\left(\frac{2.5V}{1.8V}-1\right)$$

$$2.5V = 0.8V\left(1+\frac{R4+R5}{R3}\right)$$

Setting R3 to 205k gives the following results: R4 = 78.7k and R5 = 357k. Figure 6 shows the complete schematic for this design example.

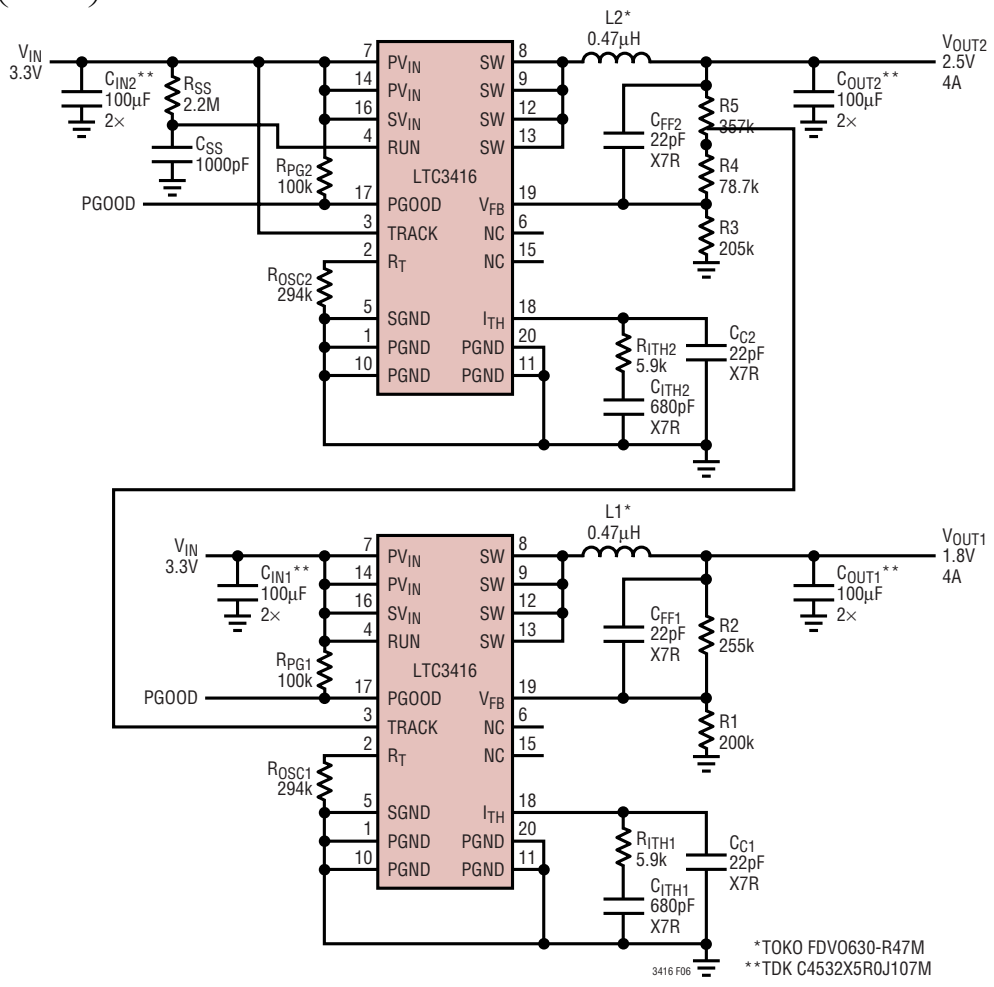


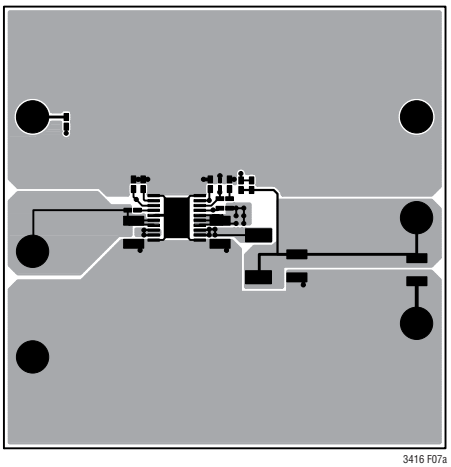
Figure 6. 1.8V and 2.5V, 4A Voltage Tracking Regulators at 1MHz

APPLICATIONS INFORMATION

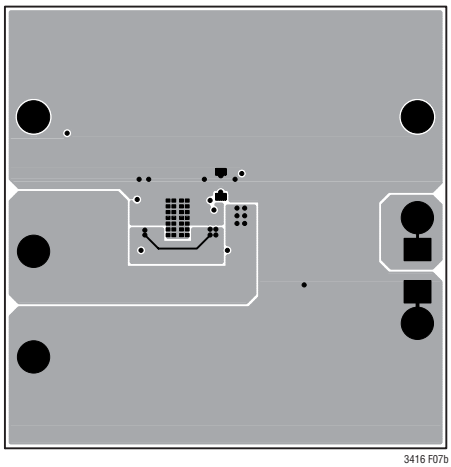
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3416. Check the following in your layout.

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3416.
2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (PV_{IN}, SV_{IN}, V_{OUT}, PGND, SGND or any other DC rail in your system).
5. Connect the V_{FB} pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and SGND.



(7a) Top Layer

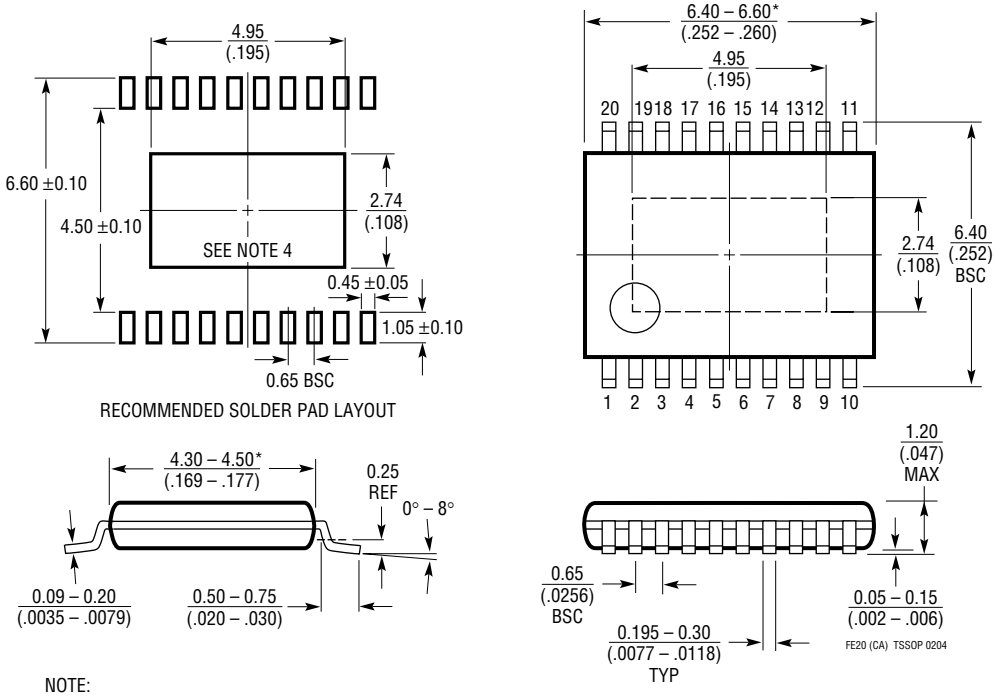


(7b) Bottom Layer

Figure 7. LTC3416 Layout Diagram

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CA

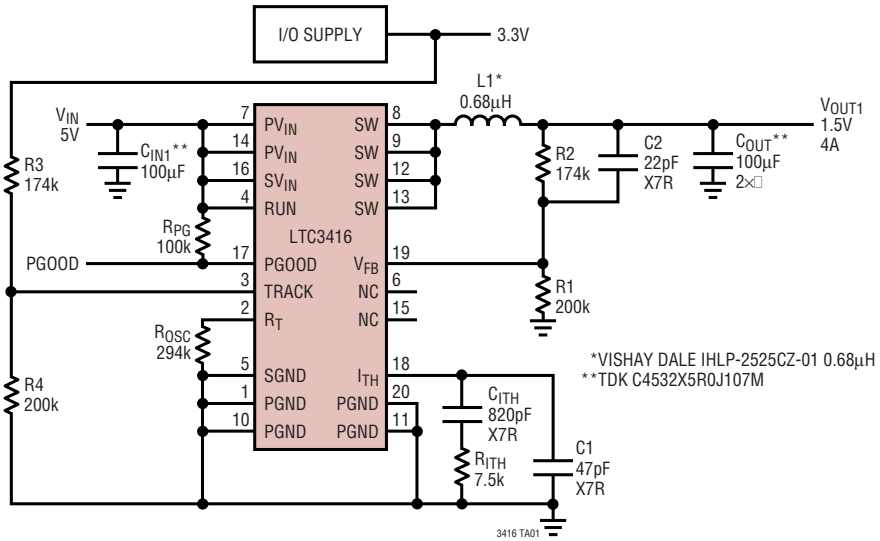


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

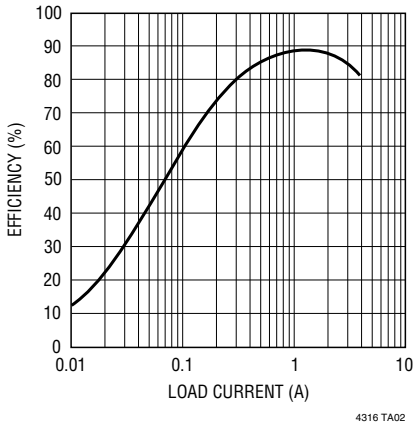
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

1.5V, 4A Step-Down Regulator Tracking from 3.3V I/O Supply



Efficiency vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1616	500mA (I_{OUT}), 1.4MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3.6V to 25V, V_{OUT} = 1.25V, I_Q = 1.9mA, I_{SD} < 1µA, ThinSOT Package
LT1676	450mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 7.4V to 60V, V_{OUT} = 1.24V, I_Q = 3.2mA, I_{SD} < 2.5µA, S8 Package
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, V_{OUT} = 1.2V, I_Q = 1mA, I_{SD} < 15µA, S8, TSSOP16E Packages
LT1776	500mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 7.4V to 40V, V_{OUT} = 1.24V, I_Q = 3.2mA, I_{SD} < 30µA, N8, S8 Packages
LTC1879	1.20A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.7V to 10V, V_{OUT} = 0.8V, I_Q = 15µA, I_{SD} < 1µA, TSSOP16 Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.75V to 6V, V_{OUT} = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS, DFN Packages
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 0.8V I_Q = 60µA, I_{SD} < 1µA, TSSOP16E Package
LTC3413	3A (I_{OUT} Sink/source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, V_{OUT} = V_{REF}/2, I_Q = 280µA, I_{SD} < 1µA, TSSOP16E Package
LTC3414	4A (I_{OUT}), 4MHz Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.25V to 5V, V_{OUT} to 0.8V, I_Q = 64µA, TSSOP28E Package
LTC3430	60V, 2.75A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 5.5V to 60V, V_{OUT} = 1.2V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16E Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT} = 2.5V, I_Q = 25µA, I_{SD} < 1µA, MS Package

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