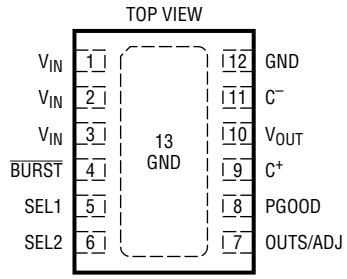
ABSOLUTE MAXIMUM RATINGS

(Note 1)

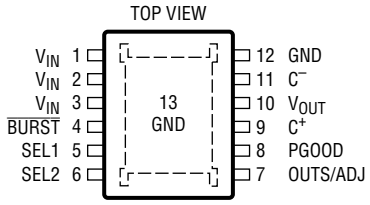
V_{IN}, SEL1, SEL2, $\overline{BURST}$ ..... –0.3V to 38V
V_{OUT}, OUTS/ADJ, PGOOD ..... –0.3V to 6V
I_{PGOOD} 2mA
V_{OUT} Short-Circuit Duration ..... Indefinite

Operating Junction Temperature Range (Notes 2, 3)
(E-/I-Grade) ..... –40°C to 125°C
(H-Grade) ..... –40°C to 150°C
(MP-Grade) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(MSE Only) ..... 300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (3mm × 4mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB GND



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3245EDE#PBF	LTC3245EDE#TRPBF	3245	12-Lead (3mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3245IDE#PBF	LTC3245IDE#TRPBF	3245	12-Lead (3mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3245EMSE#PBF	LTC3245EMSE#TRPBF	3245	12-Lead Plastic MSOP	–40°C to 125°C
LTC3245IMSE#PBF	LTC3245IMSE#TRPBF	3245	12-Lead Plastic MSOP	–40°C to 125°C
LTC3245HMSE#PBF	LTC3245HMSE#TRPBF	3245	12-Lead Plastic MSOP	–40°C to 150°C
LTC3245MPMSE#PBF	LTC3245MPMSE#TRPBF	3245	12-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, (Note 2). V_{IN} = 12V, V_{OUT} = 5V, C_{FLY} = 1µF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Input Voltage Range		●	2.7		38	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling	●		2.4 2.2	2.7	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, (Note 2). V_{IN} = 12V, V_{OUT} = 5V, C_{FLY} = 1µF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VIN}	V_{IN} Quiescent Current SEL1 = SEL2 = 0V V_{OUT} Enabled, $\overline{BURST}$ = 0V V_{OUT} Enabled, $\overline{BURST}$ = V_{IN}	 Shutdown, V_{OUT} = 0V CP Enabled, Output in Regulation CP Enabled, Output in Regulation	 		 4 18 20	 8 35 40	 µA µA µA
V_{OUT5_BM}	Fixed 5V Burst Mode Output Regulation (OUTS/ADJ Connected to V_{OUT}, $\overline{BURST}$ = 0V, SEL2 = V_{IN}, SEL1 = 0V) (Note 5)	5V ≤ V_{IN} < 38V, I_{OUT} ≤ 250mA 4V ≤ V_{IN} < 5V, I_{OUT} ≤ 150mA 3.3V ≤ V_{IN} < 4V, I_{OUT} ≤ 75mA 3V ≤ V_{IN} < 3.3V, I_{OUT} ≤ 45mA	● ● ● ●	4.8 4.8 4.8 4.8		5.2 5.2 5.2 5.2	V V V V
V_{OUT5_LN}	Fixed 5V Low Noise Output Regulation (OUTS/ADJ Connected to V_{OUT}, $\overline{BURST}$ = V_{IN}, SEL2 = V_{IN}, SEL1 = 0V) (Note 5)	5V ≤ V_{IN} < 38V, I_{OUT} ≤ 200mA 4V ≤ V_{IN} < 5V, I_{OUT} ≤ 120mA 3.3V ≤ V_{IN} < 4V, I_{OUT} ≤ 60mA 3V ≤ V_{IN} < 3.3V, I_{OUT} ≤ 35mA	● ● ● ●	4.8 4.8 4.8 4.8		5.2 5.2 5.2 5.2	V V V V
V_{OUT33_BM}	Fixed 3.3V Burst Mode Output Regulation (OUTS/ADJ Connected to V_{OUT}, $\overline{BURST}$ = 0V, SEL2 = V_{IN}, SEL1 = V_{IN}) (Note 5)	5V ≤ V_{IN} < 38V, I_{OUT} ≤ 250mA 4V ≤ V_{IN} < 5V, I_{OUT} ≤ 175mA 3.3V ≤ V_{IN} < 4V, I_{OUT} ≤ 110mA 2.7V ≤ V_{IN} < 3.3V, I_{OUT} ≤ 60mA	● ● ● ●	3.17 3.17 3.17 3.17		3.43 3.43 3.43 3.43	V V V V
V_{OUT33_LN}	Fixed 3.3V Low Noise Output Regulation (OUTS/ADJ Connected to V_{OUT}, $\overline{BURST}$ = V_{IN}, SEL2 = V_{IN}, SEL1 = V_{IN}) (Note 5)	5V ≤ V_{IN} < 38V, I_{OUT} ≤ 220mA 4V ≤ V_{IN} < 5V, I_{OUT} ≤ 140mA 3.3V ≤ V_{IN} < 4V, I_{OUT} ≤ 90mA 2.7V ≤ V_{IN} < 3.3V, I_{OUT} ≤ 50mA	● ● ● ●	3.17 3.17 3.17 3.17		3.43 3.43 3.43 3.43	V V V V
V_{ADJ}	OUTS/ADJ Reference Voltage (Note 4)	SEL2 = 0V, SEL1 = V_{IN}, I_{OUT} = 0mA	●	1.176	1.200	1.224	V
R_{CL}	Load Regulation (Referred to ADJ)	SEL2 = 0V, SEL1 = V_{IN}			0.2		mV/mA
V_{PG_RISE}	PGOOD Rising Threshold	V_{OUT}% of Final Regulation Voltage			95	98	%
V_{PG_FALL}	PGOOD Falling Threshold	V_{OUT}% of Final Regulation Voltage		88	91		%
V_{PG_LOW}	PGOOD Output Low Voltage	I_{PGOOD} = 0.2mA	●		0.1	0.4	V
I_{PG_HIGH}	PGOOD Output High Leakage	V_{PGOOD} = 5V		–1	0	1	µA
V_{LOW}	$\overline{BURST}$, SEL1, SEL2 Input Voltage		●	0.4	0.9		V
V_{HIGH}	$\overline{BURST}$, SEL1, SEL2 input Voltage		●		1.2	2	V
I_{LOW}	$\overline{BURST}$, SEL1, SEL2 Input Current	V_{PIN} = 0V		–1	0	1	µA
I_{HIGH}	$\overline{BURST}$, SEL1, SEL2 Input Current	V_{PIN} = 38V		0.5	1	3	µA
I_{SHORT_CKT}	I_{VOUT} Short-Circuit Current	V_{OUT} = GND			900		mA
R_{OUT}	Charge Pump Output Impedance	2:1 Step-Down Mode 1:1 Step-Down Mode 1:2 Step-Up Mode (V_{IN} = 3.3V)			3 3.5 14		Ω Ω Ω
f_{OSC}	Oscillator Frequency		●		450	500	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. This IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 2: The LTC3245E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3245I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3245H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3245MP is tested and guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 150°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$ where θ_{JA} (in °C/W) is the package thermal impedance.

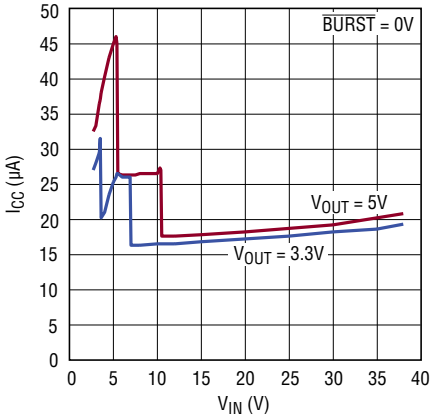
Note 4: V_{OUT} programming range is from 2.5V to 5V. See the Programming the Output Voltage section for more detail.

Note 5: The maximum operating junction temperature of 150°C must be followed. Certain combinations of input voltage and output current will cause the junction temperature to exceed 150°C and must be avoided. See Thermal Management section for information on calculating maximum operating conditions.

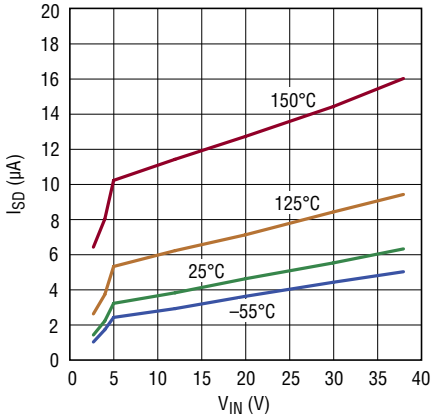
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

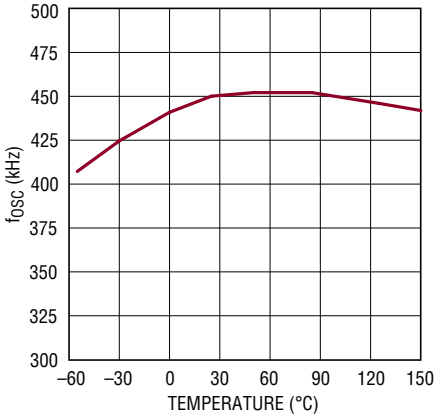
Input Operating Current vs Input Voltage



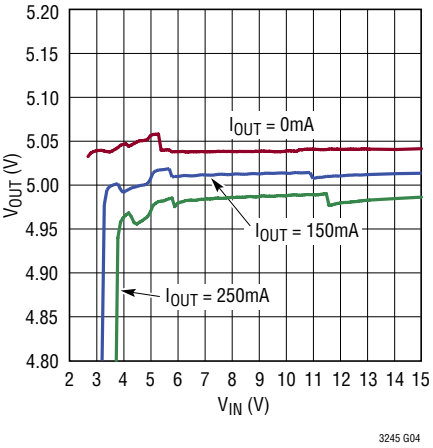
Input Shutdown Current vs Input Voltage



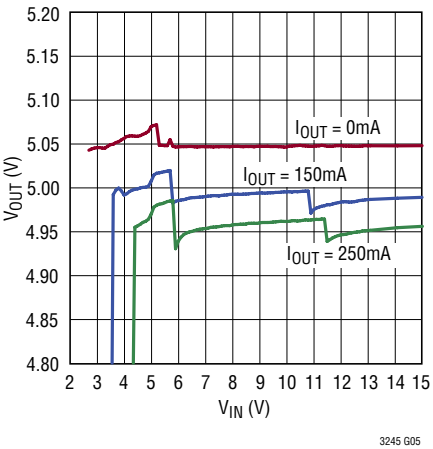
Oscillator Frequency vs Temperature



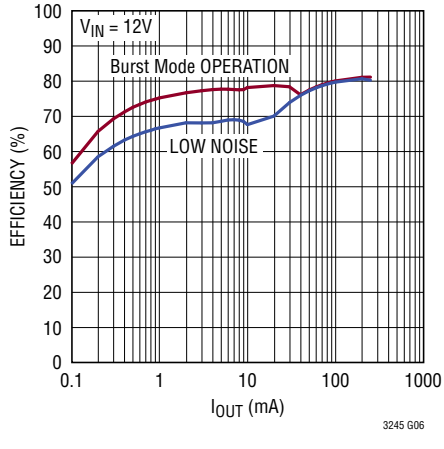
5V Fixed Output Voltage vs Input Voltage (Burst Mode Operation)



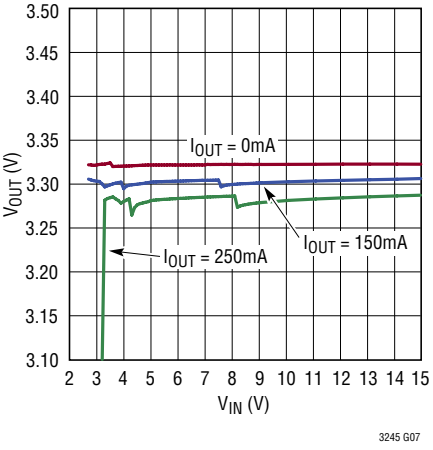
5V Fixed Output Voltage vs Input Voltage (Low Noise Operation)



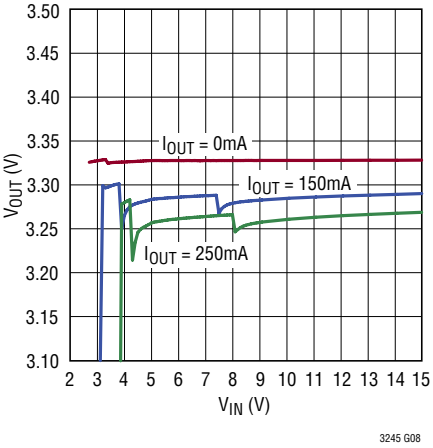
5V Fixed Efficiency vs Output Current



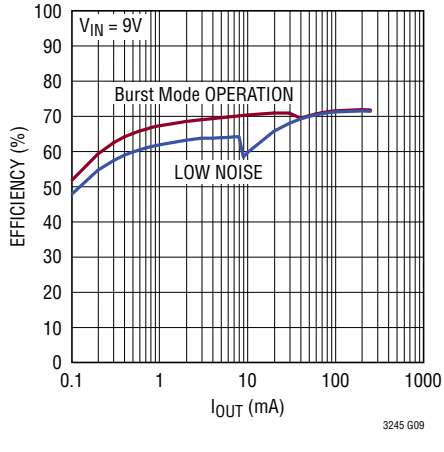
3.3V Fixed Output Voltage vs Input Voltage (Burst Mode Operation)



3.3V Fixed Output Voltage vs Input Voltage (Low Noise Operation)



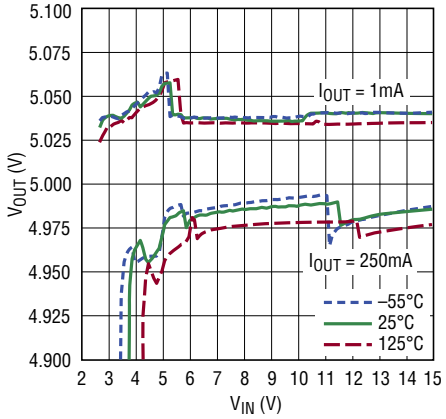
3.3V Fixed Output Efficiency vs Output Current



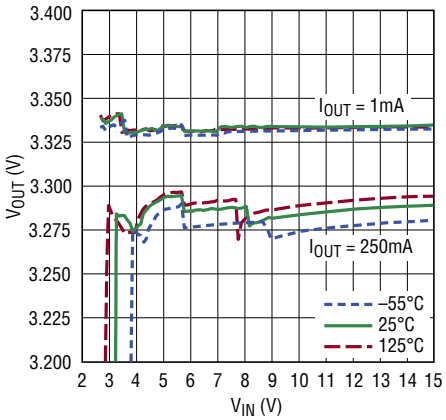
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

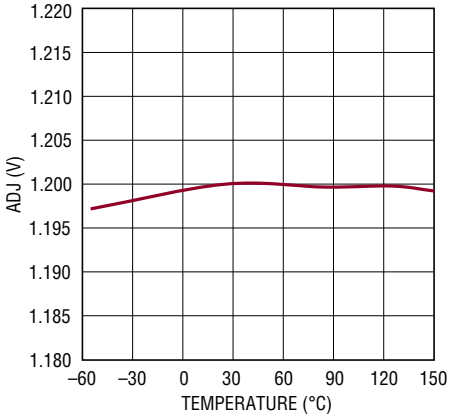
5V Fixed Output Voltage vs Falling Input Voltage (Burst Mode Operation)



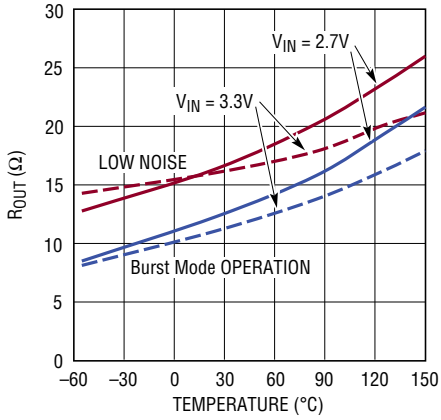
3.3V Fixed Output Voltage vs Falling Input Voltage (Burst Mode Operation)



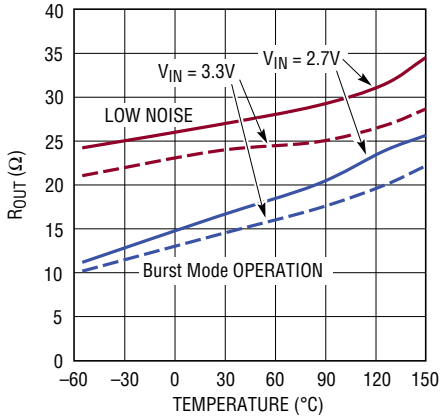
ADJ Regulation Voltage vs Temperature



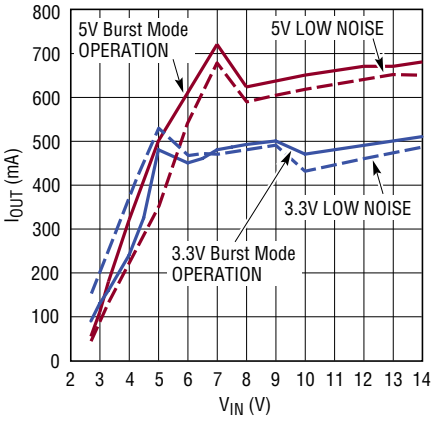
5V Output Impedance vs Temperature (Boost Mode)



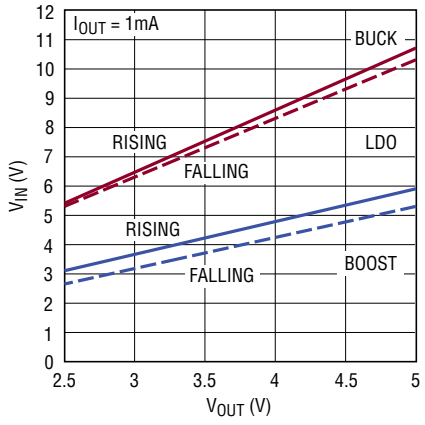
3.3V Output Impedance vs Temperature (Boost Mode)



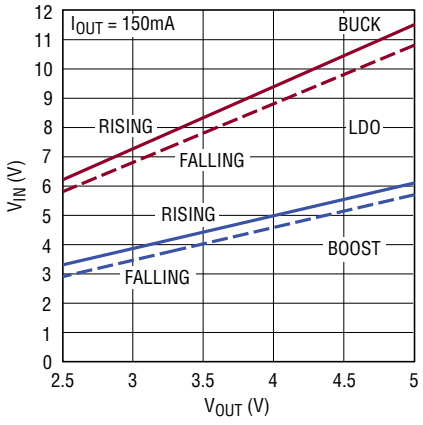
Output Current vs Input Voltage (V_{OUT} 5% Below Regulation)



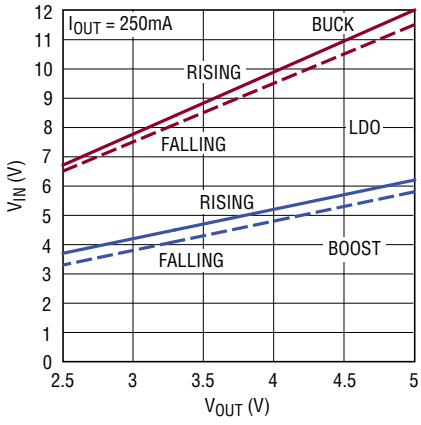
Operating Mode Transition Voltage vs Input Voltage



Operating Mode Transition Voltage vs Input Voltage



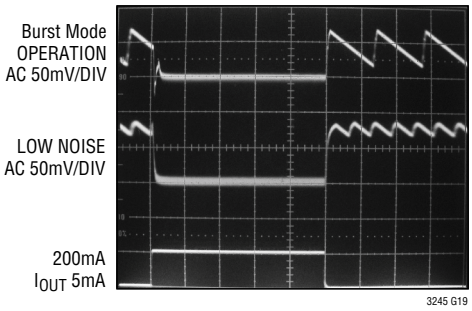
Operating Mode Transition Voltage vs Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

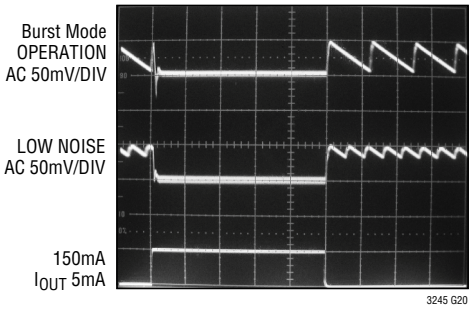
T_A = 25°C, unless otherwise noted.

5V Output Transient Response



V_{IN} = 12V
V_{OUT} = 5V

3.3V Output Transient Response



V_{IN} = 12V
V_{OUT} = 3.3V

PIN FUNCTIONS

V_{IN} (Pins 1, 2, 3): Power Input Pins. Input voltage for both charge pump and IC control circuitry. The V_{IN} pin operates from 2.7V to 38V. All V_{IN} pins should be connected together at pins.

$\overline{BURST}$ (Pin 4): Burst Mode Logic Input. A logic high on the $\overline{BURST}$ pin operates the charge pump in low noise constant frequency. A logic low will operates the charge pump in Burst Mode operation for higher efficiency at low output currents. The $\overline{BURST}$ pin has a 1µA (typical) pull-down current to ground and can tolerate 38V inputs allowing it to be pin-strapped to V_{IN}.

SEL1 (Pin 5): Logic Input Pin. See Table 1 for SEL1/SEL2 operating logic. The SEL1 pin has a 1µA (typical) pull-down current to ground and can tolerate 38V inputs allowing it to be pin-strapped to V_{IN}.

SEL2 (Pin 6): Logic Input Pin. See Table 1 for SEL1/SEL2 operating logic. The SEL2 pin has a 1µA (typical) pull-down current to ground and can tolerate 38V inputs allowing it to be pin-strapped to V_{IN}.

Table 1: V_{OUT} Operating Modes

SEL2	SEL1	MODE
LOW	LOW	Shutdown
LOW	HIGH	Adjustable V_{OUT}
HIGH	LOW	Fixed 5V
HIGH	HIGH	Fixed 3.3V

OUTS/ADJ (Pin 7): V_{OUT} Sense / Adjust Input Pin. This pin acts as V_{OUT} sense (OUTS) for 5V or 3.3V fixed outputs and adjust (ADJ) for adjustable output through external feedback. The ADJ pin servos to 1.2V when the device is enabled in adjustable mode. (OUTS / ADJ are selected by SEL1 and SEL2 pins; See Table 1)

PGOOD (Pin 8): Power Good Open Drain Logic Output. The PGOOD pin goes high impedance when V_{OUT} is about 6% of its final operating voltage. PGOOD is intended to be pulled up to V_{OUT} or other low voltage supply with an external resistor.

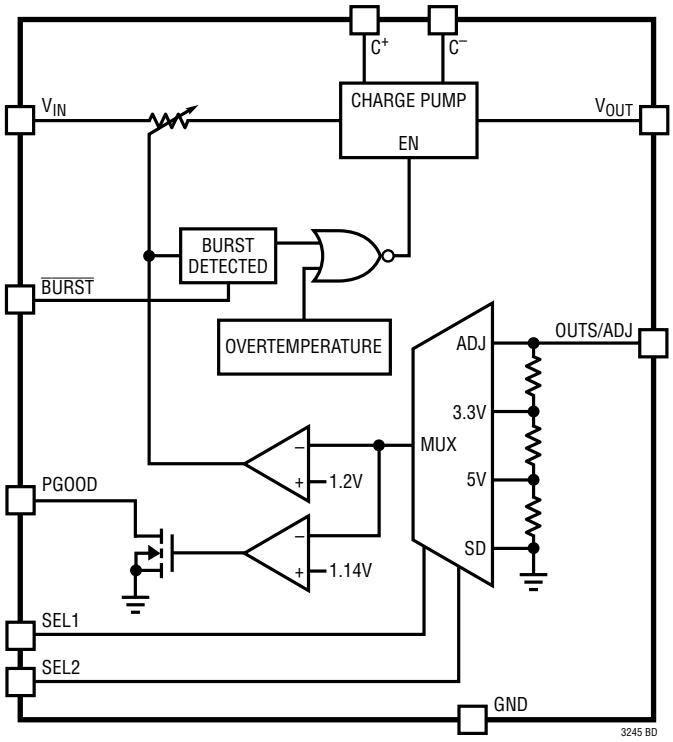
C^+ (Pin 9): Flying Capacitor Positive Connection.

V_{OUT} (Pin 10): Charge Pump Output Voltage. If V_{IN} drops below its UVLO threshold, the connection from V_{IN} becomes high impedance with no reverse leakage from V_{OUT} to V_{IN}. V_{OUT} regulation only takes place above the UVLO threshold. V_{OUT} can be programmed to regulate from 2.5V to 5V.

C^- (Pin 11): Flying Capacitor Negative Connection.

GND (Pin 12, Exposed Pad Pin 13): Ground. The exposed package pad is ground and must be soldered to the PC board ground plane for proper functionality and for rated thermal performance.

SIMPLIFIED BLOCK DIAGRAM



APPLICATIONS INFORMATION

General Operation

The LTC3245 uses switched capacitor based DC/DC conversion to provide the efficiency advantages associated with inductor based circuits as well as the cost and simplicity advantages of a linear regulator. The LTC3245's unique constant frequency architecture provides a low noise regulated output as well as lower input noise than conventional switch capacitor charge pump regulators. The LTC3245 uses an internal switch network and fractional conversion ratios to achieve high efficiency and regulation over widely varying V_{IN} and output load conditions.

Internal control circuitry selects the appropriate conversion ratio based on V_{IN} and load conditions. The device has three possible conversion modes: 2:1 step-down mode, 1:1 step-down mode and 1:2 step-up mode. Only one external flying capacitor is needed to operate in all three modes. 2:1 mode is chosen when V_{IN} is greater than two times the desired V_{OUT}. 1:1 mode is chosen when V_{IN} falls between two times V_{OUT} and V_{OUT}. 1:2 mode is chosen when V_{IN} falls below the desired V_{OUT}. An internal load current sense circuit controls the switch point of the conversion ratio as needed to maintain output regulation over all load conditions.

Regulation is achieved by sensing the output voltage and regulating the amount of charge transferred per cycle. This method of regulation provides much lower input and output ripple than that of conventional switched capacitor charge pumps. The constant frequency charge transfer also makes additional output or input filtering much less demanding than conventional switched capacitor charge pumps.

The LTC3245 has a Burst Mode operation pin that allows the user to trade output ripple for better efficiency/lower quiescent current. The device has two SEL pins that select the output regulation (fixed 5V, fixed 3.3V or adjustable) as well as shutdown. The device includes soft-start function to limit in-rush current at startup. The device is also short-circuit and overtemperature protected.

V_{OUT} Regulation and Mode Selection

As shown in the Simplified Block Diagram, the device uses a control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output charge storage capacitor. As the load on V_{OUT} increases, V_{OUT} will drop slightly increasing the amount of charge transferred until the output current matches the output load. This method of regulation applies regardless of the conversion ratio.

The optimal conversion ratio is chosen based on V_{IN}, V_{OUT} and output load conditions. Two internal comparators are used to select the default conversion ratio. Each comparator has an adjustable offset built in that increases (decreases) in proportion to the increasing (decreasing) output load current. In this manner, the conversion ratio switch point is optimized to provide peak efficiency over all supply and load conditions while maintaining regulation. Each comparator also has built-in hysteresis to reduce the tendency of oscillating between modes when a transition point is reached.

Low Noise vs Burst Mode Operation

Burst Mode operation is selected by driving the $\overline{BURST}$ pin low. In Burst Mode operation the LTC3245 delivers a minimum amount of charge each cycle forcing V_{OUT} above regulation at light output loads. When the LTC3245 detects that V_{OUT} is above regulation the device stops charge transfer and goes into a low current sleep state. During this sleep state, the output load is supplied by the output capacitor. The device will remain in the sleep state until the output drops enough to require another burst of charge. Burst Mode operation allows the LTC3245 to achieve high efficiency even at light loads. If the output load exceeds the minimum charge transferred per cycle, then the device will operate continuously to maintain regulation.

Unlike traditional charge pumps who's burst current is dependant on many factors (i.e., supply, switch strength, capacitor selection, etc.), the LTC3245 burst current is regulated which helps to keep burst output ripple voltage relatively constant and is typically 50mV for C_{OUT} = 10µF.

Driving the $\overline{BURST}$ pin high puts the LTC3245 in low noise operation. In low noise operation the minimum amount of charge delivered each cycle and sleep hysteresis are reduced compared to Burst Mode operation. This results in lower burst output ripple (typically 20mV for C_{OUT} = 10µF) and will transition to constant frequency operation at lighter loads.

APPLICATIONS INFORMATION

Short-Circuit/Thermal Protection

The LTC3245 has built-in short-circuit current limiting as well as overtemperature protection. During short-circuit conditions the device will automatically limit the output current.

The LTC3245 has thermal protection that will shut down the device if the junction temperature exceeds the overtemperature threshold (typically 175°C). Thermal shutdown is included to protect the IC in cases of excessively high ambient temperatures, or in cases of excessive power dissipation inside the IC. The charge transfer will reactivate once the junction temperature drops back to approximately 165°C.

When the thermal protection is active, the junction temperature is beyond the specified operating range. Thermal protection is intended for momentary overload conditions outside normal operation. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Soft-Start Operation

To prevent excessive current flow at V_{IN} during start-up, the LTC3245 has built-in soft-start circuitry. Soft-start is achieved by increasing the amount of current available to the output charge storage capacitor linearly over a period of approximately 500µs. Soft-start is enabled whenever the device is brought out of shutdown, and is disabled shortly after regulation is achieved.

Programming the Output Voltage (OUTS/ADJ Pin)

The LTC3245 output voltage programming is very flexible offering a fixed 3.3V output, fixed 5V output as well as adjustable output that is programmed through an external resistor divider. The desired output regulation method is selected through the SET pins.

For a fixed output simply short OUTS (OUTS/ADJ pin) to V_{OUT} as shown in Figure 1. Fixed 3.3V operation is enabled by driving both SEL1 and SEL2 pins high, while fixed 5V operating is selected by driving SEL2 high with SEL1 low. Driving both SEL1 and SEL2 low shuts down the device causing V_{OUT} to go high impedance.

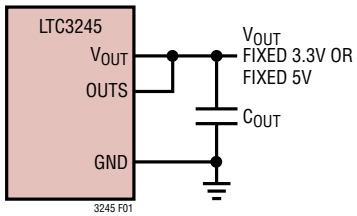


Figure 1: Fixed Output Operation

Adjustable output programming is accomplished by connecting ADJ (OUTS/ADJ pin) to a resistor divider between V_{OUT} and GND as shown in Figure 2. Adjustable operation is enabled by driving SEL1 high and SEL2 low. Driving both SEL1 and SEL2 low shuts down the device causing V_{OUT} to go high impedance.

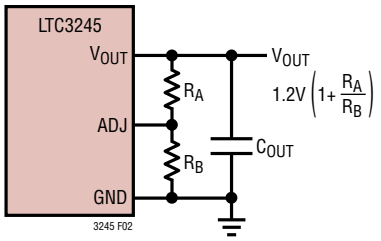


Figure 2: Adjustable Output Operation

Using adjustable operation the output (V_{OUT}) can be programmed to regulate from 2.5V to 5V. The limited programming range provides the required V_{OUT} operating voltage without overstressing the V_{OUT} pin.

The desired adjustable output voltage is programmed by solving the following equation for R_A and R_B:

$$\frac{R_A}{R_B} = \frac{V_{OUT}}{1.2V} - 1$$

Select a value for R_B in the range of 1k to 1M and solve for R_A. Note that the resistor divider current adds to the total no load operating current. Thus a larger value for R_B will result in lower operating current.

APPLICATIONS INFORMATION

2:1 Step-Down Charge Pump Operation

When the input supply is greater than about two times the output voltage, the LTC3245 will operate in 2:1 step-down mode. Charge transfer happens in two phases. On the first phase the flying capacitor (C_{FLY}) is connected between V_{IN} and V_{OUT}. On this phase C_{FLY} is charged up and current is delivered to V_{OUT}. On the second phase the flying capacitor (C_{FLY}) is connected between V_{OUT} and GND. The charge stored on C_{FLY} during the first phase is transferred to V_{OUT} on the second phase. When in 2:1 step-down mode the input current will be approximately half of the total output current. The efficiency (η) and chip power dissipation (P_D) in 2:1 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \frac{1}{2} I_{OUT}} = \frac{2V_{OUT}}{V_{IN}}$$

$$P_D = \left(\frac{V_{IN}}{2} - V_{OUT}\right) I_{OUT}$$

1:1 Step-Down Charge Pump Operation

When the input supply is less than about two times the output voltage but more than the programmed output voltage, the LTC3245 will operate in 1:1 step-down mode. This method of regulation is very similar to a linear regulator. Charge is delivered directly from V_{IN} to V_{OUT} through most of the oscillator period. The charge transfer is briefly interrupted at the end of the period. The interruption in charge transfer improves stability and transient response. When in 1:1 step-down mode the input current will be approximately equal to the total output current. Thus efficiency (η) and chip power dissipation (P_D) in 1:1 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet I_{OUT}} = \frac{V_{OUT}}{V_{IN}}$$

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT}$$

1:2 Step-Up Charge Pump Operation

When the input supply is less than the output voltage the LTC3245 will operate in 1:2 step-up mode. Charge transfer happens in two phases. On the first phase the flying capacitor (C_{FLY}) is connected between V_{IN} and GND. On this phase C_{FLY} is charged up. On the second phase the flying capacitor (C_{FLY}) is connected between V_{IN} and V_{OUT} and the charge stored on C_{FLY} during the first phase is transferred to V_{OUT}. When in 1:2 step-up mode the input current will be approximately twice the total output current. Thus efficiency (η) and chip power dissipation (P_D) in 1:2 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet 2\, I_{OUT}} = \frac{V_{OUT}}{2V_{IN}}$$

$$P_D = (2V_{IN} - V_{OUT})\, I_{OUT}$$

Due to the limited drive in 1:2 step-up mode the device always operates in Burst Mode operation when operating at this conversion ratio. This is done to delay the onset of dropout at the expense of more output ripple.

PGOOD Output Operation

The LTC3245 includes an open-drain power good (PGOOD) output pin. If the chip is in shutdown or under UVLO conditions (V_{IN} < 2.2V typical), PGOOD is low impedance to ground. PGOOD becomes high impedance when V_{OUT} rises to 95% (typical) of its regulation voltage. PGOOD stays high impedance until V_{OUT} is shut down or drops below the PGOOD threshold (91% typical) due to an overload condition. A pull-up resistor can be inserted between PGOOD and a low voltage positive logic supply (such as V_{OUT}) to signal a valid power good condition. The use of a large pull-up resistor on PGOOD and a capacitor placed between PGOOD and GND can be used to delay the PGOOD signal if desired.

V_{OUT} Ripple and Capacitor Selection

The type and value of capacitors used with the LTC3245 determine several important parameters such as regulator control loop stability, output ripple and charge pump

APPLICATIONS INFORMATION

strength. The value of C_{OUT} directly controls the amount of output ripple for a given load current when operating in constant frequency mode. Increasing the size of C_{OUT} will reduce the output ripple.

To reduce output noise and ripple, it is suggested that a low ESR (equivalent series resistance < 0.1Ω) ceramic capacitor (10µF or greater) be used for C_{OUT}. Tantalum and aluminum capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but are not recommended to be used alone because of their high ESR.

Both the style and value of C_{OUT} can significantly affect the stability of the LTC3245. As shown in the Block Diagram, the device uses a control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output charge storage capacitor. The charge storage capacitor also serves to form the dominant pole for the control loop. To prevent ringing or instability it is important for the output capacitor to maintain at least 4µF of capacitance over all conditions (see Ceramic Capacitor Selection Guidelines).

Likewise excessive ESR on the output capacitor will tend to degrade the loop stability of the LTC3245. The closed loop output resistance of the device is designed to be 0.3Ω for a 5V output and 0.2Ω for a 3.3V output. For a 250mA load current change, the output voltage will change by about 1.5%V. If the output capacitor has more ESR than the closed loop impedance, the closed loop frequency response will cease to roll off in a simple 1-pole fashion and poor load transient response or instability could result. Ceramic capacitors typically have exceptional ESR performance, and combined with a tight board layout, should yield excellent stability and load transient performance.

V_{IN} Capacitor Selection

The constant frequency architecture used by the LTC3245 makes input noise filtering much less demanding than with conventional regulated charge pumps. Depending on the mode of operation the input current of the LTC3245 can vary from I_{OUT} to 0mA on a cycle-by-cycle basis. Low ESR will reduce the voltage steps caused by changing input current, while the absolute capacitor value will determine the level of ripple. The total amount and type of capacitance necessary for input bypassing is very dependant on the applied source impedance as well as existing bypassing already on the V_{IN} node. For optimal input noise and ripple reduction, it is recommended that a low ESR ceramic capacitor be used for C_{IN} bypassing. An electrolytic or tantalum capacitor may be used in parallel with the ceramic capacitor on C_{IN} to increase the total capacitance, but due to the higher ESR it is not recommended that an electrolytic or tantalum capacitor be used alone for input bypassing. The LTC3245 will operate with capacitors less than 1µF but depending on the source impedance input noise can feed through to the output causing degraded performance. For best performance 1µF or greater total capacitance is suggested for C_{IN}.

Flying Capacitor Selection

Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitors since the voltage can reverse upon start-up of the LTC3245. Ceramic capacitors should always be used for the flying capacitors. The flying capacitors control the strength of the charge pump. In order to achieve the rated output current, it is necessary for the flying capacitor to have at least 0.4µF of capacitance over operating temperature with a bias voltage equal to the programmed V_{OUT} (see Ceramic Capacitor Selection Guidelines). If only 100mA or less of output current is required for the application, the flying capacitor minimum can be reduced to 0.15µF. The voltage rating of the ceramic capacitor should be V_{OUT} + 1V or greater.

Ceramic Capacitor Selection Guidelines

Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range (60% to 80% loss typical). Z5U and Y5V capacitors may also have a very strong voltage coefficient, causing them to lose an additional 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size

APPLICATIONS INFORMATION

rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 4.7µF, 10V, Y5V ceramic capacitor in an 0805 case may not provide any more capacitance than a 1µF, 10V, X5R or X7R available in the same 0805 case. In fact, over bias and temperature range, the 1µF, 10V, X5R or X7R will provide more capacitance than the 4.7µF, 10V, Y5V. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitance values are met over operating temperature and bias voltage. Below is a list of ceramic capacitor manufacturers and how to contact them:

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com

Layout Considerations

Due to the high switching frequency and transient currents produced by the LTC3245, careful board layout is necessary for optimal performance. A true ground plane and short connections to all capacitors will optimize performance, reduce noise and ensure proper regulation over all conditions.

When using the LTC3245 with an external resistor divider it is important to minimize any stray capacitance to the ADJ (OUTS/ADJ pin) node. Stray capacitance from ADJ to C^+ or C^- can degrade performance significantly and should be minimized and/or shielded if necessary.

Thermal Management

The on chip power dissipation in the LTC3245 will cause the junction to ambient temperature to rise at rate of 40°C/W or more. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the die paddle (Pin 13) with multiple vias to a large ground plane under the device can reduce the thermal resistance of the package and PC board considerably. Poor board layout and failure to connect the die paddle (Pin 13) to a large ground plane can result in thermal junction to ambient impedance well in excess of 40°C/W.

Because of the wide input operating range it is possible to exceed the specified operating junction temperature and even reach thermal shutdown. Figure 3 shows the available output current vs temperature to ensure the 150°C operating junction temperature is not exceed for input voltages less than 20V.

Figure 3 assumes worst-case operating conditions. Under some operating conditions the part can supply more current than shown without exceeding the 150°C operating junction temperature. When operating outside the constraints of Figure 3 it is the responsibility of the user to calculate worst-case operating conditions (temperature and power) to make sure the LTC3245's specified operating junction temperature is not exceeded for extended periods of time. The 2:1 Step-Down, 1:1 Step-Down, and 1:2 Step-Up Charge Pump Operation sections provide equations for calculating power dissipation (P_D) in each mode.

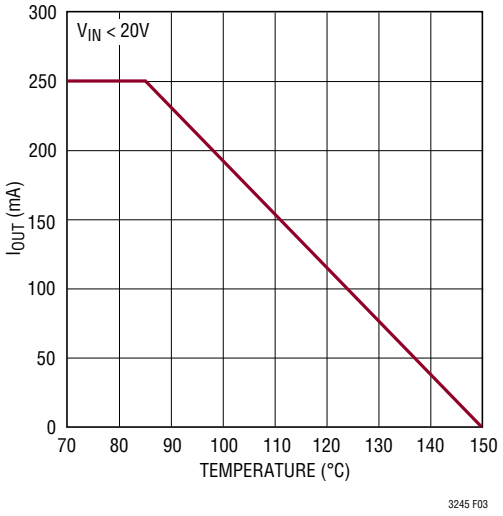


Figure 3. Available Output Current vs Temperature

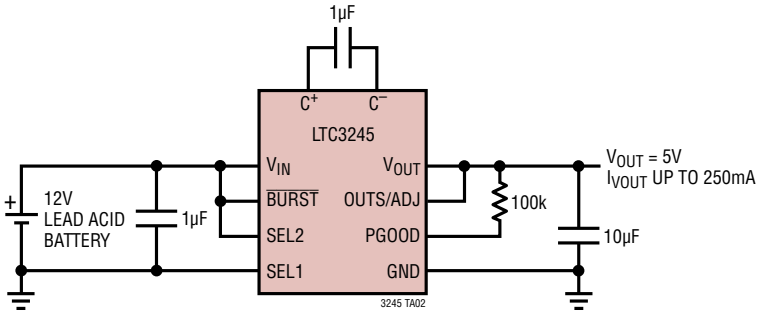
For example, if it is determined that the maximum power dissipation (P_D) is 1.2W under normal operation, then the junction to ambient temperature rise will be:

Junction to ambient = 1.2W • 40°C/W = 48°C

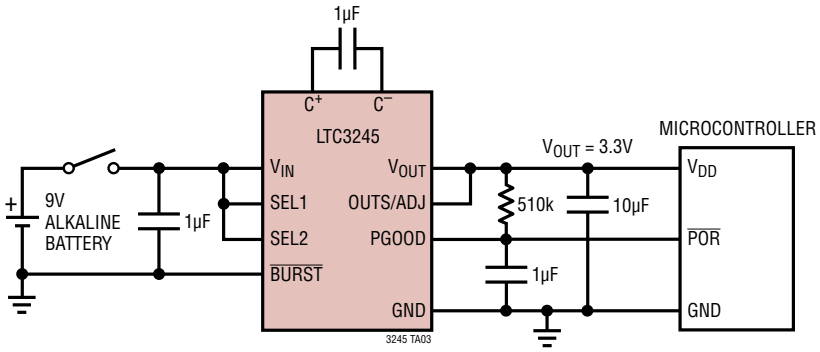
Thus, the ambient temperature under this condition cannot exceed 102°C if the junction temperature is to remain below 150°C and if the ambient temperature exceeds about 127°C the device will cycle in and out of the thermal shutdown.

TYPICAL APPLICATIONS

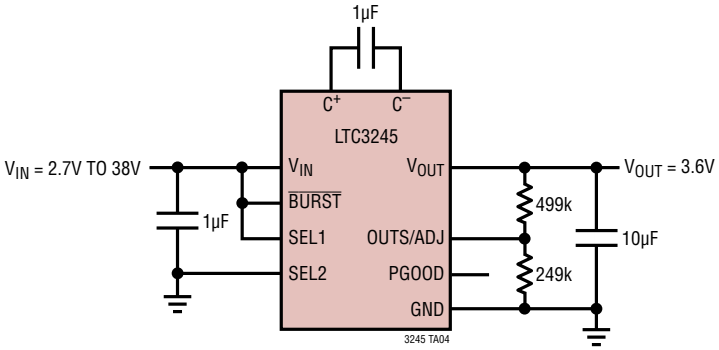
Regulated 5V Low Noise Output



High Efficiency 3.3V Microcontroller Supply from 9V Alkaline (with Power-On Reset Delay)



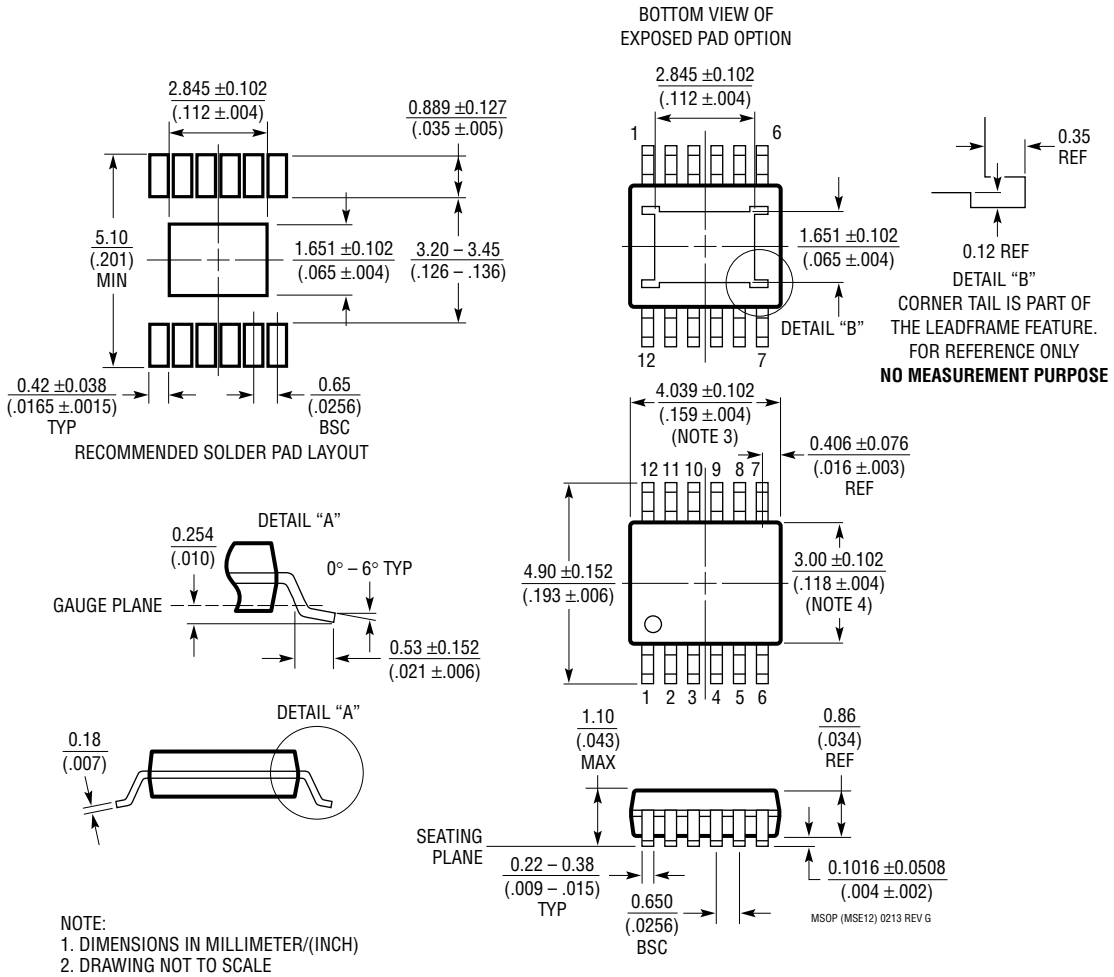
Wide Input Range Low Noise 3.6V Supply



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)

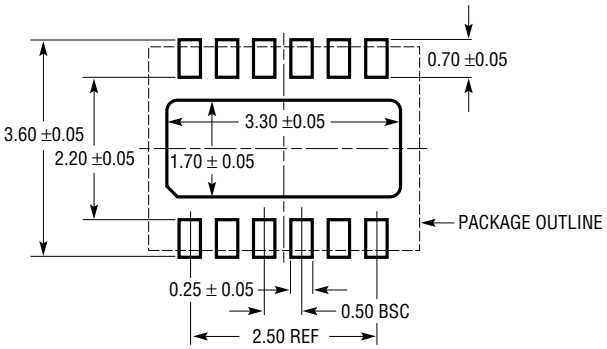


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

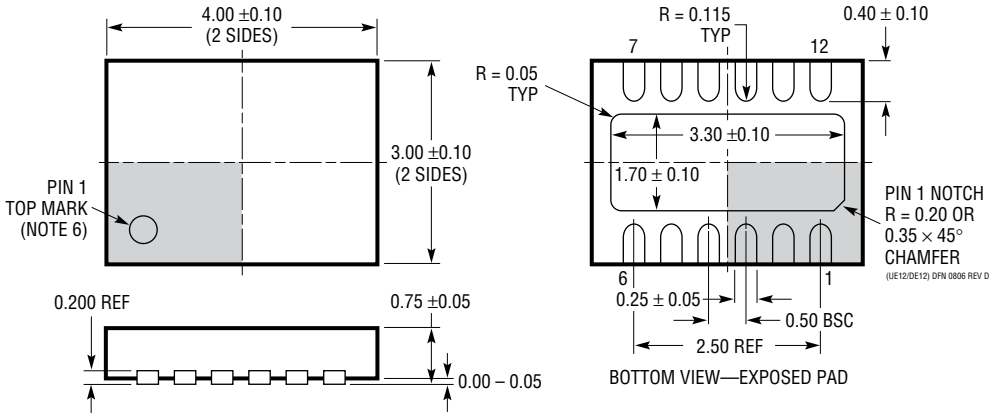
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



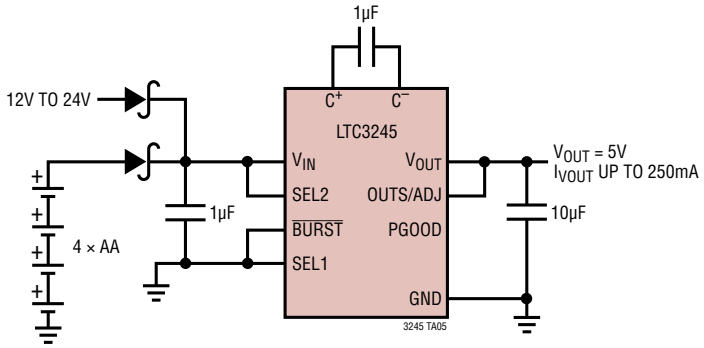
NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/13	Added MP-grade in MSOP package to Order Information table	2
		Modified Note 2 to add MP-grade	3

TYPICAL APPLICATION

Wide V_{IN} 5V Supply with Battery Backup



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1751-3.3/ LTC1751-5	100mA, 800kHz Regulated Doubler	V_{IN}: 2V to 5V, $V_{OUT(MAX)}$ = 3.3V/5V, I_Q = 20µA, I_{SD} < 2µA, MS8 Package
LTC1983-3/ LTC1983-5	100mA, 900kHz Regulated Inverter	V_{IN}: 3.3V to 5.5V, $V_{OUT(MAX)}$ = –3V/–5V, I_Q = 25µA, I_{SD} < 2µA, ThinSOT™ Package
LTC3200-5	100mA, 2MHz Low Noise, Doubler/ White LED Driver	V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5V, I_Q = 3.5mA, I_{SD} < 1µA, ThinSOT Package
LTC3202	125mA, 1.5MHz Low Noise, Fractional White LED Driver	V_{IN}: 2.7V to 4.5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 2.5mA, I_{SD} < 1µA, DFN, MS Packages
LTC3204-3.3/ LTC3204B-3.3/ LTC3204-5/ LTC3204B-5	Low Noise, Regulated Charge Pumps in (2mm × 2mm) DFN Package	V_{IN}: 1.8V to 4.5V (LTC3204B-3.3), 2.7V to 5.5V (LTC3204B-5), I_Q = 48µA, B Version without Burst Mode Operation, 6-Lead (2mm × 2mm) DFN Package
LTC3440	600mA (I_{OUT}) 2MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, 10-Lead MS Package
LTC3441	High Current Micropower 1MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, DFN Package
LTC3443	High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 28µA, I_{SD} < 1µA, DFN Package
LTC3240-3.3/ LTC3240-2.5	3.3V/2.5V Step-Up/Step-Down Charge Pump DC/DC Converter	V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 3.3V / 2.5V, I_Q = 65µA, I_{SD} < 1µA, (2mm × 2mm) DFN Package
LTC3260	Low Noise Dual Supply Inverting Charge Pump	V_{IN} Range: 4.5V to 32V, I_Q = 100µA, 100mA Charge Pump, 50mA Positive LDO, 50mA Negative LDO
LTC3261	High Voltage Low I_Q Inverting Charge Pump	V_{IN} Range: 4.5V to 32V, I_Q = 60µA, 100mA Charge Pump

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