

# LTC2302/LTC2306

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V <sub>DD</sub> , OV <sub>DD</sub> ) .....	–0.3V to 6V	Digital Output Voltage ... (GND – 0.3V) to (OV <sub>DD</sub> + 0.3V)	
Analog Input Voltage (Note 3)		Power Dissipation .....	500mW
CH0(IN <sup>+</sup> )-CH1(IN <sup>–</sup> ),		Operating Temperature Range	
REF .....	(GND – 0.3V) to (V <sub>DD</sub> + 0.3V)	LTC2302C/LTC2306C .....	0°C to 70°C
Digital Input Voltage		LTC2302I/LTC2306I .....	–40°C to 85°C
(Note 3) .....	(GND – 0.3V) to (V <sub>DD</sub> + 0.3V)	Storage Temperature Range .....	–65°C to 150°C

## PIN CONFIGURATION

<p>LTC2302 TOP VIEW</p> <p>SDO [1] <math>OV_{DD}</math> [10] CONVST [2] SCK [9] <math>V_{DD}</math> [3] SDI [8] <math>IN^+</math> [4] GND [7] <math>IN^-</math> [5] <math>V_{REF}</math> [6]</p> <p>DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN <math>T_{JMAX} = 150^{\circ}C</math>, <math>\theta_{JA} = 43^{\circ}C/W</math> EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB</p>	<p>LTC2306 TOP VIEW</p> <p>SDO [1] <math>OV_{DD}</math> [10] CONVST [2] SCK [9] <math>V_{DD}</math> [3] SDI [8] CH0 [4] GND [7] CH1 [5] <math>V_{REF}</math> [6]</p> <p>DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN <math>T_{JMAX} = 150^{\circ}C</math>, <math>\theta_{JA} = 43^{\circ}C/W</math> EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB</p>
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## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2302CDD#PBF	LTC2302CDD#TRPBF	LDGV	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2302IDD#PBF	LTC2302IDD#TRPBF	LDGV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2306CDD#PBF	LTC2306CDD#TRPBF	LDGW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2306IDD#PBF	LTC2306IDD#TRPBF	LDGW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

**CONVERTER AND MULTIPLEXER CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Notes 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 6)	●		$\pm 0.3$	$\pm 1$	LSB
Differential Linearity Error		●		$\pm 0.25$	$\pm 1$	LSB
Bipolar Zero Error	(Note 7)	●		$\pm 1$	$\pm 6$	LSB
Bipolar Zero Error Drift				0.002		LSB/ $^\circ\text{C}$
Unipolar Zero Error	(Note 7)	●		$\pm 1$	$\pm 6$	LSB
Unipolar Zero Error Drift				0.002		LSB/ $^\circ\text{C}$
Unipolar Zero Error Match (LTC2306)				$\pm 0.3$	$\pm 3$	LSB
Bipolar Full-Scale Error	(Note 8)	●		$\pm 1.5$	$\pm 8$	LSB
Bipolar Full-Scale Error Drift				0.05		LSB/ $^\circ\text{C}$
Unipolar Full-Scale Error	(Note 8)	●		$\pm 1.2$	$\pm 6$	LSB
Unipolar Full-Scale Error Drift				0.05		LSB/ $^\circ\text{C}$
Unipolar Full-Scale Error Match (LTC2306)				$\pm 0.3$	$\pm 3$	LSB

**ANALOG INPUT**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}^+$	Absolute Input Range (CH0, CH1, $IN^+$ )	(Note 9)	●	-0.05		$V_{REF}$	V
$V_{IN}^-$	Absolute Input Range (CH0, CH1, $IN^-$ )	Unipolar (Note 9)	●	-0.05		$0.25 \cdot V_{REF}$	V
		Bipolar (Note 9)	●	-0.05		$0.75 \cdot V_{REF}$	V
$V_{IN}^+ - V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ - V_{IN}^-$ (Unipolar)	●		0 to $V_{REF}$		V
		$V_{IN} = V_{IN}^+ - V_{IN}^-$ (Bipolar)	●		$\pm V_{REF}/2$		V
$I_{IN}$	Analog Input Leakage Current		●			$\pm 1$	$\mu\text{A}$
$C_{IN}$	Analog Input Capacitance	Sample Mode			55		pF
		Hold Mode			5		pF
CMRR	Input Common Mode Rejection Ratio				70		dB

**REFERENCE INPUT**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	$V_{REF}$ Input Range		●	0.1		$V_{DD}$	V
$I_{REF}$	Reference Input Current	$f_{SAMPL} = 0\text{ksps}$ , $V_{REF} = 4.096\text{V}$	●		50	80	$\mu\text{A}$
		$f_{SAMPL} = 500\text{ksps}$ , $V_{REF} = 4.096\text{V}$	●		230	260	$\mu\text{A}$
$C_{REF}$	Reference Input Capacitance				55		pF

**DYNAMIC ACCURACY**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$ . (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 1\text{kHz}$	●	71	72.8		dB
SNR	Signal-to-Noise Ratio	$f_{IN} = 1\text{kHz}$	●	71	73.2		dB
THD	Total Harmonic Distortion	$f_{IN} = 1\text{kHz}$ , First 5 Harmonics	●		-88	-78	dB
SFDR	Spurious Free Dynamic Range	$f_{IN} = 1\text{kHz}$	●	79	89		dB
	Channel-to-Channel Isolation	$f_{IN} = 1\text{kHz}$			-109		dB
	Full Linear Bandwidth	(Note 11)			700		kHz
	-3dB Input Linear Bandwidth				25		MHz
	Aperture Delay				13		ns
	Transient Response	Full-Scale Step			240		ns

**DIGITAL INPUTS AND DIGITAL OUTPUTS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IH}$	High Level Input Voltage	$V_{DD} = 5.25\text{V}$	●	2.4			V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 4.75\text{V}$	●			0.8	V
$I_{IN}$	High Level Input Current	$V_{IN} = V_{DD}$	●			$\pm 10$	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance				5		pF
$V_{OH}$	High Level Output Voltage	$OV_{DD} = 4.75\text{V}$ , $I_{OUT} = -10\mu\text{A}$ $OV_{DD} = 4.75\text{V}$ , $I_{OUT} = -200\mu\text{A}$	●	4	4.74		V V
$V_{OL}$	Low Level Output Voltage	$OV_{DD} = 4.75\text{V}$ , $I_{OUT} = 160\mu\text{A}$ $OV_{DD} = 4.75\text{V}$ , $I_{OUT} = 1.6\text{mA}$	●		0.05	0.4	V V
$I_{OZ}$	Hi-Z Output Leakage	$V_{OUT} = 0\text{V}$ to $OV_{DD}$ , CONVST High	●			$\pm 10$	$\mu\text{A}$
$C_{OZ}$	Hi-Z Output Capacitance	CONVST High			15		pF
$I_{SOURCE}$	Output Source Current	$V_{OUT} = 0\text{V}$			-10		mA
$I_{SINK}$	Output Sink Current	$V_{OUT} = OV_{DD}$			10		mA

**POWER REQUIREMENTS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{DD}$	Supply Voltage		●	4.75	5	5.25	V
$OV_{DD}$	Output Driver Supply Voltage		●	2.7		5.25	V
$I_{DD}$	Supply Current Sleep Mode	$C_L = 25\text{pF}$ CONVST = 5V, Conversion Done	● ●		2.8 7	3.5 15	mA $\mu\text{A}$
$P_D$	Power Dissipation Sleep Mode				14 35		mW $\mu\text{W}$

**TIMING CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$f_{\text{SMPL}}(\text{MAX})$	Maximum Sampling Frequency	●			500	kHz
$f_{\text{SCK}}$	Shift Clock Frequency	●			40	MHz
$t_{\text{WHCONV}}$	CONVST High Time	(Note 9) ●	20			ns
$t_{\text{HD}}$	Hold Time SDI After SCK↑	●	2.5			ns
$t_{\text{SDI}}$	Setup Time SDI Stable Before SCK↑	●	0			ns
$t_{\text{WHCLK}}$	SCK High Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$ ●	10			ns
$t_{\text{WLCLK}}$	SCK Low Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$ ●	10			ns
$t_{\text{WLCONVST}}$	CONVST Low Time During Data Transfer	(Note 9) ●	410			ns
$t_{\text{HCONVST}}$	Hold Time CONVST Low After Last SCK↓	(Note 9) ●	20			ns
$t_{\text{CONV}}$	Conversion Time	●		1.3	1.6	μs
$t_{\text{ACQ}}$	Acquisition Time	7th SCK↑ to CONVST↑ (Note 9) ●	240			ns
$t_{\text{dDO}}$	SDO Data Valid After SCK↓	$C_L = 25\text{pF}$ (Note 9) ●		10.8	12.5	ns
$t_{\text{hDO}}$	SDO Hold Time SCK↓	$C_L = 25\text{pF}$ ●	4			ns
$t_{\text{en}}$	SDO Valid After CONVST↓	$C_L = 25\text{pF}$ ●		11	15	ns
$t_{\text{dis}}$	Bus Relinquish Time	$C_L = 25\text{pF}$ ●		11	15	ns
$t_r$	SDO Rise Time	$C_L = 25\text{pF}$		4		ns
$t_f$	SDO Fall Time	$C_L = 25\text{pF}$		4		ns
$t_{\text{CYC}}$	Total Cycle Time			2		μs

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to ground with  $V_{\text{DD}}$  and  $OV_{\text{DD}}$  wired together (unless otherwise noted).

**Note 3:** When these pin voltages are taken below ground or above  $V_{\text{DD}}$ , they will be clamped by internal diodes. These products can handle input currents greater than 100mA below ground or above  $V_{\text{DD}}$  without latchup.

**Note 4:**  $V_{\text{DD}} = 5\text{V}$ ,  $OV_{\text{DD}} = 5\text{V}$ ,  $V_{\text{REF}} = 4.096\text{V}$ ,  $f_{\text{SMPL}} = 500\text{ksps}$ , unless otherwise specified.

**Note 5:** Linearity, offset and full-scale specifications apply for a single-ended analog input with respect to GND for the LTC2306 and  $\text{IN}^+$  with respect to  $\text{IN}^-$  tied to GND for the LTC2302.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** Bipolar zero error is the offset voltage measured from  $-0.5\text{LSB}$  when the output code flickers between 0000 0000 0000 and 1111 1111 1111. Unipolar zero error is the offset voltage measured from  $+0.5\text{LSB}$  when the output code flickers between 0000 0000 0000 and 0000 0000 0001.

**Note 8:** Full-scale bipolar error is the worst-case of  $-FS$  or  $+FS$  untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error.

**Note 9:** Guaranteed by design, not subject to test.

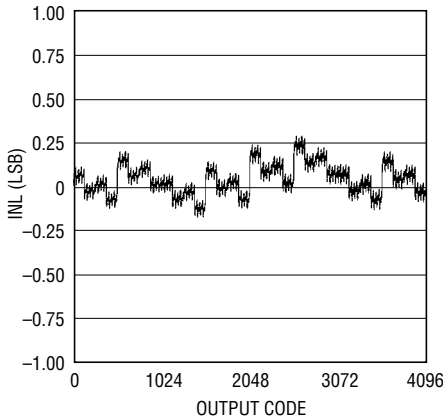
**Note 10:** All specifications in dB are referred to a full-scale  $\pm 2.048\text{V}$  input with a  $4.096\text{V}$  reference voltage.

**Note 11:** Full linear bandwidth is defined as the full-scale input frequency at which the SINAD degrades to 60dB or 10 bits of accuracy.

## TYPICAL PERFORMANCE CHARACTERISTICS

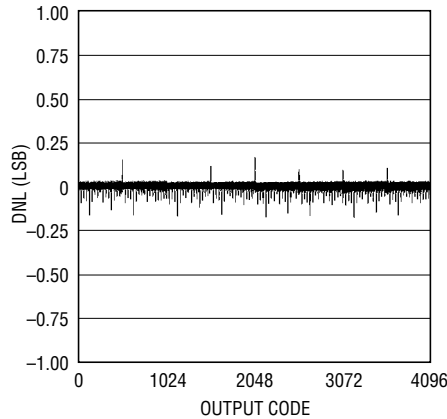
(LTC2302)  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 0V_{DD} = 5V$ ,  $V_{REF} = 4.096V$ ,  $f_{SAMPL} = 500\text{ksps}$ , unless otherwise noted.

**Integral Nonlinearity  
vs Output Code**



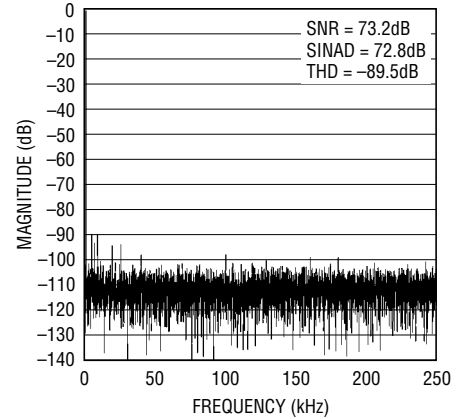
23026 G01

**Differential Nonlinearity  
vs Output Code**



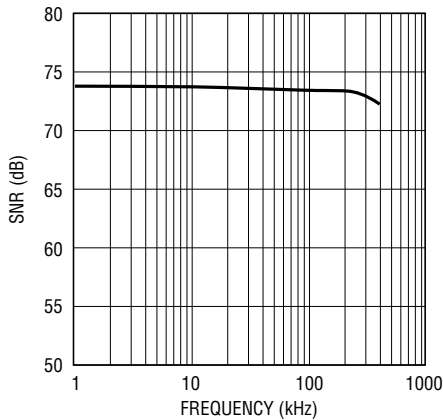
23026 G02

**1kHz Sine Wave  
8192 Point FFT Plot**



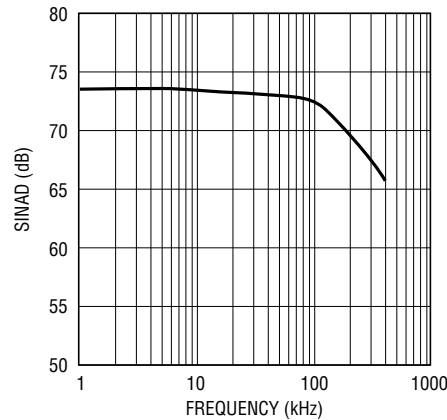
23026 G03

**SNR vs Input Frequency**



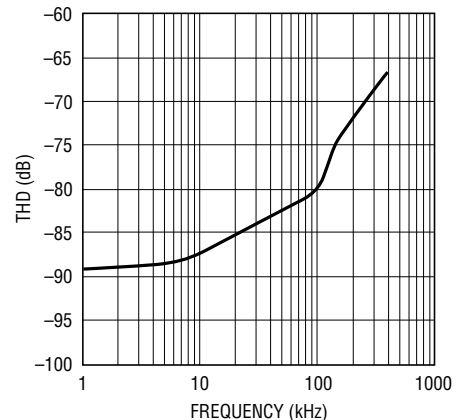
23026 G04

**SINAD vs Input Frequency**



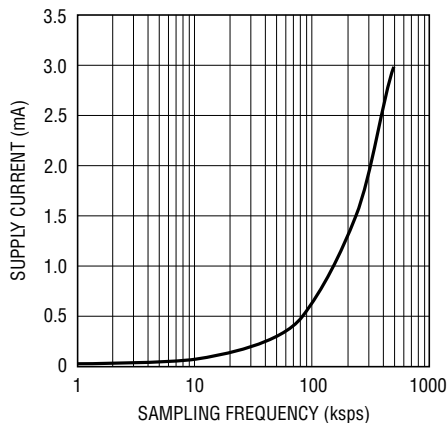
23026 G05

**THD vs Input Frequency**



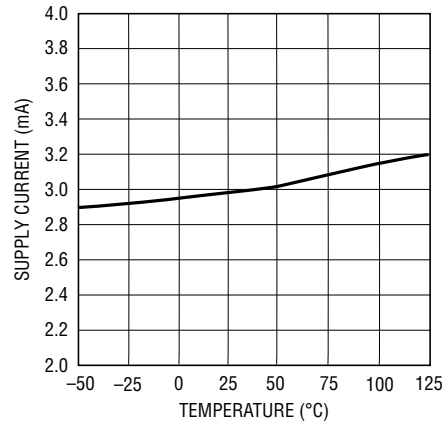
23026 G06

**Supply Current  
vs Sampling Frequency**



23026 G07

**Supply Current vs Temperature**

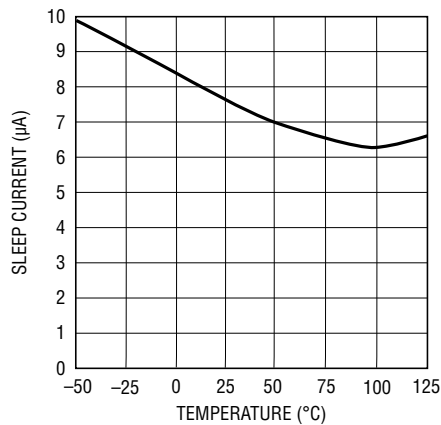


23026 G08

## TYPICAL PERFORMANCE CHARACTERISTICS

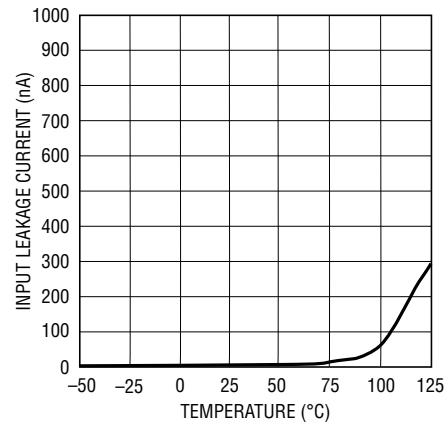
(LTC2302)  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 0\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{REF} = 4.096\text{V}$ ,  $f_{SAMPL} = 500\text{ksps}$ , unless otherwise noted.

Sleep Current vs Temperature



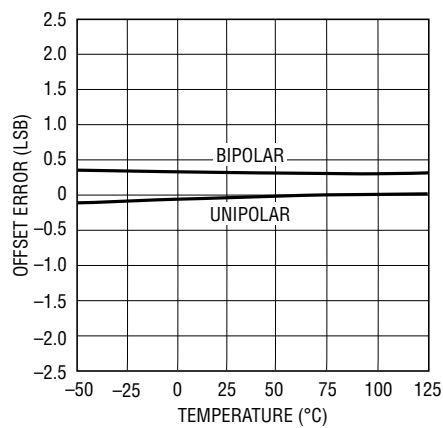
23026 G09

Analog Input Leakage Current vs Temperature



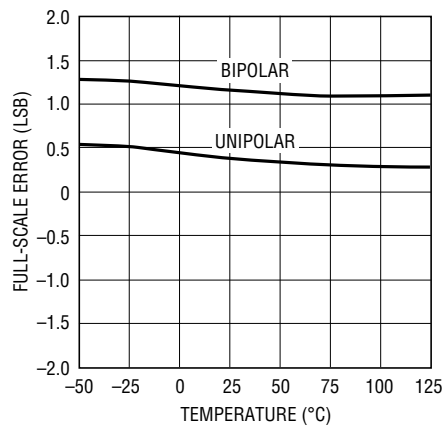
23026 G10

Offset Error vs Temperature



23026 G11

Full-Scale Error vs Temperature

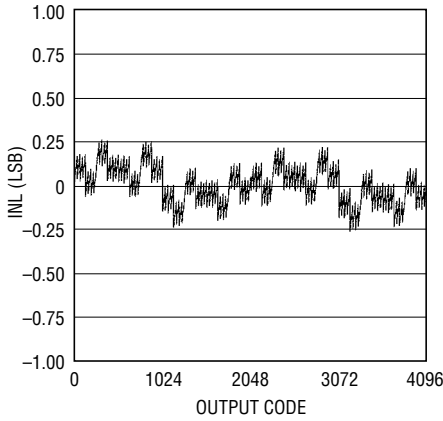


23026 G12

## TYPICAL PERFORMANCE CHARACTERISTICS

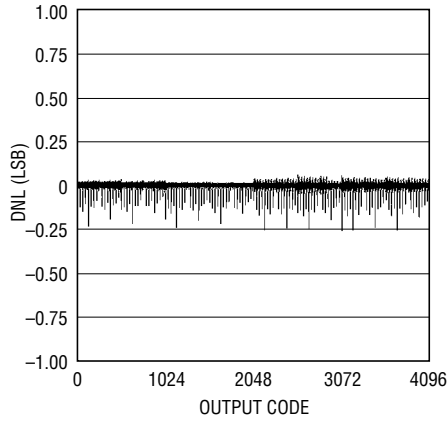
(LTC2306)  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 0V_{DD} = 5V$ ,  $V_{REF} = 4.096V$ ,  $f_{SAMPL} = 500\text{ksps}$ , unless otherwise noted.

**Integral Nonlinearity  
vs Output Code**



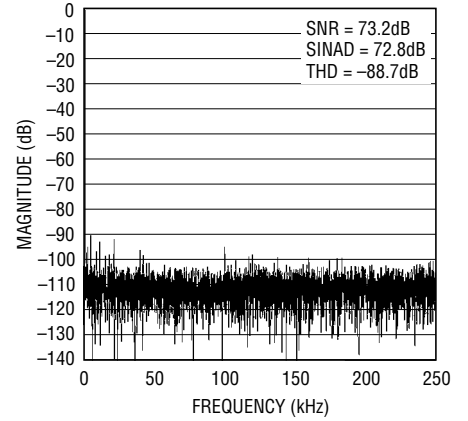
23026 G13

**Differential Nonlinearity  
vs Output Code**



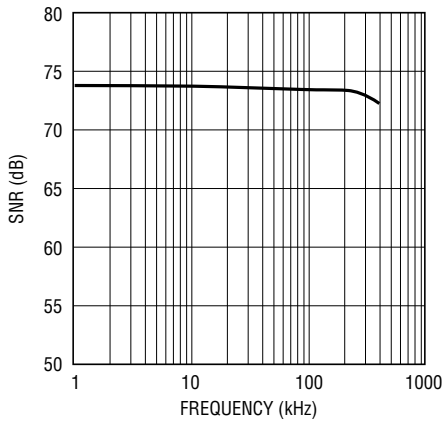
23026 G14

**1kHz Sine Wave  
8192 Point FFT Plot**



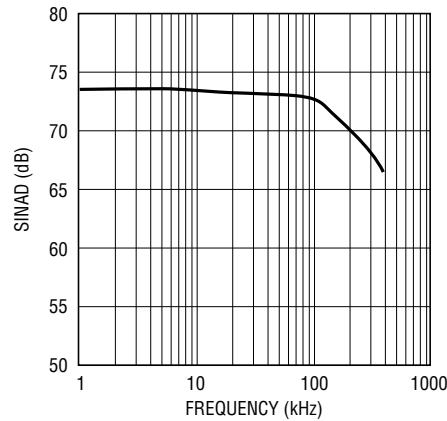
23026 G15

**SNR vs Input Frequency**



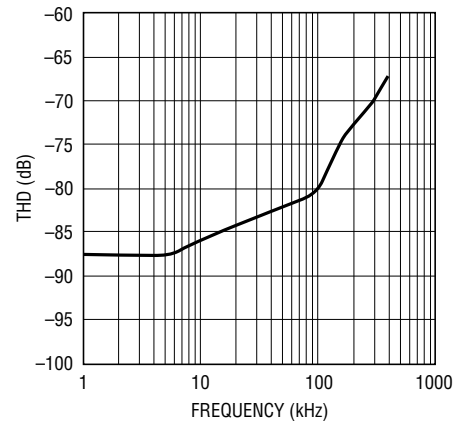
23026 G16

**SINAD vs Input Frequency**



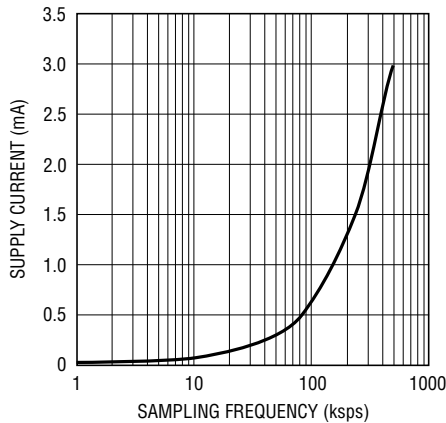
23026 G17

**THD vs Input Frequency**



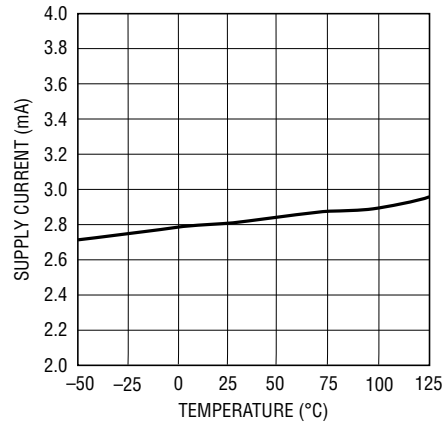
23026 G18

**Supply Current  
vs Sampling Frequency**



23026 G19

**Supply Current vs Temperature**



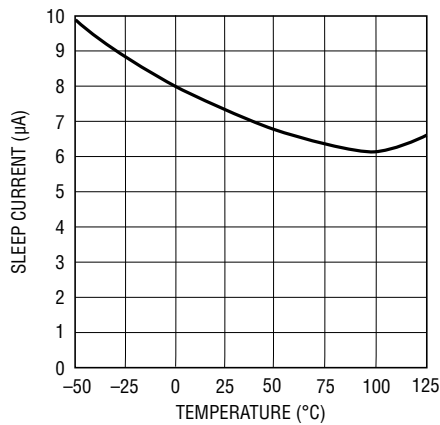
23026 G20

23026fb

## TYPICAL PERFORMANCE CHARACTERISTICS

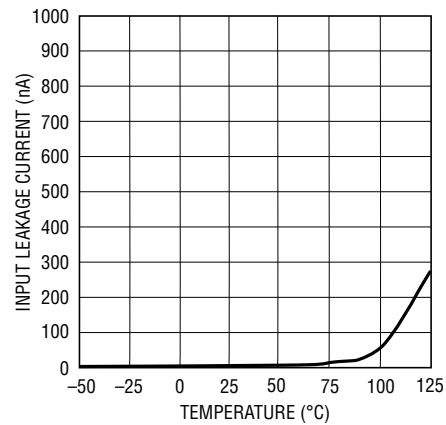
(LTC2306)  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 0V_{DD} = 5V$ ,  $V_{REF} = 4.096V$ ,  $f_{SAMPL} = 500\text{ksps}$ , unless otherwise noted.

**Sleep Current vs Temperature**



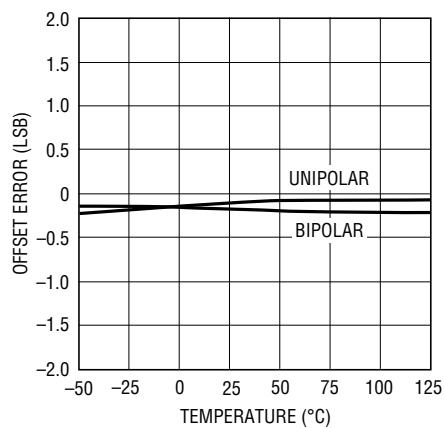
23026 G21

**Analog Input Leakage Current vs Temperature**



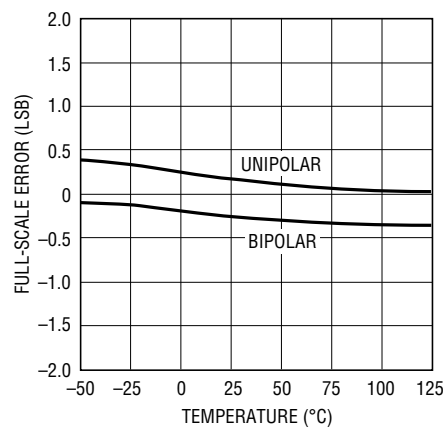
23026 G22

**Offset Error vs Temperature**



23026 G23

**Full-Scale Error vs Temperature**



23026 G24



## PIN FUNCTIONS

### LTC2302

**SDO (Pin 1):** Three-State Serial Data Out. SDO outputs the data from the previous conversion. SDO is shifted out serially on the falling edge of each SCK pulse. SDO is enabled by a low level on CONVST.

**CONVST (Pin 2):** Conversion Start. A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends.

**V<sub>DD</sub> (Pin 3):** 5V Supply. The range of V<sub>DD</sub> is 4.75V to 5.25V. Bypass V<sub>DD</sub> to GND with a 0.1μF ceramic capacitor and a 10μF tantalum capacitor in parallel.

**IN<sup>+</sup>, IN<sup>-</sup> (Pin 4, Pin 5):** Positive (IN<sup>+</sup>) and Negative (IN<sup>-</sup>) Differential Analog Inputs.

**V<sub>REF</sub> (Pin 6):** Reference Input. Connect an external reference at V<sub>REF</sub>. The range of the external reference is 0.1V to V<sub>DD</sub>. Bypass to GND with a minimum 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor.

**GND (Pin 7):** Ground. All GND pins must be connected to a solid ground plane.

**SDI (Pin 8):** Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses.

**SCK (Pin 9):** Serial Data Clock. SCK synchronizes the serial data transfer. The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK.

**OV<sub>DD</sub> (Pin 10):** Output Driver Supply. Bypass OV<sub>DD</sub> to GND with a 0.1μF ceramic capacitor close to the pin. The range of OV<sub>DD</sub> is 2.7V to 5.25V.

**Exposed Pad (Pin 11):** Exposed Pad Ground. Must be soldered directly to ground plane.

### LTC2306

**SDO (Pin 1):** Three-State Serial Data Out. SDO outputs the data from the previous conversion. SDO is shifted out serially on the falling edge of each SCK pulse. SDO is enabled by a low level on CONVST.

**CONVST (Pin 2):** Conversion Start. A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends.

**V<sub>DD</sub> (Pin 3):** 5V Supply. The range of V<sub>DD</sub> is 4.75V to 5.25V. Bypass V<sub>DD</sub> to GND with a 0.1μF ceramic capacitor and a 10μF tantalum capacitor in parallel.

**CH0, CH1 (Pin 4, Pin 5):** Channel 0 and Channel 1 Analog Inputs. CH0, CH1 can be configured as single-ended or differential input channels. See the Analog Input Multiplexer section.

**V<sub>REF</sub> (Pin 6):** Reference Input. Connect an external reference at V<sub>REF</sub>. The range of the external reference is 0.1V to V<sub>DD</sub>. Bypass to GND with a minimum 10μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor.

**GND (Pin 7):** Ground. All GND pins must be connected to a solid ground plane.

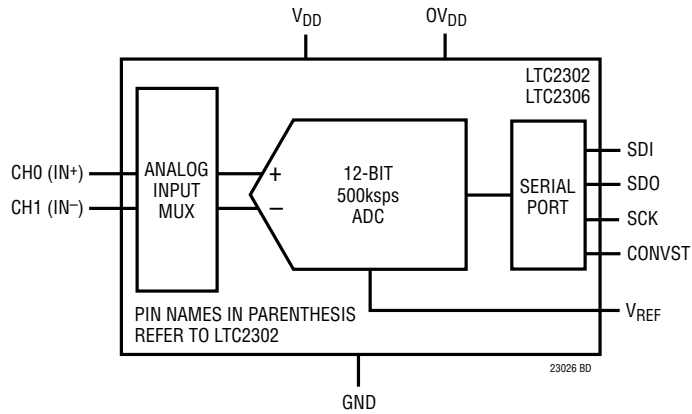
**SDI (Pin 8):** Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses.

**SCK (Pin 9):** Serial Data Clock. SCK synchronizes the serial data transfer. The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK.

**OV<sub>DD</sub> (Pin 10):** Output Driver Supply. Bypass OV<sub>DD</sub> to OGND with a 0.1μF ceramic capacitor close to the pin. The range of OV<sub>DD</sub> is 2.7V to 5.5V.

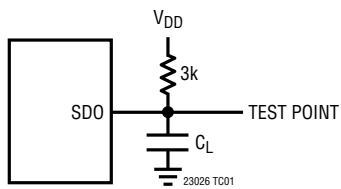
**Exposed Pad (Pin 11):** Exposed Pad Ground. Must be soldered directly to ground plane.

## BLOCK DIAGRAM

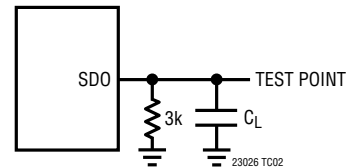


## TEST CIRCUITS

Load Circuit for  $t_{dis}$  Waveform 1

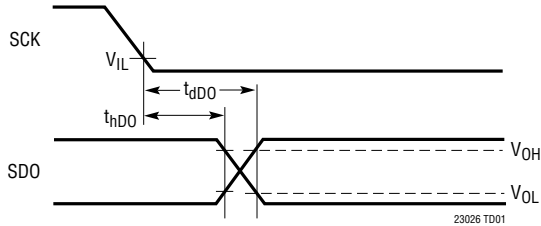


Load Circuit for  $t_{dis}$  Waveform 2,  $t_{en}$

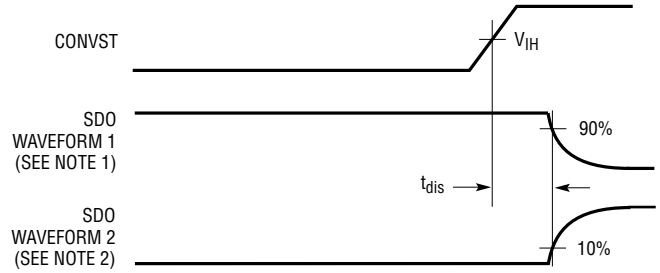


## TIMING DIAGRAMS

Voltage Waveforms for SDO Delay Times,  $t_{dDO}$  and  $t_{hDO}$



Voltage Waveforms for  $t_{dis}$

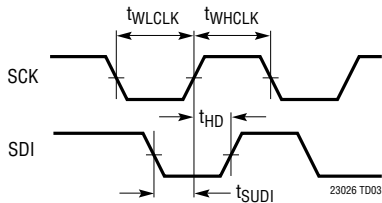


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

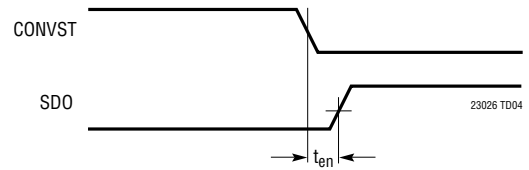
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

23026 TD02

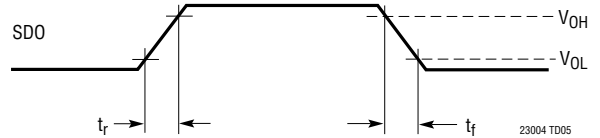
$t_{WLCLK}$  (SCK Low Time)  
 $t_{WHCLK}$  (SCK High Time)  
 $t_{HD}$  (Hold Time SDI After SCK↑)  
 $t_{SUDI}$  (Setup Time SDI Stable Before SCK↑)



Voltage Waveforms for  $t_{en}$



Voltage Waveforms for SDO Rise and Fall Times  $t_r$ ,  $t_f$



## APPLICATIONS INFORMATION

### Overview

The LTC2302/LTC2306 are low noise, 500ksps, 1-/2-channel, 12-bit successive approximation register (SAR) A/D converters. The LTC2306 includes a 2-channel analog input multiplexer (MUX) while the LTC2302 includes an input MUX that allows the polarity of the differential input to be selected. Both ADCs include an SPI-compatible serial port for easy data transfers and can operate in either unipolar or bipolar mode. Unipolar mode should be used for single-ended operation with the LTC2306, since single-ended input signals are always referenced to GND. The LTC2302/LTC2306 can be put into a power-down sleep mode during idle periods to save power.

Conversions are initiated by a rising edge on the CONVST input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, a 6-bit input word ( $D_{IN}$ ) at the SDI input configures the MUX and programs various modes of operation. As the  $D_{IN}$  bits are shifted in, data from the previous conversion is shifted out on SDO. After the 6 bits of the  $D_{IN}$  word have been shifted in, the ADC begins acquiring the analog input in preparation for the next conversion as the rest of the data is shifted out. The acquire phase requires a minimum time of 240ns for the sample-and-hold capacitors to acquire the analog input signal.

During the conversion, the internal 12-bit capacitive charge-redistribution DAC output is sequenced through a successive approximation algorithm by the SAR starting

from the most significant bit (MSB) to the least significant bit (LSB). The sampled input is successively compared with binary weighted charges supplied by the capacitive DAC using a differential comparator. At the end of a conversion, the DAC output balances the analog input. The SAR contents (a 12-bit data word) that represent the sampled analog input are loaded into 12 output latches that allow the data to be shifted out.

### Programming the LTC2306 and LTC2302

The software compatible LTC2302/LTC2306/LTC2308 family features a 6-bit  $D_{IN}$  word to program various modes of operation. Don't care bits (X) are ignored. The SDI data bits are loaded on the rising edge of SCK, with the S/D bit loaded on the first rising edge (see Figure 6 in the Timing and Control section). The input data word for the LTC2306 is defined as follows:

S/D	O/S	X	X	UNI	X
-----	-----	---	---	-----	---

S/D = SINGLE-ENDED/DIFFERENTIAL BIT

O/S = ODD/SIGN BIT

UNI = UNIPOLAR/BIPOLAR BIT

X = DON'T CARE

For the LTC2302, the input data word is defined as:

X	O/S	X	X	UNI	X
---	-----	---	---	-----	---

APPLICATIONS INFORMATION

Analog Input Multiplexer

The analog input MUX is programmed by the S/D and O/S bits of the D<sub>IN</sub> word for the LTC2306 and the O/S bit of the D<sub>IN</sub> word for the LTC2302. Table 1 and Table 2 list MUX configurations for all combinations of the configuration bits. Figure 1a shows several possible MUX configurations and Figure 1b shows how the MUX can be reconfigured from one conversion to the next.

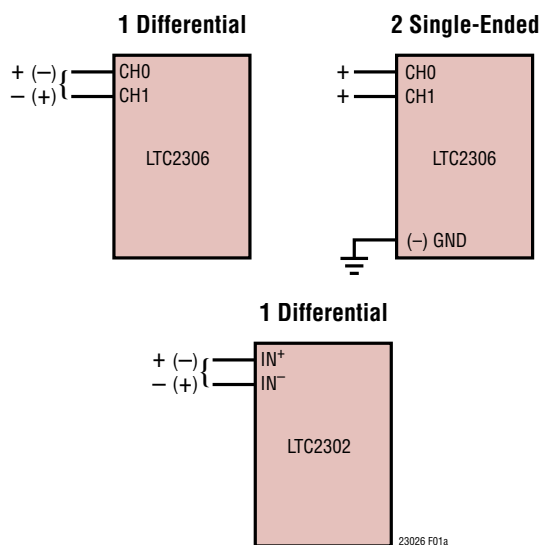


Figure 1a. Example MUX Configurations

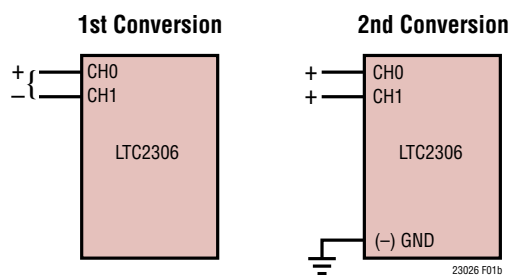


Figure 1b. Changing the MUX Assignment “On the Fly”

Table 1. Channel Configuration for the LTC2306

S/D	O/S	CH0	CH1
0	0	+	-
0	1	-	+
1	0	+	
1	1		+

WITH RESPECT TO GND

NOTE: UNIPOLAR MODE SHOULD BE USED FOR SINGLE-ENDED OPERATION, SINCE INPUT SIGNALS ARE ALWAYS REFERENCED TO GND

Table 2. Channel Configuration for the LTC2302

O/S	IN+	IN-
0	+	-
1	-	+

Driving the Analog Inputs

The analog inputs of the LTC2302/LTC2306 are easy to drive. Each of the analog inputs of the LTC2306 (CHO and CH1) can be used as a single-ended input relative to GND or as a differential pair. The analog inputs of the LTC2302 (IN<sup>+</sup>, IN<sup>-</sup>) are always configured as a differential pair. Regardless of the MUX configuration, the “+” and “-” inputs are sampled at the same instant. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors during the acquire mode. In conversion mode, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, the ADC inputs can be driven directly. Otherwise, more acquisition time should be allowed for a source with higher impedance.

## APPLICATIONS INFORMATION

### Reference

A low noise, stable reference is required to ensure full performance. The LT<sup>®</sup>1790 and LT6660 are adequate for most applications. The LT6660 is available in 2.5V, 3V, 3.3V and 5V versions, and the LT1790 is available in 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V versions. The exceptionally low input noise allows the input range to be optimized for the application by changing the reference voltage. The  $V_{REF}$  input must be decoupled with a 10 $\mu$ F capacitor in parallel with a 0.1 $\mu$ F capacitor, so verify that the device providing the reference voltage is stable with capacitive loads.

If the voltage reference is 5V and can supply 5mA, it can be used for both  $V_{REF}$  and  $V_{DD}$ .  $V_{DD}$  must be connected to a clean analog supply, and a quiet 5V reference voltage makes a convenient supply for this purpose.

### Input Filtering

The noise and distortion of the input amplifier and other circuitry must be considered since they will add to the ADC noise and distortion. Therefore, noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

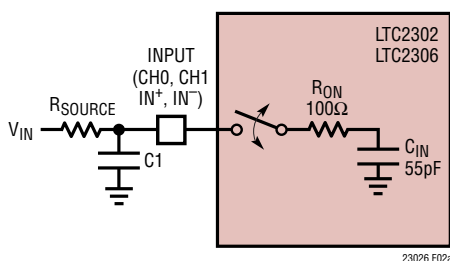


Figure 2a. Analog Input Equivalent Circuit

The analog inputs of the LTC2302/LTC2306 can be modeled as a 55pF capacitor ( $C_{IN}$ ) in series with a 100 $\Omega$  resistor ( $R_{ON}$ ) as shown in Figure 2a.  $C_{IN}$  gets switched to the selected input once during each conversion. Large filter RC time constants will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to 12-bit resolution within the acquisition time ( $t_{ACQ}$ ) if DC accuracy is important.

When using a filter with a large  $C_{FILTER}$  value (e.g., 1 $\mu$ F), the inputs do not completely settle and the capacitive input switching currents are averaged into a net DC current ( $I_{DC}$ ). In this case, the analog input can be modeled by an equivalent resistance ( $R_{EQ} = 1/(f_{SAMPL} \cdot C_{IN})$ ) in series with an ideal voltage source ( $V_{REF}/2$ ) as shown in Figure 2b. The magnitude of the DC current is then approximately  $I_{DC} = (V_{IN} - V_{REF}/2)/R_{EQ}$ , which is roughly proportional to  $V_{IN}$ . To prevent large DC drops across the resistor  $R_{FILTER}$ , a filter with a small resistor and large capacitor should be chosen. When running at the minimum cycle time of 2 $\mu$ s, the input current equals 106 $\mu$ A at  $V_{IN} = 5$ V, which amounts to a full-scale error of 0.5LSB when using a filter resistor ( $R_{FILTER}$ ) of 4.7 $\Omega$ . Applications requiring lower sample rates can tolerate a larger filter resistor for the same amount of full-scale error.

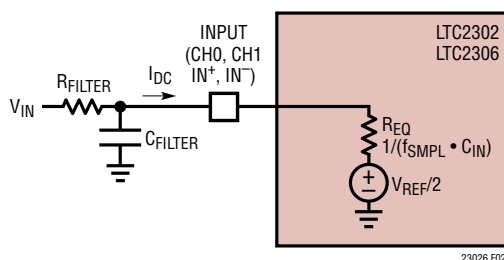


Figure 2b. Analog Input Equivalent Circuit for Large Filter Capacitances

## APPLICATIONS INFORMATION

Figures 3a and 3b show respective examples of input filtering for single-ended and differential inputs. For the single-ended case in Figure 3a, a 50Ω source resistor and a 2000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

### Dynamic Performance

FFT (fast Fourier transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

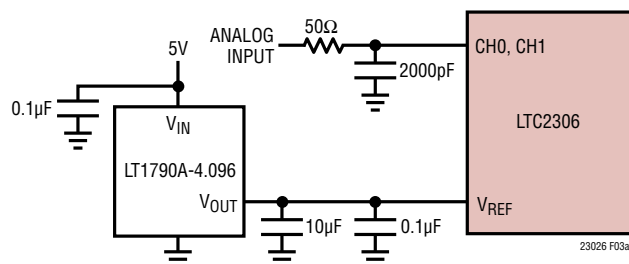


Figure 3a. Optional RC Input Filtering for Single-Ended Input

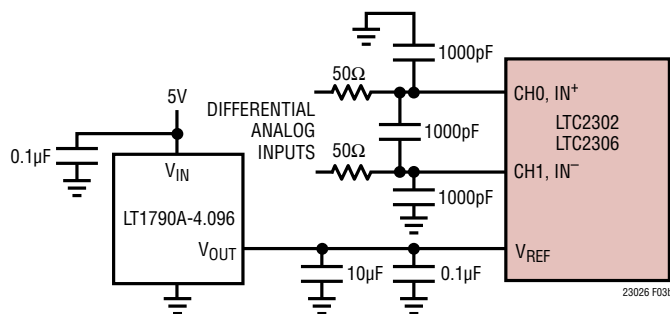


Figure 3b. Optional RC Input Filtering for Differential Inputs

### Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 4 shows a typical SINAD of 72.8dB with a 500kHz sampling rate and a 1kHz input. A SNR of 73.2dB can be achieved with the LTC2302/LTC2306.

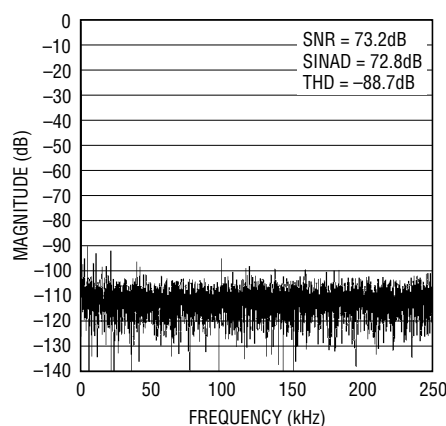


Figure 4. 1kHz Sine Wave 8192 Point FFT Plot (LTC2306)

### Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ( $f_{SAMPL}/2$ ). THD is expressed as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \dots + V_N^2}}{V_1}$$

where  $V_1$  is the RMS amplitude of the fundamental frequency and  $V_2$  through  $V_N$  are the amplitudes of the second through Nth harmonics.



## APPLICATIONS INFORMATION

### Internal Conversion Clock

The internal conversion clock is factory trimmed to achieve a typical conversion time ( $t_{\text{CONV}}$ ) of 1.3 $\mu\text{s}$  and a maximum conversion time of 1.6 $\mu\text{s}$  over the full operating temperature range. With a minimum acquisition time of 240ns, a throughput sampling rate of 500ksps is tested and guaranteed.

### Digital Interface

The LTC2302/LTC2306 communicate via a standard 4-wire SPI compatible digital interface. The rising edge of CONVST initiates a conversion. After the conversion is finished, pull CONVST low to enable the serial output (SDO). The ADC then shifts out the digital data in 2's complement format when operating in bipolar mode or in straight binary format when in unipolar mode, based on the setting of the UNI bit.

For best performance, ensure that CONVST returns low within 40ns after the conversion starts (i.e., before the first bit decision) or after the conversion ends. If CONVST is low when the conversion ends, the MSB bit will appear at SDO at the end of the conversion and the ADC will remain powered up.

### Timing and Control

The start of a conversion is triggered by the rising edge of CONVST. Once initiated, a new conversion cannot be restarted until the current conversion is complete. Figures 6 and 7 show the timing diagrams for two different examples of CONVST pulses. Example 1 (Figure 6) shows CONVST staying HIGH after the conversion ends. If CONVST is high after the  $t_{\text{CONV}}$  period, the LTC2302/LTC2306 enter sleep mode (see Sleep Mode for more details).

When CONVST returns low, the ADC wakes up and the most significant bit (MSB) of the output data sequence at SDO becomes valid after the serial data bus is enabled. All other data bits from SDO transition on the falling edge of each SCK pulse. Configuration data ( $D_{\text{IN}}$ ) is loaded into the LTC2302/LTC2306 at SDI, starting with the first SCK rising edge after CONVST returns low. The S/D bit is loaded on the first SCK rising edge.

Example 2 (Figure 7) shows CONVST returning low before the conversion ends. In this mode, the ADC and all internal circuitry remain powered up. When the conversion is complete, the MSB of the output data sequence at SDO becomes valid after the data bus is enabled. At this point ( $t_{\text{CONV}}$  1.3 $\mu\text{s}$  after the rising edge of CONVST), pulsing SCK will shift data out at SDO and load configuration data ( $D_{\text{IN}}$ ) into the LTC2302/LTC2306 at SDI. The first SCK rising edge loads the S/D bit. SDO transitions on the falling edge of each SCK pulse.

Figures 8 and 9 are the transfer characteristics for the bipolar and unipolar modes. Data is output at SDO in 2's complement format for bipolar readings or in straight binary for unipolar readings.

### Sleep Mode

The ADC enters sleep mode when CONVST is held high after the conversion is complete ( $t_{\text{CONV}}$ ). The supply current decreases to 7 $\mu\text{A}$  in sleep mode between conversions, thereby reducing the average power dissipation as the sample rate decreases. For example, the LTC2302/LTC2306 draw an average of 14 $\mu\text{A}$  with a 1ksps sampling rate. The LTC2302/LTC2306 power down all circuitry when in sleep mode.

### Board Layout and Bypassing

To obtain the best performance, a printed circuit board with a solid ground plane is required. Layout for the printed circuit board should ensure digital and analog signal lines are separated as much as possible. Care should be taken not to run any digital signal alongside an analog signal. All analog inputs should be shielded by GND.  $V_{\text{REF}}$  and  $V_{\text{DD}}$  should be bypassed to the ground plane as close to the pin as possible. Maintaining a low impedance path for the common return of these bypass capacitors is essential to the low noise operation of the ADC. These traces should be as wide as possible. See Figure 5 for a suggested layout.



APPLICATIONS INFORMATION

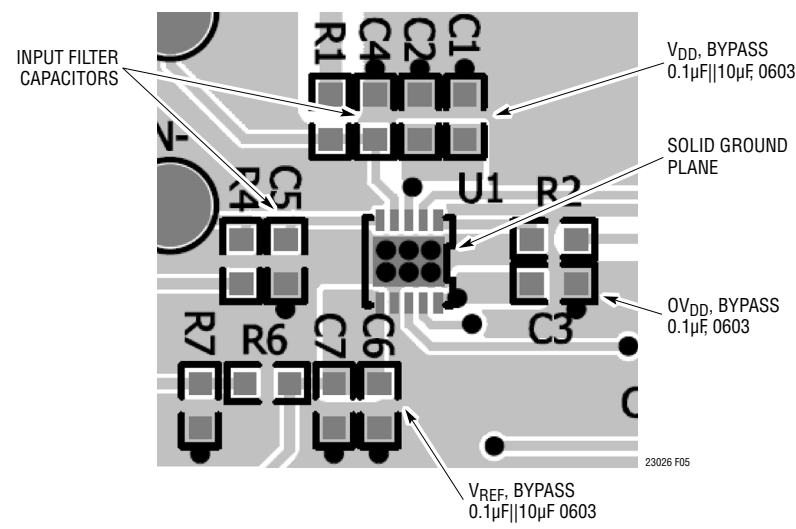


Figure 5. Suggested Layout

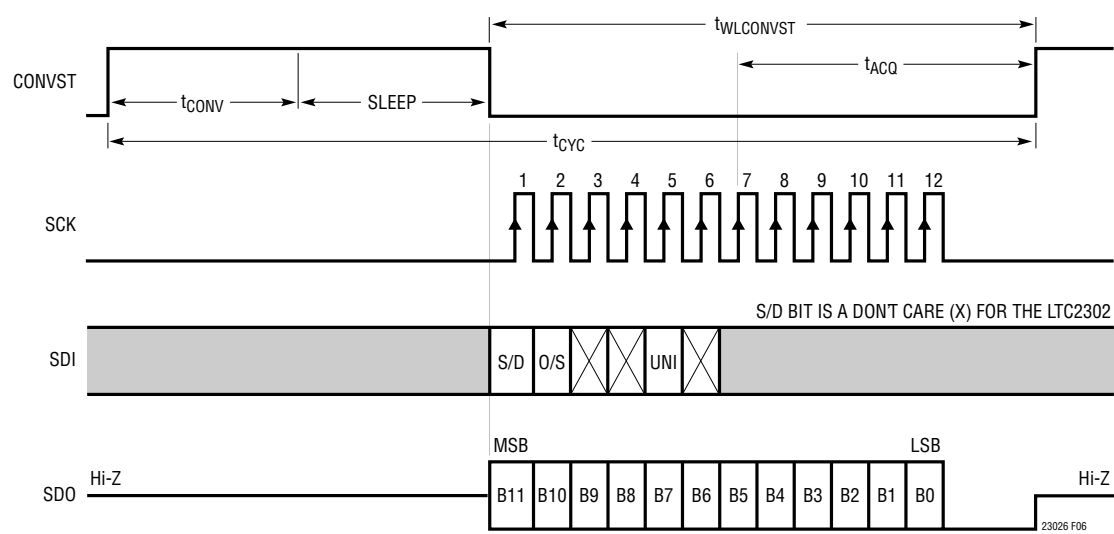


Figure 6. LTC2302/LTC2306 Timing with a Long CONVST Pulse

# APPLICATIONS INFORMATION

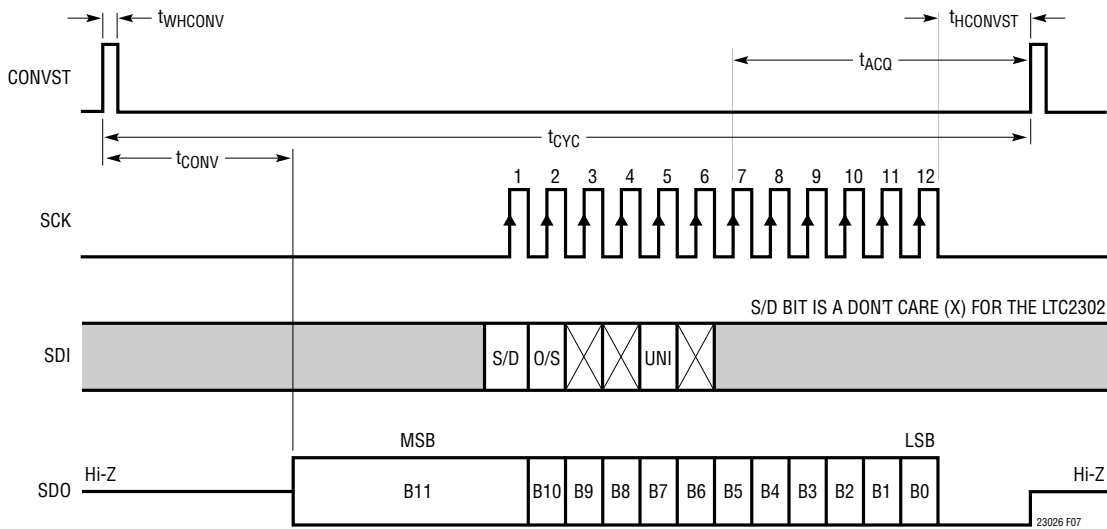


Figure 7. LTC2302/LTC2306 Timing with a Short CONVST Pulse

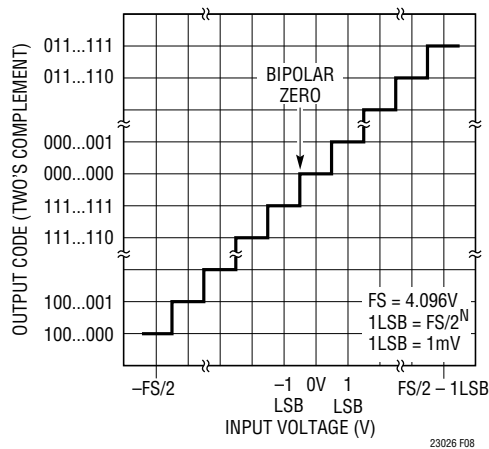


Figure 8. LTC2302/LTC2306 Bipolar Transfer Characteristics (2's Complement)

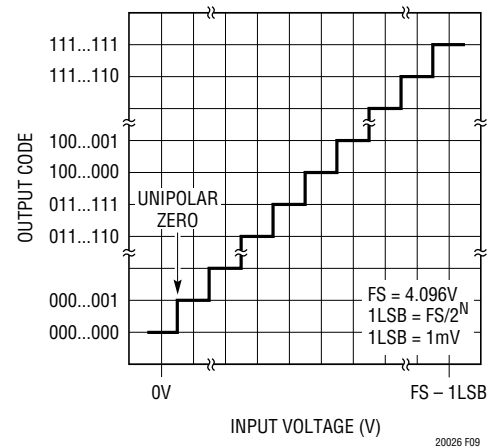


Figure 9. LTC2302/LTC2306 Unipolar Transfer Characteristics (Straight Binary)



**REVISION HISTORY** (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/15	Changed REFCOMP to $V_{REF}$	3

