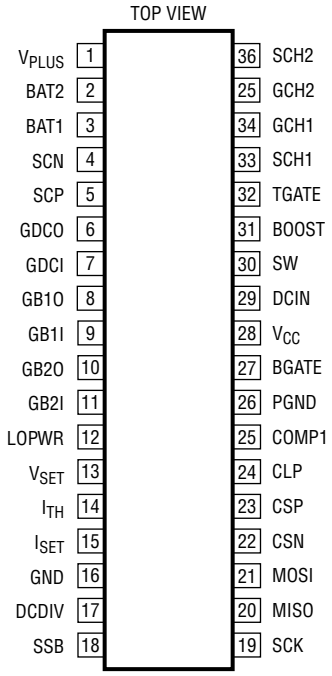
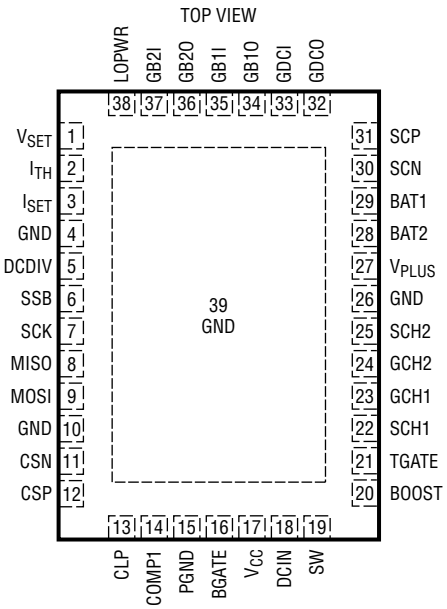
ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage from DCIN, SCP, SCN, CLP, V_{PLUS}, SW to GND ..... –0.3V to 32V
Voltage from SCH1, SCH2 to GND ..... –0.3V to 28V
Voltage from BOOST to GND ..... –0.3V to 41V
PGND with Respect to GND ..... ±0.3V
CSP, CSN, BAT1, BAT2 to GND ..... –5V to 28V
LOPWR, DCDIV to GND ..... –0.3V to 10V
SSB, SCK, MOSI, MISO to GND ..... –0.3V to 7V
COMP1 to GND ..... –0.3V to 5V
Operating Ambient Temperature Range (Note 7) ..... 0°C to 70°C
Operating Junction Temperature ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
SSOP Only ..... 300°C

PIN CONFIGURATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 70°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
THE EXPOSED PAD (PIN 39) IS GND. MUST BE SOLDERED TO THE PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1960CG#PBF	LTC1960CG#TRPBF	LTC1960CG	36-Lead Plastic SSOP	0°C to 70°C
LTC1960CUHF#PBF	LTC1960CUHF#TRPBF	1960	38-Lead (5mm × 7mm) Plastic QFN	0°C to 70°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 7), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Reference							
	DCIN Operating Range	DCIN Selected		6		28	V
I_{CH}	DCIN Operating Current	Not Charging (DCIN Selected) Charging (DCIN Selected)			1 1.3	1.5 2	mA mA
	Battery Operating Voltage Range	Battery Selected, PowerPath Function (Note 2)		6		28	V
	Battery Drain Current	Battery Selected, Not Charging, V_{DCIN} = 0V			175		µA
	V_{PLUS} Diodes Forward Voltage:						
V_{FDC}	DCIN to V_{PLUS}	I_{VCC} = 10mA			0.8		V
V_{FB1}	BAT1 to V_{PLUS}	I_{VCC} = 0mA			0.7		V
V_{FB2}	BAT2 to V_{PLUS}	I_{VCC} = 0mA			0.7		V
V_{FSCN}	SCN to V_{PLUS}	I_{VCC} = 0mA			0.7		V
UVLO	Undervoltage Lockout Threshold	V_{PLUS} Ramping Down, Measured at V_{PLUS} to GND	●	3	3.5	3.9	V
UVHYS	UV Lockout Hysteresis	V_{PLUS} Rising, Measured at V_{PLUS} to GND			60		mV
V_{VCC}	V_{CC} Regulator Output Voltage			5	5.2	5.4	V
V_{LDR}	V_{CC} Load Regulation	I_{VCC} = 0mA to 10mA			0.2	1	%
Switching Regulator							
V_{TOL}	Overall Voltage Accuracy	5V ≤ V_{OUT} < 25V, (Note 3)	 ●	–0.8 –1		0.8 1	% %
I_{TOL}	Overall Current Accuracy	IDAC Value = $3FF_{HEX}$ V_{CSP}, V_{CSN} = 12V	 ●	–5 –6		5 6	% %
f_{OSC}	Regulator Switching Frequency			255	300	345	kHz
f_{DO}	Regulator Switching Frequency in Low Dropout Mode	Duty Cycle ≥ 99%		20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle			99	99.5		%
I_{MAX}	Maximum Current Sense Threshold	V_{ITH} = 2.2V		140	155	190	mV
I_{SNS}	CA1 Input Bias Current	V_{CSP} = V_{CSN} > 5V			150		µA
CMSL	CAI Input Common Mode Low			0			V
CMSH	CAI Input Common Mode High					V_{DCIN}–0.2	V
V_{CL1}	CL1 Turn-On Threshold			95	100	105	mV
	TGATE Transition Time:						
TG t_r	TGATE Rise Time	C_{LOAD} = 3300pF, 10% to 90%			50	90	ns
TG t_f	TGATE Fall Time	C_{LOAD} = 3300pF, 10% to 90%			50	90	ns
	BGATE Transition Time:						
BG t_r	BGATE Rise Time	C_{LOAD} = 3300pF, 10% to 90%			50	90	ns
BG t_f	BGATE Fall Time	C_{LOAD} = 3300pF, 10% to 90%			40	80	ns
Trip Points							
V_{TR}	DCDIV/LOPWR Threshold	V_{DCDIV} or V_{LOPWR} Falling	●	1.166	1.19	1.215	V
V_{THYS}	DCDIV/LOPWR Hysteresis Voltage	V_{DCDIV} or V_{LOPWR} Rising			30		mV
I_{BVT}	DCDIV/LOPWR Input Bias Current	V_{DCDIV} or V_{LOPWR} = 1.19V			20	200	nA
V_{TSC}	Short-Circuit Comparator Threshold	V_{SCP} – V_{SCN}, V_{CC} ≥ 5V	●	90	100	115	mV
V_{FTO}	Fast PowerPath Turn-Off Threshold	V_{DCDIV} Rising from V_{CC}		6	7	7.9	V
V_{OVSD}	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage	V_{SET} Rising from 0.8V Until TGATE and BGATE Stop Switching			107		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 7), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DACs							
I_{RES}	IDAC Resolution	Guaranteed Monotonic Above $I_{MAX}/16$		10			bits
t_{IP} t_{ILOW}	IDAC Pulse Period: Normal Mode Low Current Mode			6	10 50	15	µs ms
V_{RES}	VDAC Resolution	Guaranteed Monotonic (5V < V_{BAT} < 25V)		11			bits
V_{STEP}	VDAC Granularity				16		mV
V_{OFF}	VDAC Offset	(Note 6)			0.8		V
t_{VP}	VDAC Pulse Period			7	11	16.5	µs
Charge MUX Switches							
t_{ONC}	GCH1/GCH2 Turn-On Time	$V_{GCHX} - V_{SCHX}$ > 3V, C_{LOAD} = 3nF			5	10	ms
t_{ONC}	GCH1/GCH2 Turn-Off Time	$V_{GCHX} - V_{SCHX}$ < 1V, from Time of V_{CSN} < V_{BATX} – 30mV, C_{LOAD} = 3nF			3	7	µs
V_{CON}	CH Gate Clamp Voltage GCH1 GCH2	I_{LOAD} = 1µA $V_{GCH1} - V_{SCH1}$ $V_{GCH2} - V_{SCH2}$		 5 5	 5.8 5.8	 7 7	 V V
V_{COFF}	CH Gate Off Voltage GCH1 GCH2	I_{LOAD} = 10µA $V_{GCH1} - V_{SCH1}$ $V_{GCH2} - V_{SCH2}$		 –0.8 –0.8	 –0.4 –0.4	 0 0	 V V
V_{TOC}	CH Switch Reverse Turn-Off Voltage	$V_{CSN} - V_{BATX}$, 5V ≤ V_{BATX} ≤ 28V	●	5	20	40	mV
V_{FC}	CH Switch Forward Regulation Voltage	$V_{BATX} - V_{CSN}$, 5V ≤ V_{BATX} ≤ 28V	●	15	35	60	mV
$I_{OC(SRC)}$ $I_{OC(SNK)}$	GCH1/GCH2 Active Regulation: Max Source Current Max Sink Current	$V_{GCHX} - V_{SCHX}$ = 1.5V			 –2 2		 µA µA
V_{CHMIN}	BATX Voltage Below Which Charging Is Inhibited	(Note 8)		3.5		4.7	V
PowerPath Switches							
t_{DLY}	Blanking Period After UVLO Trip	Switches Held Off			250		ms
t_{PPB}	Blanking Period After LOPWR Trip	Switches in 3-Diode Mode			1		sec
t_{ONPO}	GB1O/GB2O/GDCO Turn-On Time	V_{GS} < –3V, from Time of Battery/DC Removal, or LOPWR Indication	●		5	10	µs
t_{OFFPO}	GB1O/GB2O/GDCO Turn-Off Time	V_{GS} > –1V, from Time of Battery/DC Removal, or LOPWR Indication	●		3	7	µs
V_{PONO}	Output Gate Clamp Voltage GB1O GB2O GDCO	I_{LOAD} = 1µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1O} Highest (V_{BAT2} or V_{SCP}) – V_{GB2O} Highest (V_{DCIN} or V_{SCP}) – V_{GDCO}		 4.75 4.75 4.75	 6.25 6.25 6.25	 7 7 7	 V V V
V_{POFFO}	Output Gate Off Voltage GB1O GB2O GDCO	I_{LOAD} = –25µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1O} Highest (V_{BAT2} or V_{SCP}) – V_{GB2O} Highest (V_{DCIN} or V_{SCP}) – V_{GDCO}			 0.18 0.18 0.18	 0.25 0.25 0.25	 V V V
V_{TOP}	PowerPath Switch Reverse Turn-Off Voltage	$V_{SCP} - V_{BATX}$ or $V_{SCP} - V_{DCIN}$ 6V ≤ V_{SCP} ≤ 28V	●	5	20	60	mV
V_{FP}	PowerPath Switch Forward Regulation Voltage	$V_{BATX} - V_{SCP}$ or $V_{DCIN} - V_{SCP}$ 6V ≤ V_{SCP} ≤ 28V	●	0	25	50	mV
$I_{OP(SRC)}$ $I_{OP(SNK)}$	GDCI/GB1I/GB2I Active Regulation Source Current Sink Current	(Note 4)			 –4 75		 µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 7), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ONPI}	Gate B1I/B2I/DCI Turn-On Time	V_{GS} < –3V, C_{LOAD} = 3nF (Note 5)			300		µs
t_{OFFPI}	Gate B1I/B2I/DCI Turn-Off Time	V_{GS} > –1V, C_{LOAD} = 3nF (Note 5)			10		µs
V_{PONI}	Input Gate Clamp Voltage	I_{LOAD} = 1µA					
	GB1I	Highest (V_{BAT1} or V_{SCP}) – V_{GB1I}		4.75	6.7	7.5	V
	GB2I	Highest (V_{BAT2} or V_{SCP}) – V_{GB2I}		4.75	6.7	7.5	V
	GDCI	Highest (V_{DCIN} or V_{SCP}) – V_{GDCI}		4.75	6.7	7.5	V
V_{POFFI}	Input Gate Off Voltage	I_{LOAD} = 25µA					
	GB1I	Highest (V_{BAT1} or V_{SCP}) – V_{GB1I}			0.18	0.25	V
	GB2I	Highest (V_{BAT2} or V_{SCP}) – V_{GB2I}			0.18	0.25	V
	GDCI	Highest (V_{DCIN} or V_{SCP}) – V_{GDCI}			0.18	0.25	V
Logic I/O							
I_{IH}/I_{IL}	SSB/SCK/MOSI Input High/Low Current		●	–1		1	µA
V_{IL}	SSB/MOSI/SCK Input Low Voltage		●			0.8	V
V_{IH}	SSB/MOSI/SCK Input High Voltage		●	2			V
V_{OL}	MISO Output Low Voltage	I_{OL} = 1.3mA	●			0.4	V
I_{OFF}	MISO Output Off-State Leakage Current	V_{MISO} = 5V	●			2	µA
SPI Timing (See Timing Diagram)							
T_{WD}	Watch Dog Timer		●	1.2	2.5	4.5	sec
t_{SSH}	SSB High Time			680			ns
t_{CYC}	SCK Period	C_{LOAD} = 200pF R_{PULLUP} = 4.7k on MISO	●	2			µs
t_{SH}	SCK High Time			680			ns
t_{SL}	SCK Low Time			680			ns
t_{LD}	Enable Lead Time			200			ns
t_{LG}	Enable Lag Time			200			ns
t_{su}	Input Data Set-Up Time		●	100			ns
t_H	Input Data Hold Time		●	100			ns
t_A	Access Time (From Hi-Z to Data Active on MISO)		●			125	ns
t_{dis}	Disable Time (Hold Time to Hi-Z State on MISO)		●			125	ns
t_V	Output Data Valid	C_L = 200pF, R_{PULLUP} = 4.7k on MISO	●			580	ns
t_{HO}	Output Data Hold		●	0			ns
t_{lr}	SCK/MOSI/SSB Rise Time	0.8V to 2V				250	ns
t_{lf}	SCK/MOSI/SSB Fall Time	2V to 0.8V				250	ns
t_{Of}	MISO Fall Time	2V to 0.4V, C_L = 200pF	●			400	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. Battery voltage must be adequate to drive gates of PowerPath P-channel FET switches. This does not affect charging voltage of the battery, which can be zero volts.

Note 3. See Test Circuit.

Note 4. DCIN, BAT1, BAT2 are held at 12V and GDCI, GB1I, GB2I are forced to 10.5V. SCP is set at 12.0V to measure source current at GDCI, GB1I and GB2I. SCP is set at 11.9V to measure sink current at GDCI, GB1I and GB2I.

Note 5. Extrapolated from testing with C_L = 50pF.

Note 6. VDAC offset is equal to the reference voltage, since

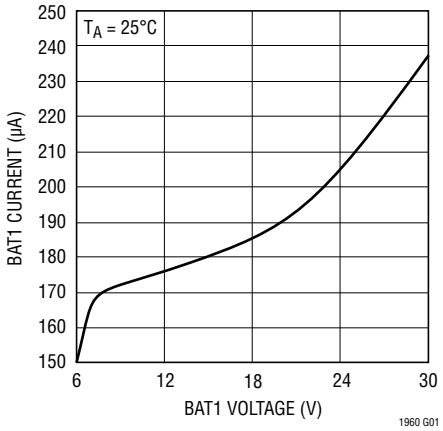
$V_{OUT} = V_{REF}(16mV \bullet VDAC_{(VALUE)}/2047 + 1)$

Note 7. The LTC1960C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance at –40°C and 85°C, but is not tested at these extended temperature limits.

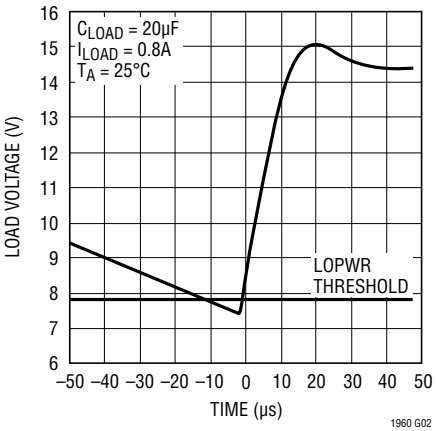
Note 8. Does not apply to low current mode. Refer to “The Current DAC Block” in the Operation section.

TYPICAL PERFORMANCE CHARACTERISTICS

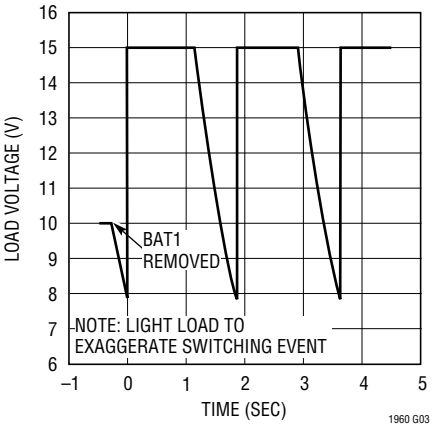
Battery Drain Current (BAT1 Selected)



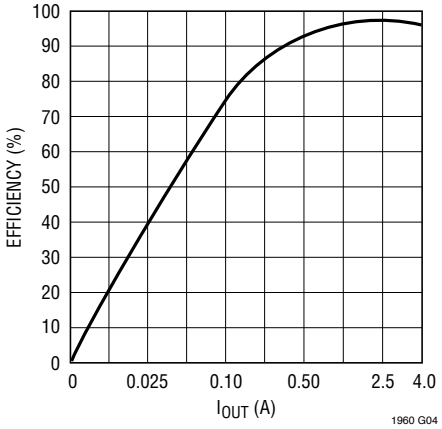
PowerPath Switching



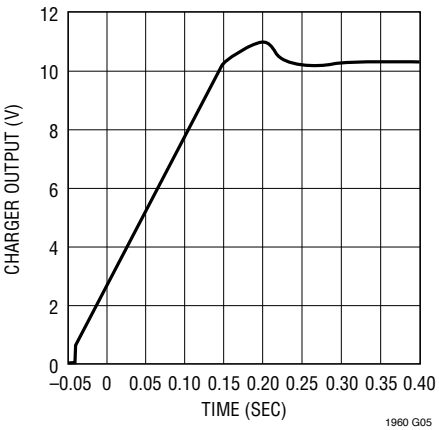
PowerPath Autonomous Switching



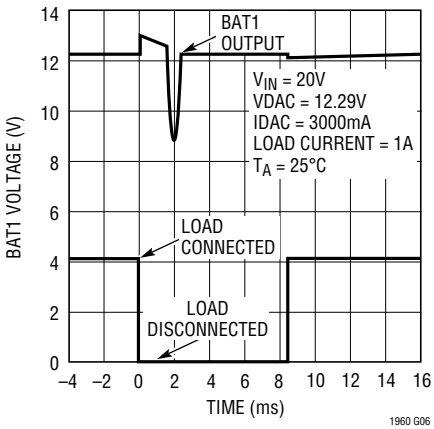
Charger Efficiency



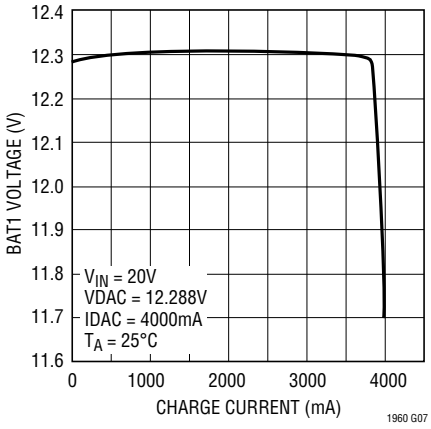
Charger Start-Up



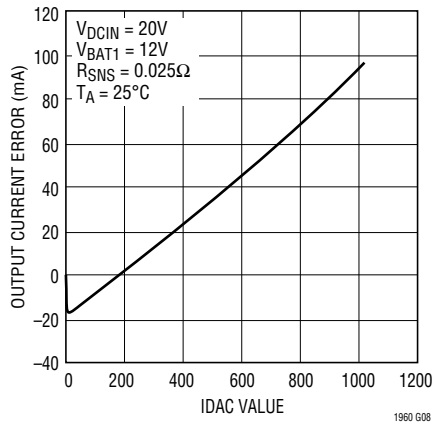
Charger Load Dump



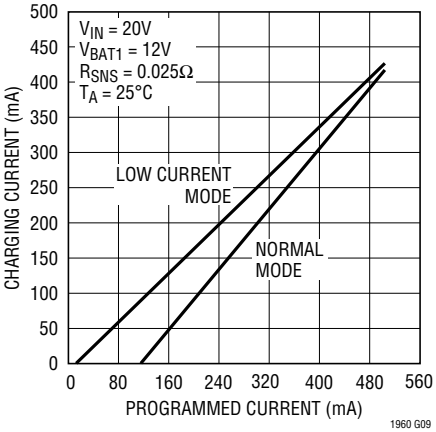
Charger Load Regulation



Charging Current Accuracy



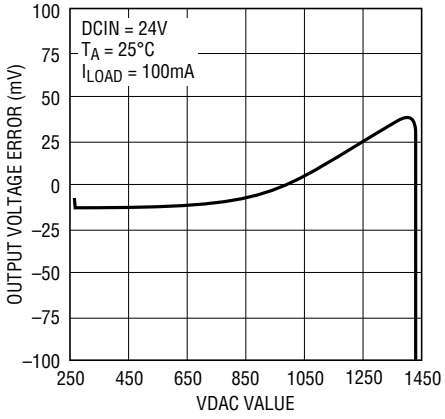
IDAC Low Current Mode vs Normal Mode



Rev. C

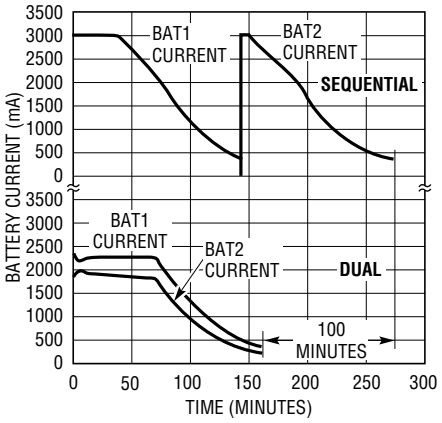
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Accuracy



1960 G10

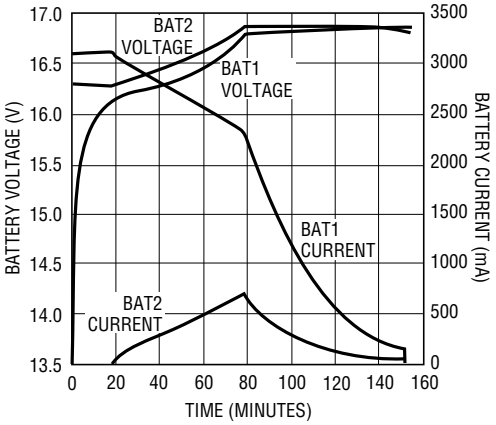
Dual vs Sequential Charging



BATTERY TYPE: 10.8V Li-Ion (MOLTECH NI2020)
REQUESTED CURRENT = 3A
REQUESTED VOLTAGE = 12.3V
MAX CHARGER CURRENT = 4.1A

1960 G11

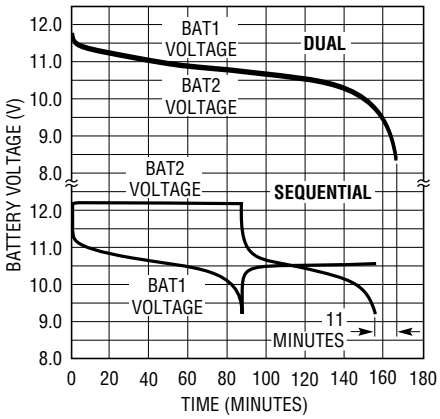
Dual Charging Batteries with Different Charge State



BAT1 INITIAL CAPACITY = 0%
BAT2 INITIAL CAPACITY = 90%
PROGRAMMED CHARGER CURRENT = 3A
PROGRAMMED CHARGER VOLTAGE = 16.8V

1960 G12

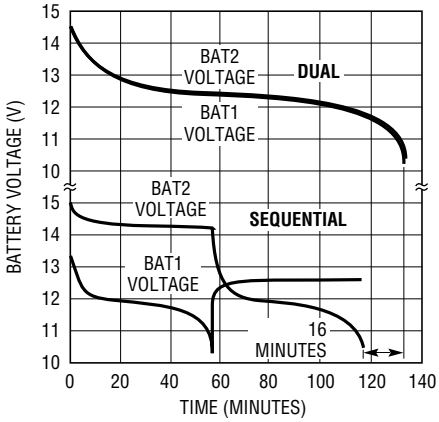
Dual vs Sequential Discharge



BATTERY TYPE: 10.8V Li-Ion(MOLTECH NI2020)
LOAD CURRENT = 3A

1960 G13

Dual vs Sequential Discharge



BATTERY TYPE: 12V NIMH (MOLTECH NJ1020)
LOAD: 33W

1960 G14

PIN FUNCTIONS (G/UHF)

Input Power Related

SCN (Pin 4/Pin 30): PowerPath Current Sensing Negative Input. This pin should be connected directly to the "bottom" (output side) of the sense resistor, R_{SC}, in series with the three PowerPath switch pairs, for detecting short-circuit current events. Also powers LTC1960 internal circuitry when all other sources are absent.

SCP (Pin 5/Pin 31): PowerPath Current Sensing Positive Input. This pin should be connected directly to the "top" (switch side) of the sense resistor, R_{SC}, in series with the three PowerPath switch pairs, for detecting short-circuit current events.

GDCO (Pin 6/Pin 32): DCIN Output Switch Gate Drive. Together with GDCI, this pin drives the gate of the P-channel switch in series with the DCIN input switch.

GDCI (Pin 7/Pin 33): DCIN Input Switch Gate Drive. Together with GDCO, this pin drives the gate of the P-channel switch connected to the DCIN input.

GB1O (Pin 8/Pin 34): BAT1 Output Switch Gate Drive. Together with GB1I, this pin drives the gate of the P-channel switch in series with the BAT1 input switch.

GB1I (Pin 9/Pin 35): BAT1 Input Switch Gate Drive. Together with GB1O, this pin drives the gate of the P-channel switch connected to the BAT1 input.

GB2O (Pin 10/Pin 36): BAT2 Output Switch Gate Drive. Together with GB2I, this pin drives the gate of the P-channel switch in series with the BAT2 input switch.

GB2I (Pin 11/Pin 37): BAT2 Input Switch Gate Drive. Together with GB2O, this pin drives the gate of the P-channel switch connected to the BAT2 input.

CLP (Pin 24/Pin 13): The Positive Input to the Supply Current Limiting Amplifier CL1. The threshold is set at 100mV above the voltage at the DCIN pin. When used to limit supply current, a filter is needed to filter out the switching noise.

Battery Charging Related

V_{SET} (Pin 13/Pin 1): The Tap Point of a Programmable Resistor Divider Which Provides Battery Voltage Feedback to the Charger. A capacitor from CSN to V_{SET} and from V_{SET} to GND provide necessary compensation and filtering for the voltage loop.

I_{TH} (Pin 14/Pin 2): The Control Signal of the Inner Loop of the Current Mode PWM. Higher I_{TH} voltage corresponds to higher charging current in normal operation. A capacitor of at least 0.1µF to GND filters out PWM ripple. Typical full-scale output current is 30µA. Nominal voltage range for this pin is 0V to 2.4V.

I_{SET} (Pin 15/Pin 3): A capacitor from I_{SET} to ground is required to filter higher frequency components from the delta-sigma IDAC.

CSN (Pin 22/Pin 11): Current Amplifier CA1 Input. Connect this to the common output of the charger MUX switches.

CSP (Pin 23/Pin 12): Current Amplifier CA1 Input. This pin and the CSN pin measure the voltage across the sense resistor, R_{SNS}, to provide the instantaneous current signals required for both peak and average current mode operation.

COMP1 (Pin 25/Pin 14): The Compensation Node for the Amplifier CL1. A capacitor is required from this pin to GND if input current amplifier CL1 is used. At input adapter current limit, this node rises to 1V. By forcing COMP1 low, amplifier CL1 will be defeated (no adapter current limit). COMP1 can source 10µA.

BGATE (Pin 27/Pin 16): Drives the bottom external MOSFET of the battery charger buck converter.

SW (Pin 30/Pin 19): PWM switch node connected to source of the top external MOSFET switch. Used as reference for top gate driver.

BOOST (Pin 31/Pin 20): Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from a diode drop below V_{CC} to (DCIN + V_{CC}).

PIN FUNCTIONS (G/UHF)

TGATE (Pin 32/Pin 21): Drives the top external MOSFET of the battery charger buck converter.

SCH1 (Pin 33/Pin 22), SCH2 (Pin 36/Pin 25): Charger MUX N-Channel Switch Source Returns. These two pins are connected to the sources of the back-to-back switch pairs, Q3/Q4 and Q9/Q10 (see Typical Application on back page of data sheet), respectively. A small pull-down current source returns these nodes to 0V when the switches are turned off.

GCH1 (Pin 34/Pin 23), GCH2 (Pin 35/Pin 24): Charger MUX N-Channel Switch Gate Drives. These two pins drive the gates of the back-to-back switch pairs, Q3/Q4 and Q9/Q10, between the charger output and the two batteries.

External Power Supply Pins

V_{PLUS} (Pin 1/Pin 27): Supply. The V_{PLUS} pin is connected via four internal diodes to the DCIN, SCN, BAT1, and BAT2 pins. Bypass this pin with a 1µF to 2µF capacitor.

BAT1 (Pin 3/Pin 29), BAT2 (Pin 2/Pin 28): These two pins are the inputs from the two batteries for power to the LTC1960 and to provide voltage feedback to the battery charger.

LOPWR (Pin 12/Pin 38): LOPWR Comparator Input from SCN External Resistor Divider to GND. If the voltage at LOPWR is lower than the LOPWR comparator threshold, then system power has failed and power is autonomously switched to a higher voltage source, if available. See PowerPath section of LTC1960 operation.

DCDIV (Pin 17/Pin 5): External DC Source Comparator Input from DCIN External Resistor Divider to GND. If the voltage at DCDIV is above the DCDIV comparator threshold, then the DC bit is set and the wall adapter power is considered to be adequate to charge the batteries. If DCDIV rises more than 1.8V above V_{CC}, then all of the PowerPath switches are latched off until all power is removed.

A capacitor from DCDIV to GND is recommended to prevent noise-induced false emergency turn-off conditions from being detected. Refer to "Fast PowerPath Turn-Off" in the Operation section and the Typical Application on the back page of this data sheet.

DCIN (Pin 29/Pin 18): Supply. External DC power source. A 1µF bypass capacitor should be connected to this pin as close as possible. No series resistance is allowed, since the adapter current limit comparator input is also this pin.

Internal Power Supply Pins

GND (Pin 16/Pin 4, Pin 10, Pin 26, Pin 39): Ground for Low Power Circuitry.

PGND (Pin 26/Pin 15): High Current Ground Return for BGATE Driver.

V_{CC} (Pin 28/Pin 17): Internal Regulator Output. Bypass this output with at least a 2µF to 4.7µF capacitor. Do not use this regulator output to supply more than 1mA to external circuitry.

Digital Interface Pins

SSB (Pin 18/Pin 6): SPI Slave Select Input. Active low. TTL levels. This signal is low when clocking data to/from the LTC1960.

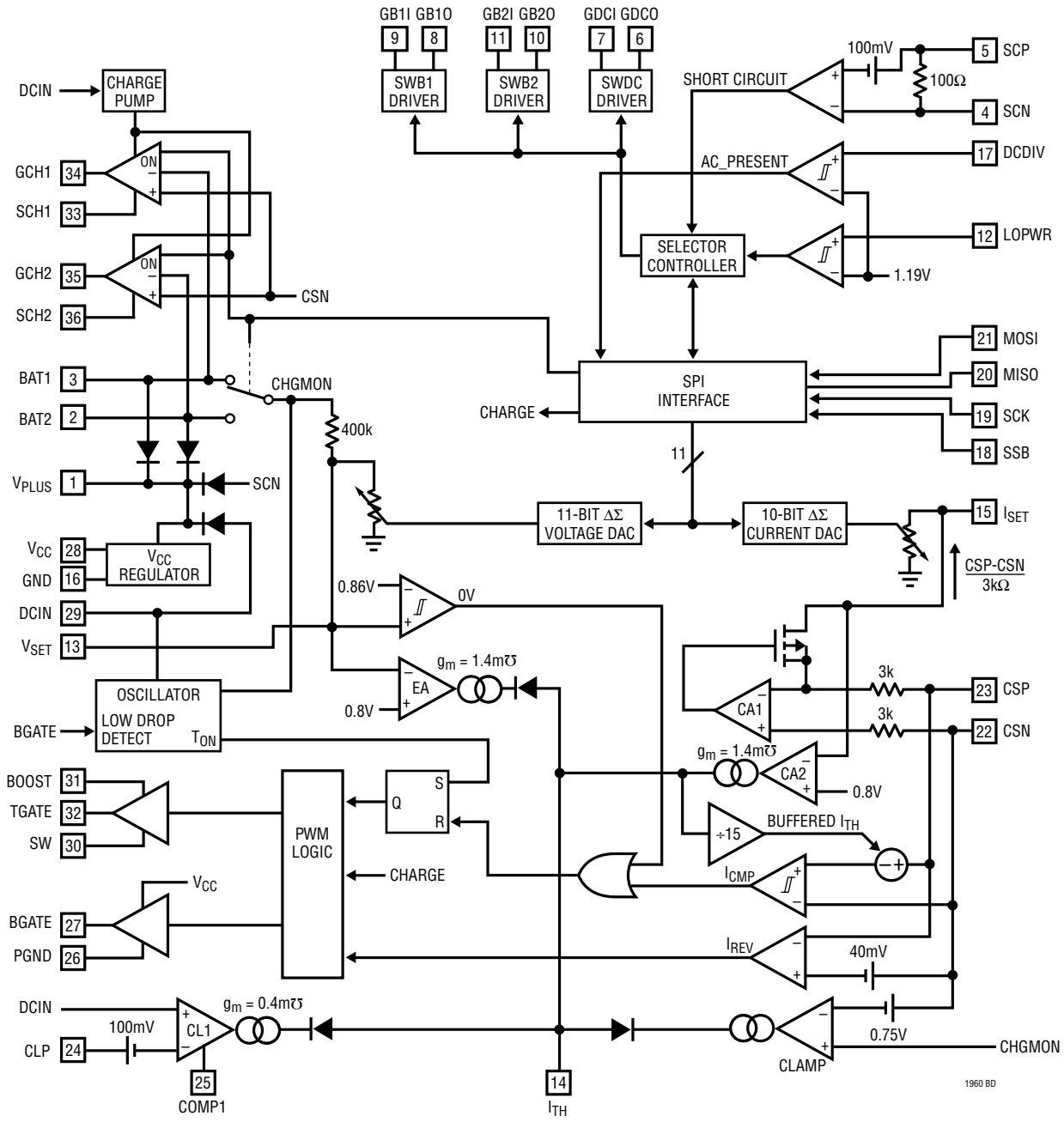
SCK (Pin 19/Pin 7): Serial SPI Clock. TTL levels.

MISO (Pin 20/Pin 8): SPI Master-In-Slave-Out Output, Open Drain. Serial data is transmitted from the LTC1960, when SSB is low, on the falling edge of SCK. TTL levels. A 4.7k pull-up resistor is recommended.

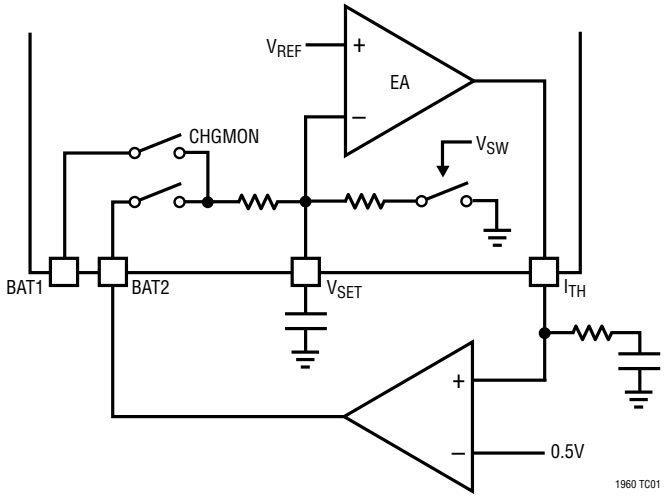
MOSI (Pin 21/Pin 9): SPI Master-Out-Slave-In Input. Serial data is transmitted to the LTC1960, when SSB is low, on the rising edge of SCK. TTL levels.

GND (Exposed Pad Pin 39, UHF Package Only): Ground. Must be soldered to the PCB ground for rated thermal performance.

BLOCK DIAGRAM (LTC1960CG Pin Numbers Shown)

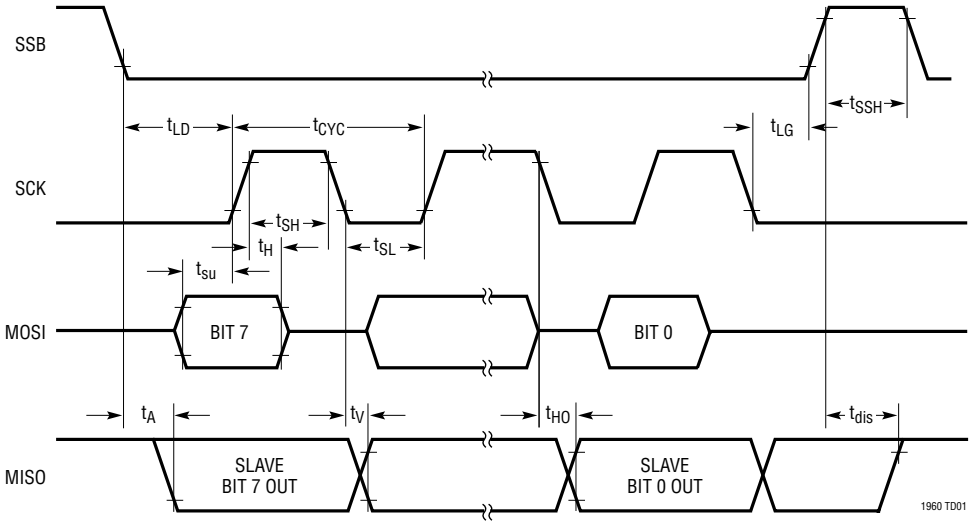


TEST CIRCUIT



TIMING DIAGRAM

SPI Timing Diagram



OPERATION (Refer to Block Diagram and Typical Application)

OVERVIEW

The LTC1960 is composed of a battery charger controller, charge MUX controller, PowerPath controller, SPI interface, a 10-bit current DAC (IDAC) and 11-bit voltage DAC (VDAC). When coupled with a low cost microprocessor, it forms a complete battery charger/selector system for two batteries. The battery charger is programmed for voltage and current, and the charging battery is selected via the SPI interface. Charging can be accomplished only if the voltage at DCDIV indicates that sufficient voltage is available from the input power source, usually an AC adapter. The charge MUX, which selects the battery to be charged, is capable of charging both batteries simultaneously by selecting both batteries for charging. The charge MUX switch drivers are configured to allow charger current to share between the two batteries and to prevent current from flowing in a reverse direction in the switch. The amount of current that each battery receives will depend upon the relative capacity of each battery and the battery voltage. This can result in significantly shorter charging times (up to 50% for Li-Ion batteries) than sequential charging of each battery. In order to continue charging, the CHARGE_BAT information must be updated more frequently than the internal watchdog timer.

The PowerPath controller selects which of the pairs of PFET switches, input and output, will provide power to the system load. The selection is accomplished over the SPI interface. If the system voltage drops below the threshold set by the LOPWR resistor divider, then all of the output side PFETs are turned on quickly and power is taken from the highest voltage source available at the DCIN, BAT1 or BAT2 inputs. The input side PFETs act as diodes in this mode and power is taken from the source with the highest voltage. The input side PowerPath switch driver that is delivering power then closes its input switch to reduce the power dissipation in the PFET bulk diode. In effect, this system provides diode -like behavior from the FET switches, without the attendant high power dissipation from diodes. The microprocessor is informed of this 3-diode mode status when it polls the PowerPath status register via the SPI interface. The microprocessor can then assess which power source is capable of providing power, and program the PowerPath switches accordingly. Since high speed PowerPath switching at LOPWR trip points is handled autonomously, there is no need for real-time microprocessor resources to accomplish this task.

Simultaneous discharge of both batteries is accomplished by simply programming both batteries for discharge into the system load. The switch drivers prevent reverse current flow in the switches and automatically discharge both batteries into the load, sharing current according to the relative capacity of the batteries. Simultaneous dual discharge can increase battery operating time by approximately 10% by reducing losses in the switches and reducing internal losses associated with high discharge rates.

SPI Interface

The SPI interface is used to write to the internal PowerPath registers, the charger control registers, the current DAC, and the voltage DAC. The SPI is also able to read internal status registers. There are two types of SPI write commands. The first write command is a 1-byte command used to load PowerPath and charger control bits. The second write command is a 2-byte command used to load the DACs. The SPI read command is a 2-byte command. In order to ensure the integrity of the SPI communication, the last bit received by the SPI is echoed back over the MISO output after the next falling SCK. The data format is set up so that the master has the option of aborting a write if the returned MISO bit is not as expected.

OPERATION

1-Byte SPI Write Format:

	bit 7.....byte 1.....bit 0
MOSI	D0 D1 D2 X A0 A1 A2 0
MISO	X D0 D1 D2 X A0 A1 A2
Charger Write Address:	A[2:0] = b111
Charger Write Data:	D2 = X
	D1 = CHARGE_BAT2
	D0 = CHARGE_BAT1
PowerPath Write Address:	A[2:0] = b110
PowerPath Write Data:	D2 = POWER_BY_DC
	D1 = POWER_BY_BAT2
	D0 = POWER_BY_BAT1

2-Byte SPI Write Format:

	bit 7.....byte 1.....bit 0	bit 7.....byte 2.....bit 0
MOSI	D0 D1 D2 D3 D4 D5 D6 1	D7 D8 D9 D10 A0 A1 A2 0
MISO	X D0 D1 D2 D3 D4 D5 D6	1 D7 D8 D9 D10 A0 A1 A2
IDAC Write Address:	A[2:0] = b000	
IDAC Data Bits D9-D0:	IDAC value data (MSB-LSB)	
IDAC Data Bit D10 :	Normal mode = 0, low current mode = 1 (Dual battery charging is disabled)	
VDAC Write Address:	A[2:0] = b001	
VDAC Data Bits D10-D0:	VDAC value (MSB-LSB)	

Subsequent SPI communication is inhibited until after the addressed DAC is finished loading. It is recommended that the master transmit 0X01 bytes until MISO goes low. This handshaking procedure is illustrated in Figure 1.

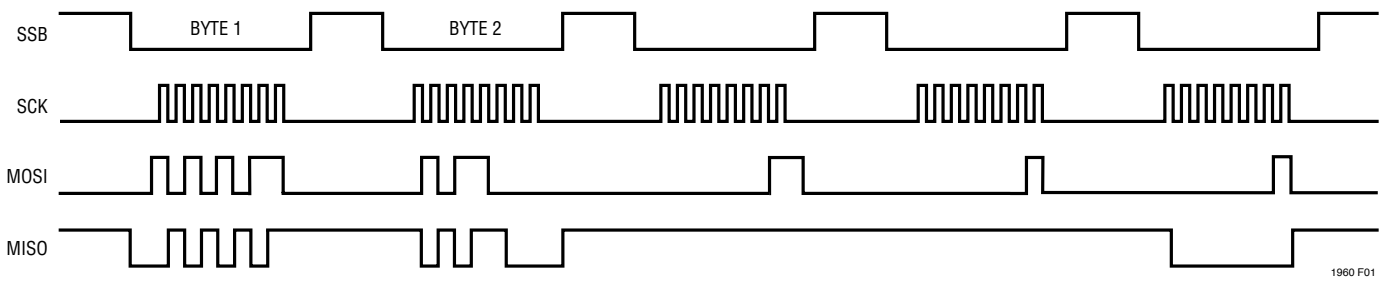


Figure 1. SPI Write to VDAC of Data = b101_0101_0101

OPERATION

2-Byte SPI Read Format:

	bit 7.....byte 1.....bit 0	bit 7.....byte 2.....bit 0
MOSI	0 0 0 0 A0 A1 A2 0	0 0 0 0 A0 A1 A2 1
MISO	X 0 0 0 0 A0 A1 A2	X FA LP DC PF CH X X

Status Address: A[2:0] = b010

Status Read Data:

LP = LOW_POWER (Low power comparator output)

DC = DCDIV (DCDIV comparator output)

PF = POWER_FAIL (Set if selected power supply failed to hold up system power after three tries)

CH = CHARGING (One or more batteries are being charged)

FA = FAULT. This bit is set for any of the following conditions:

1) The LTC1960 is still in power-on reset.

2) The LTC1960 has detected a short circuit and has shut down power and charging.

3) The system has asserted a fast off using DCDIV.

Note: All other values of A[2:0] are reserved and must not be used.

A status read is illustrated in Figure 2.

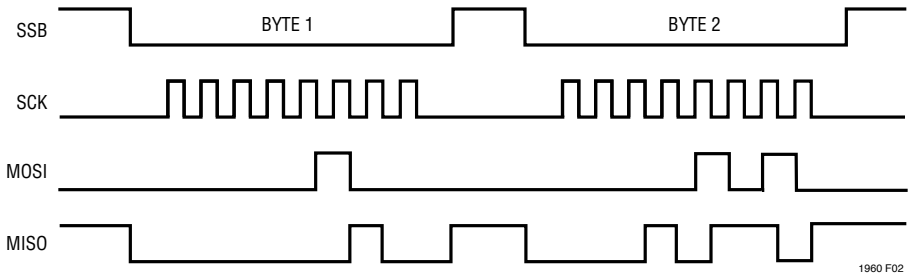


Figure 2. SPI Read of FA = 0, LP = 0, DC = 1, PF = 0, and CH = 1

OPERATION

Battery Charger Controller

The LTC1960 charger controller uses a constant off-time, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the SR latch and turned off when the main current comparator ICMP resets the SR latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current reverses, as indicated by current comparator IREV, or the beginning of the next cycle. The oscillator uses the equation:

$$t_{OFF} = \frac{1}{f_{OSC}} \bullet \frac{(V_{DCIN} - V_{CSN})}{V_{DCIN}}$$

to set the bottom MOSFET on time. The peak inductor current at which ICMP resets the SR latch is controlled by the voltage on I_{TH}. I_{TH} is in turn controlled by several loops, depending upon the situation at hand. The average current control loop converts the voltage between CSP and CSN to a representative current. Error amp CA2 compares this current against the desired current requested by the IDAC at the I_{SET} pin and adjusts I_{TH} until the IDAC value is satisfied. The BAT1/BAT2 MUX provides the selected battery voltage at CHGMON, which is divided down to the V_{SET} pin by the VDAC resistor divider and is used by error amp EA to decrease I_{TH} if the V_{SET} voltage is above the 0.8V reference. The amplifier CL1 monitors and limits the input current, normally from the AC adapter, to a preset level ($100mV/R_{CL}$). At input current limit, CL1 will decrease the I_{TH} voltage and thus reduce battery charging current.

An overvoltage comparator, OV, guards against transient overshoots (>7%). In this case, the top MOSFET is turned off until the overvoltage condition is cleared. This feature is useful for batteries which "load dump" themselves by opening their protection switch to perform functions such as calibration or pulse mode charging.

Charging is inhibited for battery voltages below the minimum charging threshold, V_{CHMIN}. Charging is not inhibited when the low current mode of the IDAC is selected.

The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is normally recharged from V_{CC} through an external diode when the top MOSFET is turned off. A 2µF to 4.7µF capacitor across V_{CC} to GND is required to provide a low dynamic impedance to charge the boost capacitor. It is also required for stability and power-on reset purposes.

As V_{IN} decreases towards the selected battery voltage, the converter will attempt to turn on the top MOSFET continuously ("dropout"). A dropout timer detects this condition and forces the top MOSFET to turn off, and the bottom MOSFET on, for about 200ns at 40µs intervals to recharge the bootstrap capacitor.

Charge MUX Switches

The equivalent circuit of a charge MUX switch driver is shown in Figure 3. If the charger controller is not enabled, the charge MUX drivers will drive the gate and source of the series-connected MOSFETs to a low voltage and the switch is off. When the charger controller is on, the charge MUX driver will keep the MOSFETs off until the voltage at CSN rises at least 35mV above the battery voltage. GCH1 is then driven with an error amplifier EAC until the voltage between BAT1 and CSN satisfies the error amplifier or until GCH1 is clamped by the internal Zener diode. The time required to close the switch could be quite long (many ms) due to the small currents output by the error amp and depending upon the size of the MOSFET switch.

If the voltage at CSN decreases below V_{BAT1} – 20mV, a comparator CC quickly turns off the MOSFETs to prevent reverse current from flowing in the switches. In essence, this system performs as a low forward voltage diode. Operation is identical for BAT2.

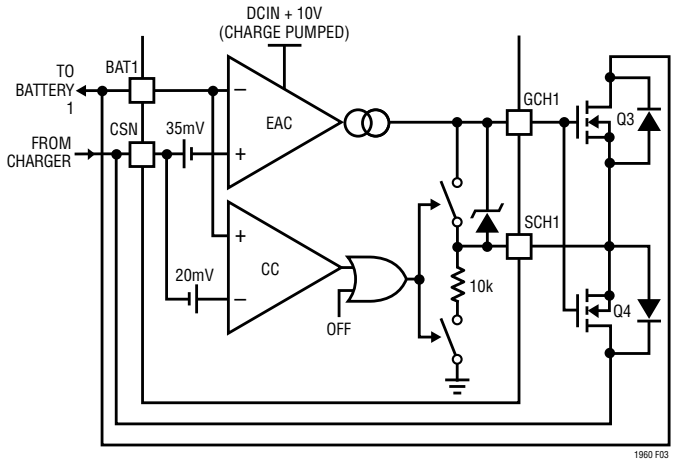


Figure 3. Charge MUX Switch Driver Equivalent Circuit

OPERATION

Dual Charging

Note that the charge MUX switch drivers will operate together to allow both batteries to be charged simultaneously. If both charge MUX switch drivers are enabled, only the battery with the lowest voltage will be charged until its voltage rises to equal the higher voltage battery. The charge current will then share between the batteries according to the capacity of each battery.

If both batteries are selected for charging, only batteries with voltages above V_{CHMIN} are allowed to charge. Dual charging is not allowed when the low current mode of the IDAC is selected. If dual charging is enabled when the IDAC enters low current mode, then only BAT1 will be charged.

Charger Start-Up

When the charger controller is enabled by the SPI Interface block, the charger output CSN will ramp from 0V until it exceeds the selected battery voltage. The clamp error amp is used to prevent the charger output from exceeding the selected battery voltage by more than 0.7V during the start-up transient while the charge MUX switches, have yet to close. Once the charge MUX switches have closed, the clamp releases I_{TH} to allow control by another loop.

PowerPath Controller

The PowerPath switches are turned on and off via the SPI interface, in any combination. The external P-MOSFETs are usually connected as an input switch and an output switch. The output switch PFET is connected in series with the input PFET and the positive side of the short-circuit sensing resistor, R_{SC}. The input switch is connected in series between the power source and the output PFET. The PowerPath switch driver equivalent circuit is shown in Figure 4. The output PFET is driven high and low by the output side driver controlling pin GXXO, the PFET is either on or off. The gate of the input PFET is driven by an error amplifier which monitors the voltage between the input power source (BAT1 in this case) and SCP. If the switch is turned off, the two outputs are driven to the higher of the two voltages present across the input/output terminals of the switch. When the switch is instructed to turn on, the output side driver immediately drives the gate of the output PFET approximately 6V below the highest of the voltages present at the input/output. When the output PFET turns on, the voltage at SCP will be pulled up to a diode drop below the source voltage by the bulk diode of the input PFET. If the source voltage is more than 25mV above SCP, EAP will drive the gate of the input PFET low until the input PFET turns on and reduces the voltage across the input/output to the EAP set point, or until the Zener clamp engages to limit the voltage applied to the input PFET. If the source voltage drops more than 20mV below SCP, then comparator CP turns on SWP to quickly prevent large reverse current in the switch. This operation mimics a diode with a low forward voltage drop.

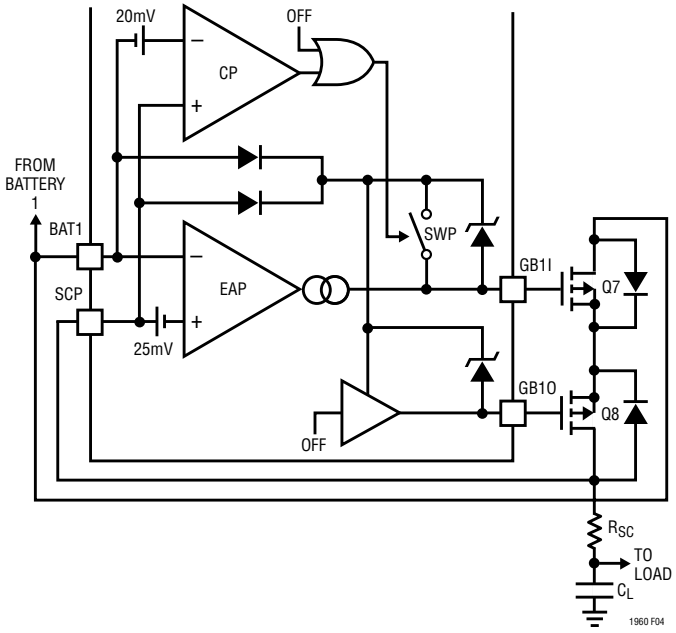


Figure 4. PowerPath Driver Equivalent Circuit

Autonomous PowerPath Switching

The LOPWR comparator monitors the voltage at the load through the resistor divider from pin SCN. If any POWER_BY bit is set and the LOPWR comparator trips, then all of the switches are turned on (3-diode mode) by the PowerPath controller to ensure that the system is powered from the source with the highest voltage. The PowerPath controller waits approximately 1 second, to allow power to stabilize, and then reverts to the previous PowerPath switch configuration. A power-fail counter is incremented to indicate that a failure has occurred. If the power-fail counter equals a value of 3, then the PowerPath controller sets the switches to 3-diode mode and the PF

OPERATION

bit is set in the status register. This is a three-strikes-and-you're-out process which is intended to debounce the PowerPath PF indicator. The power-fail counter is reset by a PowerPath SPI write.

Short-Circuit Protection

Short-circuit protection operates in both a current mode and a voltage mode. If the voltage between SCP and SCN exceeds the short-circuit comparator threshold V_{TSC} for more than 15ms, then all of the PowerPath switches are turned off and the FAULT bit (FA) is set. Similarly, if the voltage at SCN falls below 3V for more than 15ms, then all of the PowerPath switches are turned off and the FA bit is set. The FA bit is reset by removing all power sources and allowing the voltage at V_{PLUS} to fall below the UVLO threshold. If the FA bit is set, charging is disabled until V_{PLUS} exceeds the UVLO threshold and charging is requested via the SPI interface.

When a hard short-circuit occurs, it might pull all of the power sources down to near 0V potentials. The capacitors on V_{CC} and V_{PLUS} must be large enough to keep the circuit operating correctly during the 15ms short-circuit event. The charger will stop within a few microseconds leaving a small current which must be provided by the capacitor on V_{PLUS}. The recommended minimum values (1µF on V_{PLUS} and 2µF on V_{CC}, including tolerances) should keep the LTC1960 operating above the UVLO trip voltage long enough to perform the short-circuit function when the input voltages are greater than 8V. Increasing the capacitor across V_{CC} to 4.7µF will allow operation down to the recommended 6V minimum.

Fast PowerPath Turn-Off

All of the PowerPath switches can be forced off by setting the DCDIV pin to a voltage between 8V and 10V. This will have the same effect as a short-circuit event. The PF status bit will also be set. DCDIV must be less than 5V and V_{PLUS} must decrease below the UVLO threshold to re-enable the PowerPath switches.

Power-Up Strategy

All three PowerPath switches are turned on after V_{PLUS} exceeds the UVLO threshold for more than 250ms. This delay is to prevent oscillation from a turn-on transient near the UVLO threshold.

The Voltage DAC Block

The voltage DAC (VDAC) is a delta-sigma modulator which controls the effective value of an internal resistor, R_{VSET} = 7.2k, used to program the maximum charger voltage. Figure 5 is a simplified diagram of the VDAC operation. The charger monitor MUX is connected to the appropriate battery indicated by the CHARGE_BATx bit. The delta-sigma modulator and switch SWV convert the VDAC value, received via SPI communication, to a variable resistance equal to $(11/8)R_{VSET}/(VDAC_{(VALUE)}/2047)$. In regulation, V_{SET} is servo driven to the 0.8V reference voltage, V_{REF}.

Therefore, programmed voltage is:

$$V_{BATx} = (8/11)\ V_{REF}\ 405.3k/7.2k \bullet (VDAC_{(VALUE)}/2047) + V_{REF} = 32{,}752mV \bullet (VDAC_{(VALUE)}/2047) + 0.8V$$

Note that the reference voltage must be subtracted from the VDAC value in order to obtain the correct output voltage. This value is $V_{REF}/16mV = 50\ (32_{HEX})$.

Capacitors C_{B1} and C_{B2} are used to average the voltage present at the V_{SET} pin as well as provide a zero in the voltage loop to help stability and transient response time to voltage variations. See the Applications Information section.

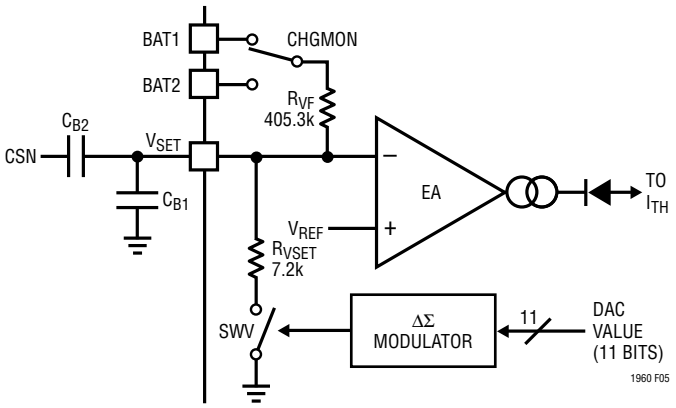


Figure 5. Voltage DAC Operation

OPERATION

The Current DAC Block

The current DAC is a delta-sigma modulator which controls the effective value of an internal resistor, R_{SET} = 18.77k, used to program the maximum charger current. Figure 6 is a simplified diagram of the DAC operation. The delta-sigma modulator and switch convert the IDAC value, received via SPI communication, to a variable resistance equal to $1.25R_{SET}/(IDAC_{(VALUE)}/1023)$. In regulation, I_{SET} is servo driven to the 0.8V reference voltage, V_{REF}, and the current from R_{SET} is matched against a current derived from the voltage between pins CSP and CSN. This current is $(V_{CSP} – V_{CSN})/3k$.

Therefore, programmed current is:

$$I_{AVG} = \frac{V_{REF} \bullet 3k}{(1.25R_{SNS}\ R_{SET})} \bullet \left(\frac{IDAC_{(VALUE)}}{1023}\right)$$

When the low current mode bit (D10) is set to 1, the current DAC enters a different mode of operation. The current DAC output is pulse-width modulated with a high frequency clock having a duty cycle value of 1/8. Therefore, the maximum output current provided by the charger is $I_{MAX}/8$. The delta-sigma output gates this low duty cycle signal on and off. The delta-sigma shift registers are then clocked at a slower rate, about 40ms/bit, so that the charger has time to settle to the $I_{MAX}/8$ value. The resulting average charging current is equal to 1/8 of the current programmed in normal mode. Dual battery charging is disabled in low current mode. If both batteries are selected for charging, then only BAT1 will charge.

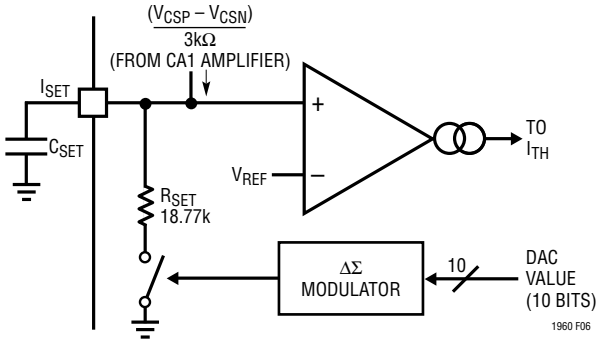


Figure 6. Current DAC Operation

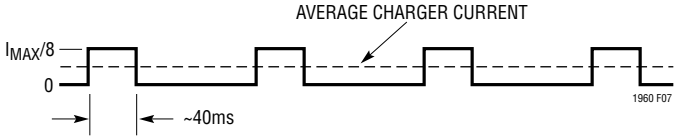


Figure 7. Charging Current Waveform in Low Current Mode

APPLICATIONS INFORMATION

Automatic Current Sharing

In a dual parallel charge configuration, the LTC1960 does not actually control the current flowing into each individual battery. The capacity, or amp-hour rating, of each battery determines how the charger current is shared. This automatic steering of current is what allows both batteries to reach their full capacity points at the same time. In other words, given all other things equal, charge termination will happen simultaneously.

A battery can be modeled as a huge capacitor and hence governed by the same laws.

$I = C \bullet (dV/dT)$, where:

I = The current flowing through the capacitor

C = Capacity rating of battery (using amp-hour value instead of capacitance)

dV = Change in voltage

dt = Change in time

The equivalent model of a set or parallel batteries is a set of parallel capacitors. Since they are in parallel, the change in voltage over change in time is the same for both batteries 1 and 2.

$$\frac{dV}{dt_{BAT1}} = \frac{dV}{dt_{BAT2}}$$

From here we can simplify.

$$I_{BAT1}/C_{BAT1} = dV/dt = I_{BAT2}/C_{BAT2}$$

$$I_{BAT2} = I_{BAT1}\ C_{BAT2}/C_{BAT1}$$

At this point you can see that the current divides as the ratio of the two batteries capacity ratings. The sum of the current into both batteries is the same as the current being supply by the charger. This is independent of the mode of the charger (CC or CV).

$$I_{CHRG} = I_{BAT1} + I_{BAT2}$$

From here we solve for the actual current for each battery.

$$I_{BAT2} = I_{CHRG}\ C_{BAT2}/(C_{BAT1} + C_{BAT2})$$

$$I_{BAT1} = I_{CHRG}\ C_{BAT1}/(C_{BAT1} + C_{BAT2})$$

Please note that the actual observed current sharing will vary from manufactures claimed capacity ratings since it is actual physical capacity rating at the time of charge. Capacity rating will change with age and use and hence the current sharing ratios can change over time.

In dual charge mode, the charger uses feedback from the BAT2 input to determine charger output voltage. When charging batteries with significantly different initial states of charge (i.e., one almost full, the other almost depleted), the full battery will get a much lower current. This will cause a voltage difference across the charge MUX switches, which may cause the BAT1 voltage to exceed the programmed voltage. Using MOSFETs in the charge MUX with lower $R_{DS(ON)}$ will alleviate this problem.

Adapter Limiting

An important feature of the LTC1960 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 8 senses the voltage across R_{CL}, connected between the CLP and DCIN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to $100mV/R_{CL}$. A lowpass filter formed by 5kΩ and 0.1µF is required to eliminate switching noise. If the current limit is not used, CLP should be connected to DCIN.

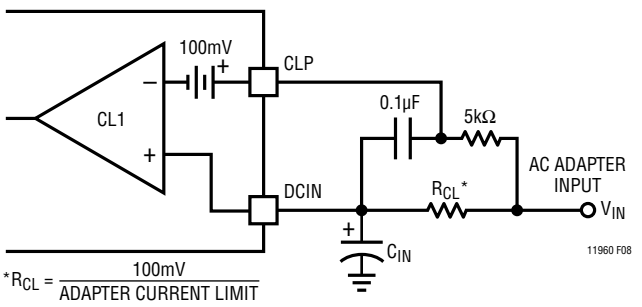


Figure 8. Adapter Current Limiting

Rev. C

APPLICATIONS INFORMATION

Watchdog Timer

Charging will begin when either CHARGE_BAT1 or CHARGE_BAT2 bits are set in the charger register (address: 111). Charging will stop if the charger register is not updated prior to the expiration of the watchdog timer. Simply repeating the same data transmission to the charger register at a rate higher than once per second will ensure that charging will continue uninterrupted.

Extending System to More Than Two Batteries

The LTC1960 can be extended to manage systems with more than three sources of power. Contact Linear Technology Applications Engineering for more information.

Charging Depleted Batteries

Some batteries contain internal protection switches that disconnect a load if the battery voltage falls below what is considered a reasonable minimum. In this case, the charger may not start because the voltage at the battery terminal is less than 5V. The low current mode of the IDAC must be used in this case to condition the battery. In low current mode, there is no minimum voltage requirement (but dual charging is not allowed). Usually, the battery will detect that it is being charged and then close its protection switch, which will allow the IDAC to switch to normal mode. Smart batteries require that charging current not exceed 100mA until valid charging voltage and charging current parameters are transmitted via the SMBus. The low current IDAC mode is ideal for this purpose.

Starting Charge with Dissimilar Batteries in Dual Charge Mode

When charging batteries of different charger termination voltages, the charger should be started using the following procedure:

Step 1. Select only the lowest termination voltage battery for charging, and set the charger to its charging parameters.

Step 2. When the battery current is flowing into that battery, change to dual charging mode (without stopping the charger) and set the appropriate charging parameters for this dual charger condition.

If this procedure is not followed, and BAT2 is significantly higher voltage than BAT1, the charger could refuse to charge either battery.

Charge Termination Issues

Batteries with constant-current charging and voltage-based charger termination might experience problems with reductions of charger current caused by adapter limiting. It is recommended that input limiting feature be defeated in such cases. Consult the battery manufacturer for information on how your battery terminates charging.

Setting Output Current Limit

The full-scale output current setting of the IDAC will produce V_{MAX} = 102.3mV between CSP and CSN. To set the full-scale current of the DAC simply divide V_{MAX} by R_{SNS}.

This is expressed by the following equation:

$$R_{SNS} = 0.1023/I_{MAX}$$

Table 1. Recommended R_{SNS} Resistor Values

I_{MAX} (A)	R_{SNS} (Ω) 1%	R_{SNS} (W)
1.023	0.100	0.25
2.046	0.050	0.25
4.092	0.025	0.5
8.184	0.012	1

Use resistors with low ESL.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher V_{IN}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. In no case should

APPLICATIONS INFORMATION

ΔI_L exceed 0.6(I_{MAX}) due to limits imposed by IREV and CA1. Remember the maximum ΔI_L occurs at the maximum input voltage. In practice, 10µH is the lowest value recommended for use.

Charger Switching Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with the LTC1960 charger: An N-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the V_{CC} voltage. This voltage is typically 5.2V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the B_{VDSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. The LTC1960 charger is always operating in continuous mode so the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = V_{OUT}/V_{IN}$$

$$\text{Synchronous Switch Duty Cycle} = (V_{IN} - V_{OUT})/V_{IN}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = V_{OUT}/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)} + k(V_{IN})^2 (I_{MAX})(C_{RSS})(f)$$

$$P_{SYNC} = (V_{IN} - V_{OUT})/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)\ R_{DS(ON)}$$

Where $\delta\Delta T$ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current. Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short-circuit when the duty cycle in this switch is nearly 100%. The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

If the LTC1960 charger is to operate in low dropout mode or with a high duty cycle greater than 85%, then the topside N-channel efficiency generally improves with a larger MOSFET. Using asymmetrical MOSFETs may achieve cost savings or efficiency gains.

The Schottky diode D1, shown in the Typical Application on the back page, conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 4A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance. The diode may be omitted if the efficiency loss can be tolerated.

Calculating IC Power Dissipation

The power dissipation of the LTC1960 is dependent upon the gate charge of Q_{TG} and Q_{BG} (refer to Typical Application). The gate charge is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the FET.

$$P_D = (V_{DCIN} - V_{VCC}) \bullet [f_{OSC}(Q_{TG} + Q_{BG}) + I_{VCC}] + V_{DCIN} \bullet I_{DCIN}$$

Example: $V_{VCC} = 5.2V$, $V_{DCIN} = 19V$, $f_{OSC} = 345kHz$, $Q_{G2} = Q_{G3} = 15nC$, $I_{VCC} = 0mA$.

$$P_D = 165mW$$

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V_{SET}/I_{SET} Capacitors

Capacitor C7 is used to filter the delta-sigma modulation frequency components to a level which is essentially DC. Acceptable voltage ripple at I_{SET} is about $10mV_{P-P}$. Since the period of the delta-sigma switch closure, $T_{\Delta\Sigma}$, is about 10µs and the internal IDAC resistor, R_{SET}, is 18.77k, the ripple voltage can be approximated by:

$$\Delta V_{ISET} = \frac{V_{REF} \bullet T_{\Delta\Sigma}}{R_{SET} \bullet C7}$$

Then the equation to extract C7 is:

$$C7 = \frac{V_{REF} \bullet T_{\Delta\Sigma}}{\Delta V_{ISET} \bullet R_{SET}}$$

$$= 0.8/0.01/18.77k(10\mu s) \cong 0.043\mu F$$

In order to prevent overshoot during start-up transients, the time constant associated with C7 must be shorter than the time constant of C5 at the I_{TH} pin. If C7 is increased to improve ripple rejection, then C5 should be increased proportionally and charger response time to average current variation will degrade.

Capacitor C_{B1} and C_{B2} are used to filter the VDAC delta-sigma modulation frequency components to a level which is essentially DC. C_{B2} is the primary filter capacitor and C_{B1} is used to provide a zero in the response to cancel the pole associated with C_{B2}. Acceptable voltage ripple at V_{SET} is about $10mV_{P-P}$. Since the period of the delta-sigma switch closure, $T_{\Delta\Sigma}$, is about 11µs and the internal VDAC resistor, R_{VSET}, is 7.2kΩ, the ripple voltage can be approximated by:

$$\Delta V_{VSET} = \frac{V_{REF} \bullet T_{\Delta\Sigma}}{R_{VSET}(C_{B1} || C_{B2})}$$

Then the equation to extract $C_{B1} || C_{B2}$ is:

$$C_{B1} || C_{B2} = \frac{V_{REF} \bullet T_{\Delta\Sigma}}{R_{VSET} \Delta V_{VSET}}$$

C_{B2} should be 10× to 20× C_{B1} to divide the ripple voltage present at the charger output. Therefore C_{B1} = 0.01µF and C_{B2} = 0.1µF are good starting values. In order to prevent overshoot during start-up transients the time constant associated with C_{B2} must be shorter than the time constant of C5 at the I_{TH} pin. If C_{B2} is increased to improve ripple rejection, then C5 should be increased proportionally and charger response time to voltage variation will degrade.

Input and Output Capacitors

In the 4A Lithium Battery Charger (Typical Application section), the input capacitor (C_{IN}) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one-half of output charging current. Actual capacitance value is not critical. Solid tantalum, low ESR capacitors have a high ripple current rating in a relatively small surface mount package, *but caution must be used when tantalum capacitors are used for input or output bypass.* High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Only Kemet T495 series of "surge robust" low ESR tantalums are rated for high surge conditions such as battery to ground.

The relatively high ESR of an aluminum electrolytic for C15, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event.

Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (at least 20µF) from Tokin, United Chemi-Con/Marcon, et al. Other alternative capacitors include OSCON capacitors from Sanyo.

The output capacitor (C_{OUT}) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29(V_{BAT})\left(1 - \frac{V_{BAT}}{V_{DCIN}}\right)}{(L1)(f)}$$

For example:

V_{DCIN} = 19V, V_{BAT} = 12.6V, L1 = 10µH, and f = 300kHz, I_{RMS} = 0.41A.

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EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C_{OUT} is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

PowerPath and Charge MUX MOSFET Selection

Three pairs of P-channel MOSFETs must be used with the wall adapter and the two battery discharge paths. Two pairs of N-channel MOSFETs must be used with the battery charge path. The nominal gate drive levels are set by the clamp drive voltage of their respective control circuitry. This voltage is typically 6.25V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the B_{VDSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input voltage and maximum output current. For the N-channel charge path, the maximum current is the maximum programmed current to be used. For the P-channel discharge path maximum current typically occurs at end of life of the battery when using only one battery. The upper limit of $R_{DS(ON)}$ value is a function of the *actual* power dissipation capability of a given MOSFET package that must take into account the PCB layout. As a starting point, without knowing what the PCB dissipation capability would be, derate the package power rating by a factor of two.

$$R_{DS(ON)MAX} = \frac{P_{MOSFET}}{2(I_{MAX})^2}$$

If you are using a dual MOSFET package with both MOSFETs in series, you must cut the package power rating in half again and recalculate.

$$R_{DS(ON)MAX} = \frac{P_{MOSFETDUAL}}{4(I_{MAX})^2}$$

If you use identical MOSFETs for both battery paths, voltage drops will track over a wide current range. The LTC1960 linear 25mV CV drop regulation will not occur until the current has dropped below:

$$I_{LINEARMAX} = \frac{25mV}{2R_{DS(ON)MAX}}$$

However, if you try to use the above equation to determine $R_{DS(ON)}$ to force linear mode at full current, the MOSFET $R_{DS(ON)}$ value becomes unreasonably low for MOSFETs available at this time. The need for the LTC1960 voltage drop regulation only comes into play for parallel battery configurations that terminate charge or discharge using voltage. At first this seems to be a problem, but there are several factors helping out:

1. When batteries are in parallel current sharing, the current flow through any one battery is less than if it is running standalone.
2. Most batteries that charge in constant-voltage mode, such as Li-Ion, charge terminate at a current value of C/10 or less which is well within the linear operation range of the MOSFETs.
3. Voltage tracking for the discharge process does not need such precise voltage tracking values.

The LTC1960 has two transient conditions that force the discharge path P-channel MOSFETs to have two additional parameters to consider. The parameters are gate charge Q_{GATE} and single pulse power capability.

When the LTC1960 senses a LOW_POWER event, all the P-channel MOSFETs are turned on simultaneously to allow voltage recovery due to a loss of a given power source. However, there is a delay in the time it takes to turn on all the MOSFETs. Slow MOSFETs will require more bulk capacitance to hold up all the system's power supply function during the transition and fast MOSFET will require less bulk capacitance. The transition speed of a MOSFET to an on or off state is a direct function of the MOSFET gate charge.

$$t = \frac{Q_{GATE}}{I_{DRIVE}}$$

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I_{DRIVE} is the fixed drive current into the gate from the LTC1960 and "t" is the time it takes to move that charge to a new state and change the MOSFET conduction mode. Hence, time is directly related to Q_{GATE}. Since Q_{GATE} goes up with MOSFETs of lower $R_{DS(ON)}$, choosing such MOSFETs has a counterproductive increase in gate charge making the MOSFET slower. Please note that the LTC1960 recovery time specification only refers to the time it takes for the voltage to recover to the level just prior to the LOW_POWER event as opposed to full voltage.

The single pulse current rating of the MOSFET is important when a short-circuit takes place. The MOSFET must survive a 15ms overload. MOSFETs of lower $R_{DS(ON)}$ or MOSFETs that use more powerful thermal packages will have a high power surge rating. Using too small of a pulse rating will allow the MOSFET to blow to the open-circuit condition instantly like a fuse. Typically there is no outward sign of failure because it happens so fast. Please measure the surge current for all discharge power paths under worse case conditions and consult the MOSFET data sheet for the limitations. Voltage sources with the highest voltage and the most bulk capacitance are often the biggest risk. Specifically the MOSFETs in the wall adapter path with wall adapters of high voltage, large bulk capacitance and low resistance DC cables between the adapter and device are the most common failures. Remember to *only* use the *real* wall adapter with a production DC power cord when performing the wall adapter path test. The use of a laboratory power supply is unrealistic for this test and will force you to over specify the MOSFET ratings. A battery pack usually has enough series resistance to limit the peak current or are too low in voltage to create enough instantaneous power to damage their respective PowerPath MOSFETs.

PCB Layout Considerations

For maximum efficiency, the switch node rise and fall time is kept as short as possible. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential.

1. Keep the highest frequency loop path as small and tight as possible. This includes the bypass capacitors, with the higher frequency capacitors being closer to the noise source than the lower frequency capacitors. The highest frequency switching loop has the highest layout priority. For best results, avoid using vias in this loop and keep the entire high frequency loop on a single external PCB layer. If you must, use multiple vias to keep the impedance down (see Figure 9).

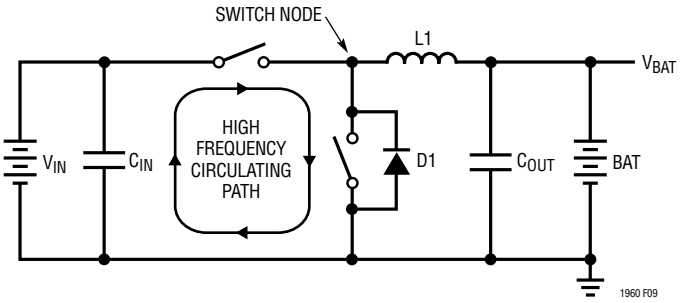


Figure 9. High Speed Switching Path

2. Run long power traces in parallel. Best results are achieved if you run each trace on separate PCB layer one on top of the other for maximum capacitance coupling and common mode noise rejection.
3. If possible, use a ground plane under the switcher circuitry to minimize capacitive interplane noise coupling.
4. Keep signal or analog ground separate. Tie this analog ground back to the power supply at the output ground using a single point connection.
5. For best current programming accuracy provide a Kelvin connection from R_{SENSE} to CSP and CSN. See Figure 10 as an example.

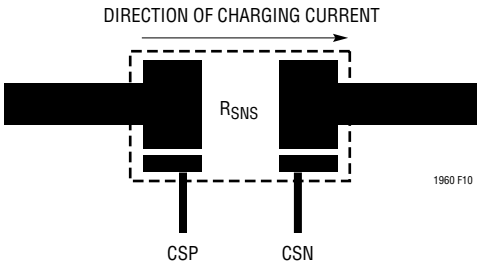
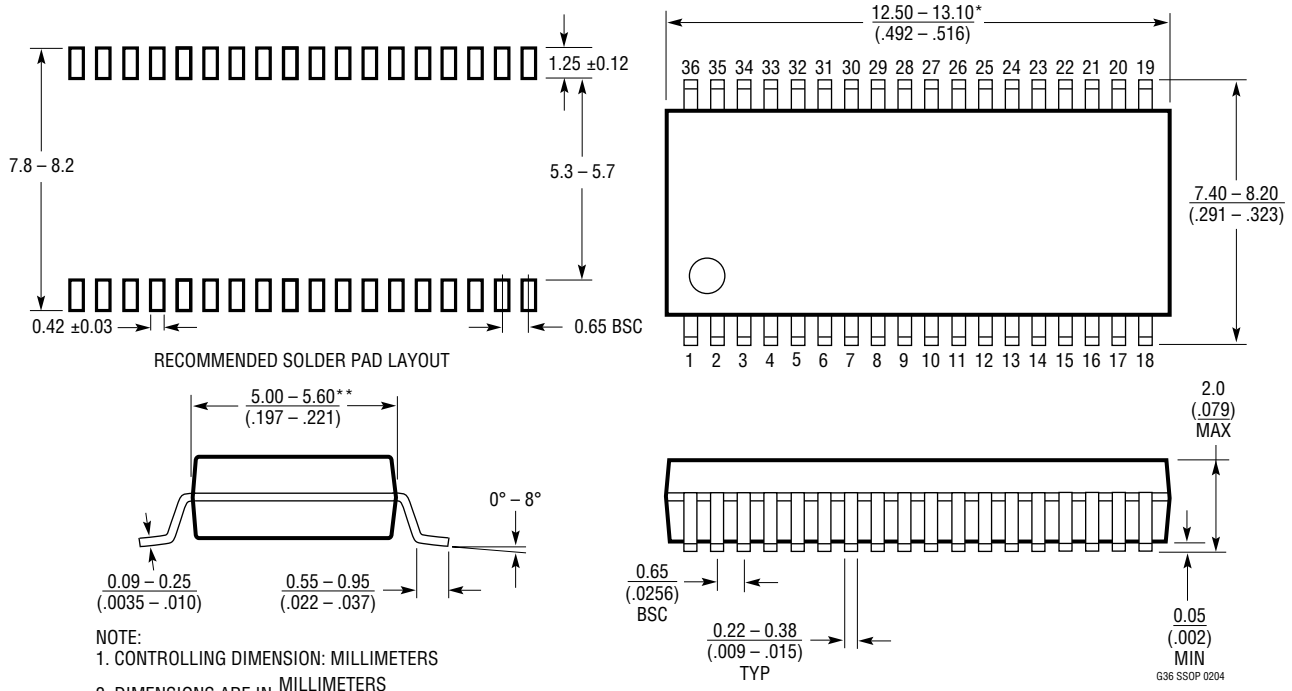


Figure 10. Kelvin Sensing of Charging Current

Rev. C

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



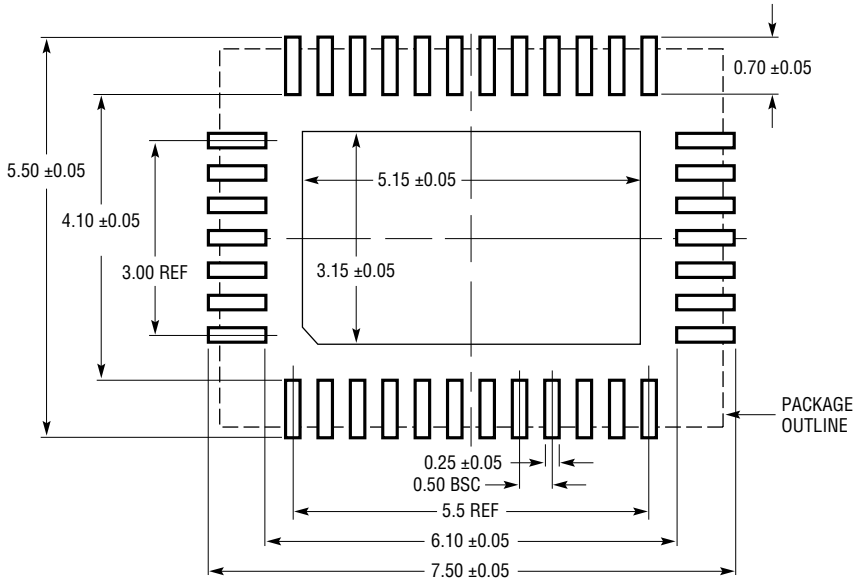
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

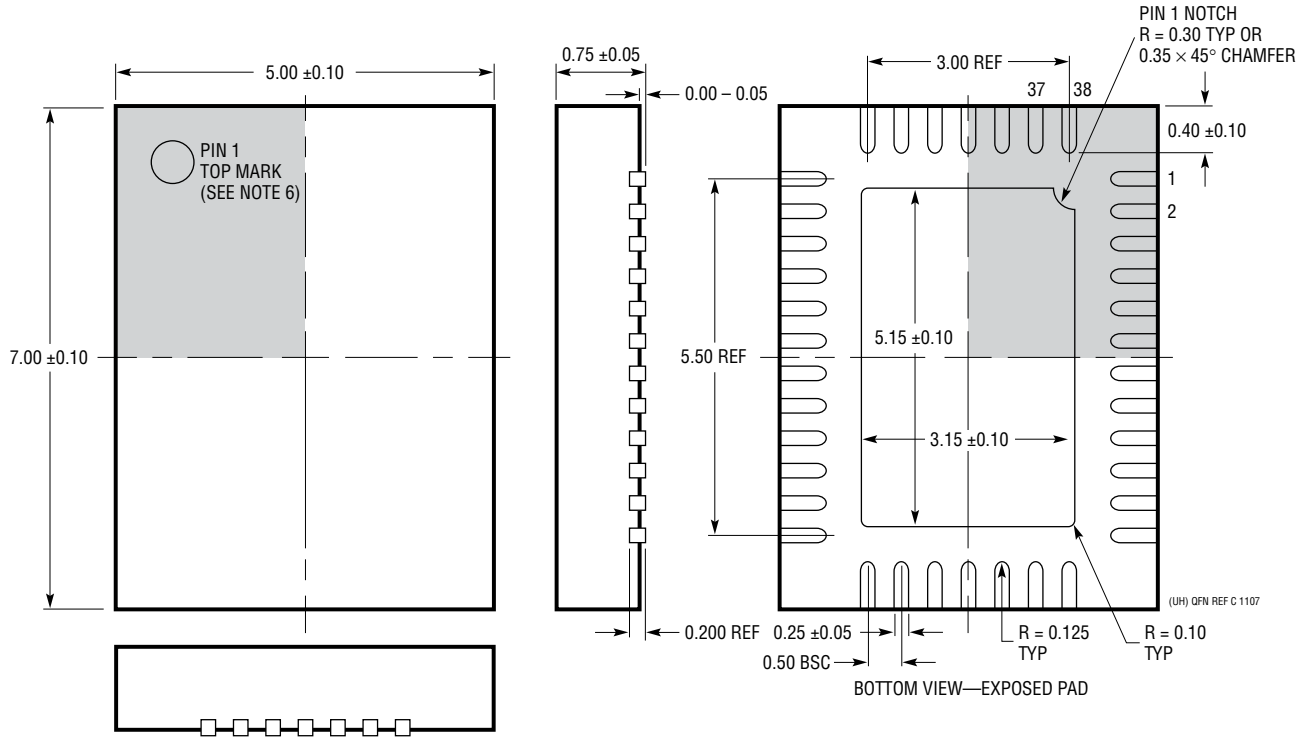
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

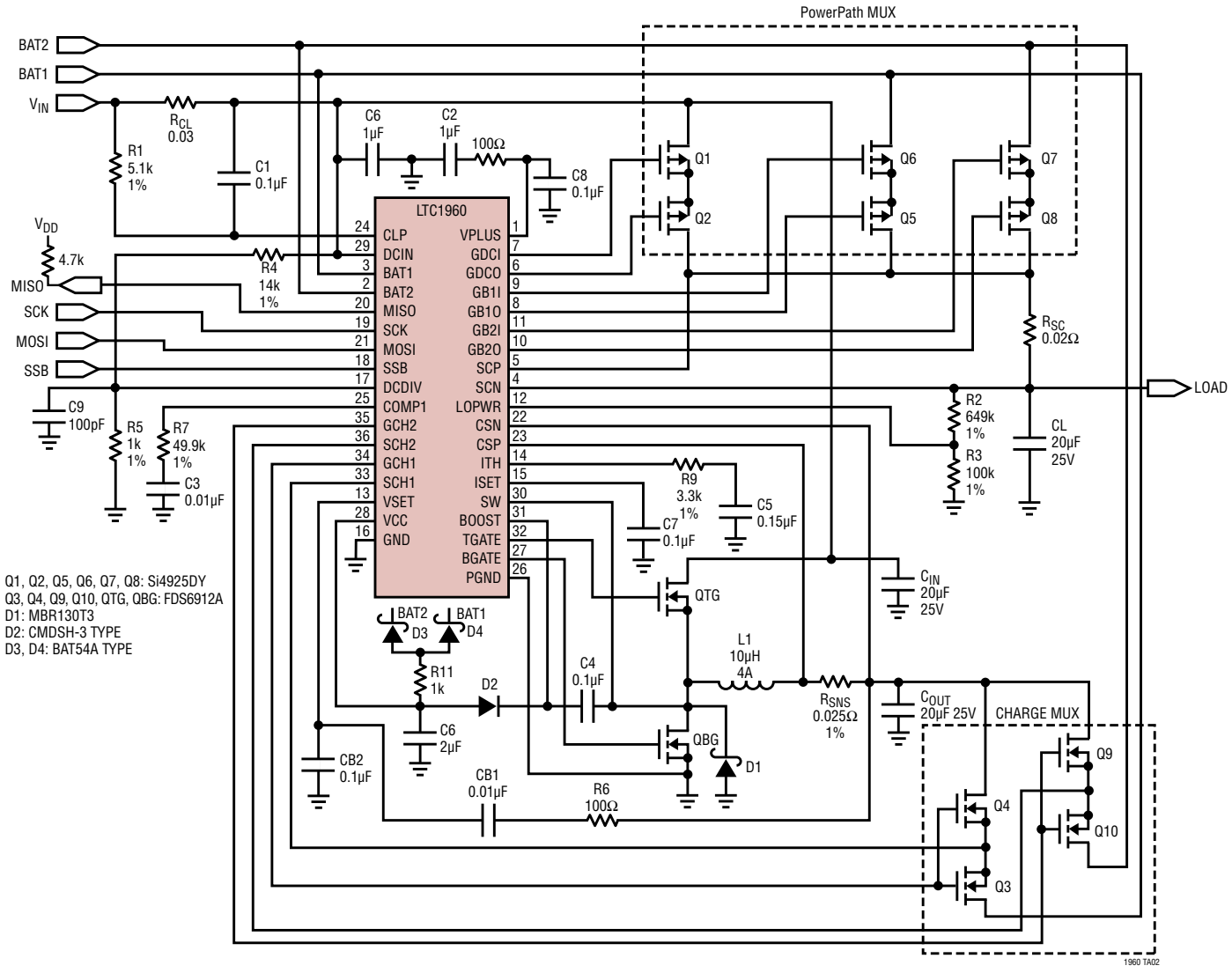
Rev. C

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	04/11	Updated Absolute Maximum Ratings section.	2
		Added Note 8.	5
		Updated Pin Functions.	8, 9
		Updated equation in “The Current DAC Block” section.	18
		Updated equation in “Calculating IC Power Dissipation” section.	21
		Updated Typical Application.	28
C	01/20	SPI address change.	13

TYPICAL APPLICATION (LTC1960CG Pin Numbers Shown)

Dual Battery Selector and 4A Charger



Q1, Q2, Q5, Q6, Q7, Q8: Si4925DY
Q3, Q4, Q9, Q10, QTG, QBG: FDS6912A
D1: MBR130T3
D2: CMDSH-3 TYPE
D3, D4: BAT54A TYPE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1505	High Efficiency Battery Charger	Up to 97% Efficiency; AC Adapter Current Limit
LTC1628-PG	2-Phase, Dual Synchronous Step-Down Controller	Minimizes C_{IN} and C_{OUT}; Power Good Output; $3.5V \le V_{IN} \le 36V$
LTC1709	2-Phase, Dual Synchronous Step-Down Controller with VID	Up to 42A Output; Minimum C_{IN} and C_{OUT}; Uses Smallest Components for Intel and AMD Processors
LTC3711	No R_{SENSE}™ Synchronous Step-Down Controller with VID	$3.5V \le V_{IN} \le 36V$; $0.925V \le V_{OUT} \le 2V$; for Transmeta, AMD and Intel Mobile Processors
LTC1759	SMBus Controlled Smart Battery Charger	Synchronous Operation for High Efficiency; Integrated SMBus Accelerator; AC Adapter Current Limit
LT1769	2A Battery Charger	Constant-Current/Constant-Voltage Switching Regulator; Input Current Limiting Maximizes Charge Current