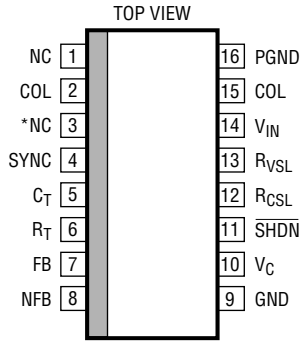
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (V_{IN}) 30V
Switch Voltage (COL) 35V
$\overline{SHDN}$ Pin Voltage 30V
Feedback Pin Current (FB) 10mA
Negative Feedback Pin Current (NFB) ..... ±10mA

Operating Junction Temperature Range
LT1534C ..... 0°C to 125°C
LT1534I ..... –40°C to 125°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION

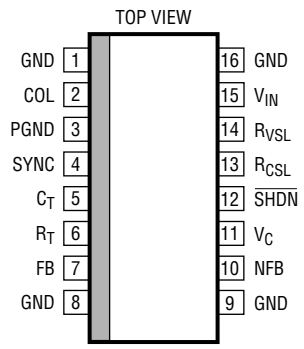


S PACKAGE
16-LEAD PLASTIC SO
*DO NOT CONNECT

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1534CS
LT1534IS



S PACKAGE
16-LEAD PLASTIC SO
**FOUR CORNER PINS ARE FUSED TO INTERNAL DIE ATTACH PADDLE FOR HEAT SINKING. CONNECT THESE FOUR PINS TO EXPANDED PC LANDS FOR PROPER HEAT SINKING.

T_{JMAX} = 125°C, θ_{JA} = 50°C/W

ORDER PART NUMBER

LT1534CS-1
LT1534IS-1

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V, V_C = 0.9V, V_{FB} = V_{REF}. COL, $\overline{SHDN}$, NFB, all other pins open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
V_{IN}	Recommended Operating Range		●	2.7		23	V
$V_{IN(MIN)}$	Minimum Input Voltage		●		2.55	2.7	V
I_{VIN}	Operating Supply Current	2.7V ≤ V_{IN} ≤ 23V, R_{VSL}, R_{CSL}, R_T = 17k	●		12	30	mA
$I_{VIN(OFF)}$	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 23V, $V_{\overline{SHDN}}$ = 0V 2.7V ≤ V_{IN} ≤ 23V, $V_{\overline{SHDN}}$ = 0V	● 		12 12	50 30	µA µA
$V_{\overline{SHDN}}$	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 23V	●	0.4	0.8	1.2	V
I_{SHDN}	Shutdown Input Current				–2		µA
Error Amplifiers							
V_{REF}	Reference Voltage	Measured at Feedback Pin	 ●	1.235 1.215	1.250 1.250	1.265 1.275	V V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}	●		250	900	nA
FB_{REG}	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 23V	●		0.003	0.03	%/V

ELECTRICAL CHARACTERISTICS

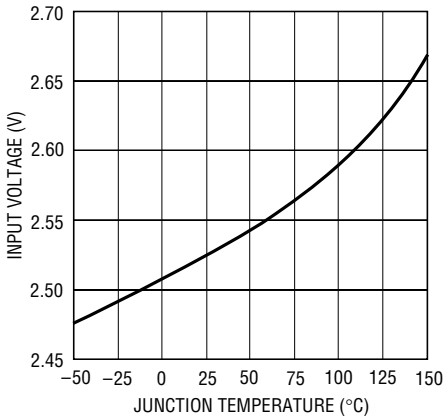
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V, V_C = 0.9V, V_{FB} = V_{REF}. COL, $\overline{SHDN}$, NFB, all other pins open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifiers							
V_{NFR}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin with Feedback Pin Open	●	–2.550	–2.500	–2.420	V
I_{NFR}	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	–37	–25		µA
NFB_{REG}	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 23V	●		0.002	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	1100 700	1500	1900 2300	µmho µmho
I_{ESK}	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 0.9V, $V_{\overline{SHDN}}$ = 1V	●	120	200	350	µA
I_{ESRC}	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 0.9V, $V_{\overline{SHDN}}$ = 1V	●	120	200	350	µA
V_{CLH}	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V			1.33		V
V_{CLL}	Error Amplifier Clamp Voltage	Low Clamp, V_{FB} = 1.5V			0.1		V
A_V	Error Amplifier Voltage Gain			180	250		V/V
Oscillator and Sync							
f_{MAX}	Maximum Switch Frequency				250		kHz
f_{SYNC}	Synchronization Frequency Range	f_{OSC} = 250kHz	●			375	kHz
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ
V_{FBfs}	FB Pin Threshold for Frequency Shift	5% Reduction from Nominal			0.4		V
Output Switches							
DC_{MAX}	Maximum Switch Duty Cycle	R_{VSL} = R_{CSL} = 4.9k, f_{OSC} = 25kHz	●	88	91		%
t_{IBL}	Switch Current Limit Blanking Time				200		ns
BV_{COL}	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 23V	●	35			V
R_{ON}	Output Switch-On Resistance	I_{COL} = 1.5A, Both COL Pins Tied Together	●		0.25	0.43	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 30% Duty Cycle = 80%		2 1.6			A A
$\Delta I_{IN}/\Delta I_{SW}$	Supply Current Increase During Switch-On Time				16		mA/A
Slew Control							
V_{SLEWR}	Output Voltage Slew Rising Edge	R_{VSL}, R_{CSL} = 17k			11		V/µs
V_{SLEWF}	Output Voltage Slew Falling Edge	R_{VSL}, R_{CSL} = 17k			14.5		V/µs
I_{SLEWR}	Output Current Slew Rising Edge	R_{VSL}, R_{CSL} = 17k			1.3		A/µs
I_{SLEWF}	Output Current Slew Falling Edge	R_{VSL}, R_{CSL} = 17k			1.3		A/µs

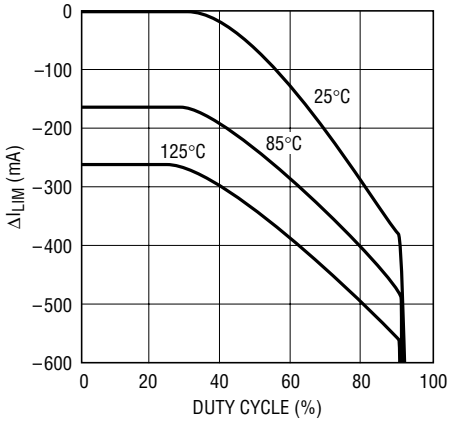
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TYPICAL PERFORMANCE CHARACTERISTICS

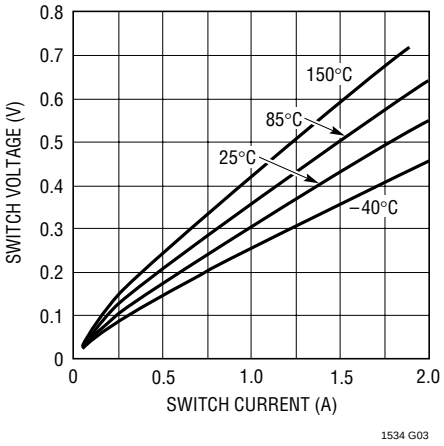
Minimum Input Voltage (V_{IN}) vs Temperature



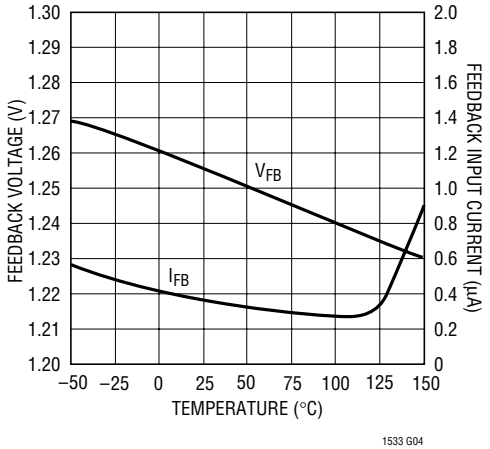
Change in Maximum Switch Current (I_{LIM}) vs Duty Cycle



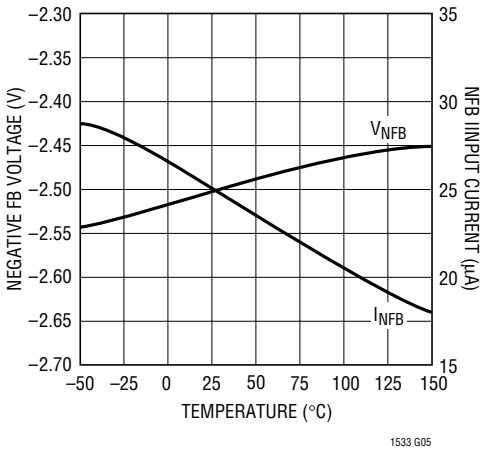
Output Switch Saturation Voltage vs Switch Current



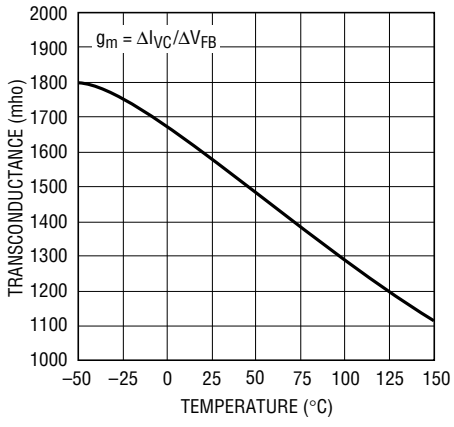
Feedback Voltage and Input Current vs Temperature



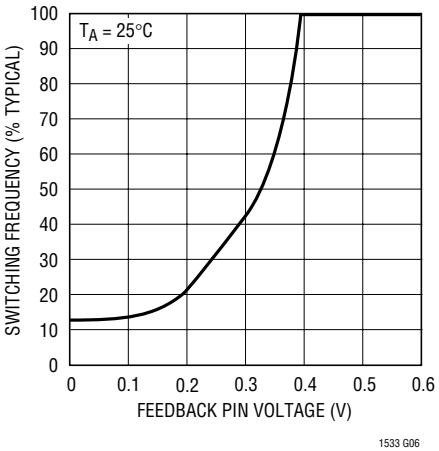
Negative Feedback Voltage and Input Current vs Temperature



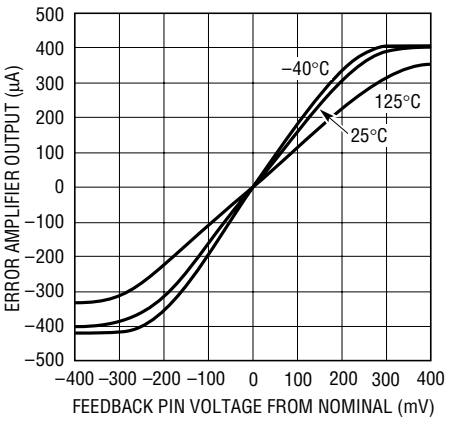
Error Amplifier Transconductance vs Temperature



Switching Frequency vs Feedback Pin Voltage

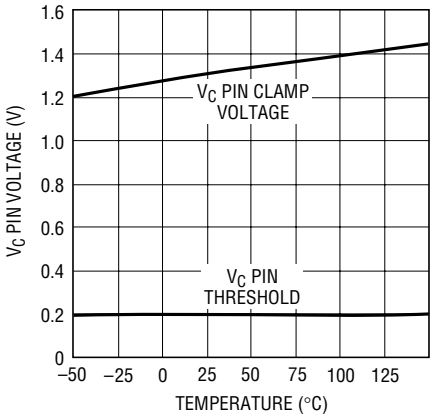


Error Amplifier Output Current (V_C)

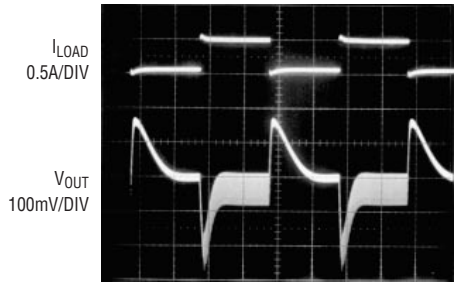


TYPICAL PERFORMANCE CHARACTERISTICS

V_C Pin Threshold and Clamp Voltage vs Temperature

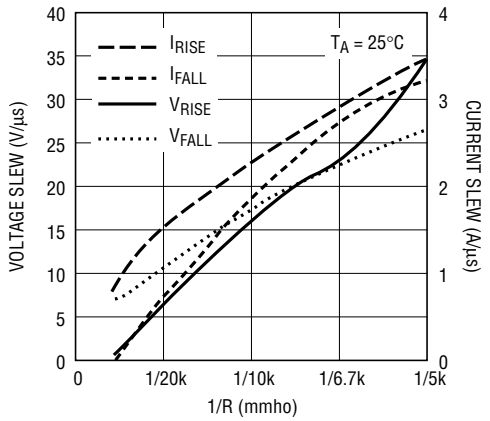


Load Transient Response

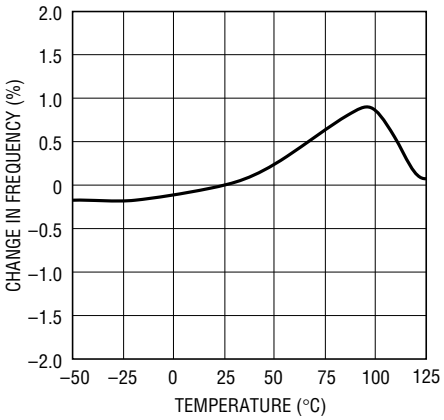


V_{IN} = 3.3V 500µs/DIV 1534 G10
V_{OUT} = 5V (NODE A)
I_{LOAD} = 0.1A TO 0.5A
FIGURE 1 CIRCUIT

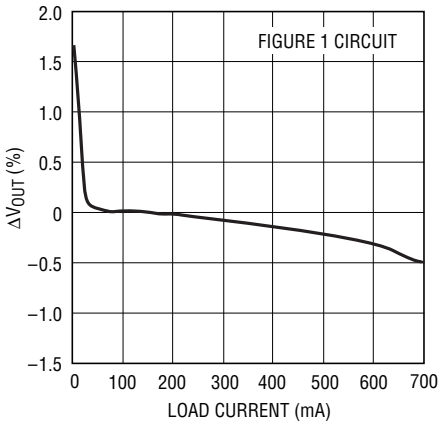
Typical Output Switch Voltage and Current Slew Rates vs Slew Setting Resistance (R_{VSL} = R_{CSL})



Percent Change in Oscillator Frequency vs Temperature (NPO Cap and Metal Film R)



Load Regulation



PIN FUNCTIONS (LT1534/LT1534-1)

COL (Pins 2, 15/Pin 2): These two pins should be connected together externally to create the collector of the power switch. The emitter returns to PGND through a sense resistor. Large currents flow into these pins so it is desirable to keep external trace lengths short to minimize radiation.

SYNC (Pin 4): The SYNC pin can be used to synchronize the oscillator to an external clock (see Oscillator Sync in Applications Information section for more details). The SYNC pin may either be floated or tied to ground if not used.

C_T (Pin 5): The oscillator capacitor pin is used in conjunction with R_T to set the oscillator frequency. For R_T = 16.9k,

$$C_{T(NF)} = 129/f_{OSC(kHz)}$$

R_T (Pin 6): The oscillator resistor pin is used to set the charge and discharge currents of the oscillator capacitor. The nominal value is 16.9k. It is possible to adjust this resistance ±25% to get a more accurate oscillator frequency.

FB (Pin 7): The feedback pin is used for positive voltage sensing and oscillator frequency shifting during start-up and short-circuit conditions. It is the inverting input to the error amplifier. The noninverting input of this amplifier connects internally to a 1.25V reference. This pin should be left open if not used.

NFB (Pin 8/Pin 10): The negative voltage feedback pin is used for sensing a negative output voltage. The pin is connected to the inverting input of the negative feedback amplifier through a 100k source resistor. The negative feedback amplifier provides a gain of –0.5 to the feedback amplifier; therefore, the nominal regulation point is –2.5V on NFB. This pin should be left open if not used.

GND (Pin 9/Pins 1, 8, 9, 16): Signal Ground. The internal error amplifier, negative feedback amplifier, oscillator, slew control circuitry and the bandgap reference are referred to this ground. Keep the connection to the feedback divider and V_C compensation network free of large ground currents.

V_C (Pin 10/Pin 11): The compensation pin is used for frequency compensation and current limiting. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

$\overline{SHDN}$ (Pin 11/Pin 12): The shutdown pin is used for disabling the switcher. Grounding this pin will disable all internal circuitry. Normally this output can be tied high (to V_{IN}) or may be left floating.

R_{CSL} (Pin 12/Pin 13): A resistor to ground sets the current slew rate for the power switch. The minimum resistor value is 3.9k and the maximum value is 68k. Current slew will be approximately:

$$I_{SLEW(A/\mu s)} = 33/R_{CSL(k\Omega)}$$

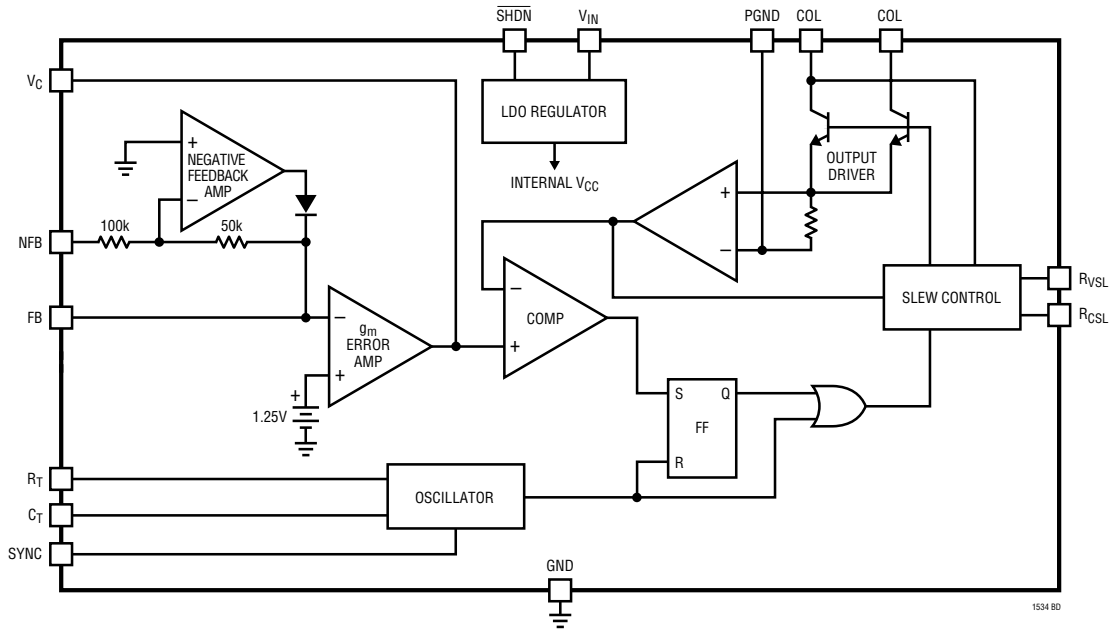
R_{VSL} (Pin 13/Pin 14): A resistor to ground sets the voltage slew rate for the power switch collector. The minimum resistor value is 3.9k and the maximum value is 68k. Voltage slew will be approximately:

$$V_{SLEW(V/\mu s)} = 220/R_{VSL(k\Omega)}$$

V_{IN} (Pin 14/Pin 15): Input Supply Pin. Bypass this pin with a ≥ 4.7µF low ESR capacitor. When V_{IN} is below 2.55V the part will go into undervoltage lockout where it will stop output switching and pull the V_C pin low.

PGND (Pin 16/Pin 3): Power Switch Ground. This ground comes from the emitters of the power switches. In normal operation this pin should have approximately 25nH inductance to ground. This can be done by trace inductance (approximately 1") or with wire or a specific inductive component (e.g., small ferrite bead). This inductance ensures stability in the current slew control loop during turn-off. Too much inductance (>50nH) may produce oscillation on the output voltage slew edges.

BLOCK DIAGRAM



OPERATION

In noise sensitive applications, switching regulators tend to be ruled out as a power supply option due to their propensity for generating unwanted noise. When switching supplies are required due to efficiency or input/output voltage constraints, great pains must be taken to work around the noise generated by a typical supply. These steps may include precise synchronization of the power supply oscillator to an external clock, synchronizing the rest of the circuit to the power supply oscillator, or halting power supply switching during noise sensitive operations. The LT1534 greatly simplifies the task of eliminating supply noise by enabling the design of an inherently low noise switching regulator power supply.

The LT1534 is a fixed frequency, current mode switching regulator with unique circuitry to control the voltage and current slew rates of the output switch. Slew control capability provides much greater control over power supply components that can create conducted and radiated electromagnetic interference. The current mode control provides excellent AC and DC line regulation and simplifies loop compensation.

Current Mode Control

A switching cycle begins with an oscillator discharge pulse which resets the RS flip-flop, turning on the output driver (refer to Block Diagram). The switch current is sensed across an internal resistor and the resulting voltage is amplified and compared to the output of the error amplifier (V_C pin). The driver is turned off once the output of the current sense amplifier exceeds the voltage on the V_C pin. Internal slope compensation is provided to ensure stability under high duty cycle conditions.

Output regulation is obtained using the error amp to set the switch current trip point. The error amp is a transconductance amplifier that integrates the difference between the feedback output voltage and an internal 1.25V reference. The output of the error amp adjusts the switch current trip point to provide the required load current at the desired regulated output voltage. This method of controlling current rather than voltage provides faster input transient response, cycle by cycle current limiting for better output switch protection and greater ease in compensating the feedback loop.

The V_C pin serves three different purposes. It is used for loop compensation, current limit adjustment and soft starting. During normal operation the V_C voltage will be between 0.2V and 1.33V. An external clamp may be used for lowering the current limit. A capacitor coupled to an external clamp can be used for soft starting.

OPERATION

The negative feedback amplifier allows for direct regulation of negative output voltages. The voltage on the NFB pin gets amplified by a gain of –0.5 and driven onto the FB input, i.e., the NFB pin regulates to –2.5V while the amplifier output internally drives the FB pin to 1.25V as in normal operation. The negative feedback amplifier input impedance is 100k (typ) referred to ground.

Slew Control

Control of output voltage and current slew rates is done via two feedback loops. One loop controls the output switch collector voltage dV/dt and the other loop controls the emitter current dI/dt. Output slew control is achieved by comparing the currents generated by these two slewing events to currents created by external resistors R_{VSL} and R_{CSL}. The two control loops are combined internally to provide a smooth transition from current slew control to voltage slew control.

Internal Regulator

Most of the control circuitry operates from an internal 2.4V low dropout regulator that is powered from V_{IN}. The internal low dropout design allows V_{IN} to vary from 2.7V to 23V with virtually no change in device performance. When the part is put into shutdown, the internal regulator is turned off, leaving only a small (12μA typ) current drain from V_{IN}.

Protection Features

There are three modes of protection in the LT1534. The first is overcurrent limit. This is achieved via the clamping action of the V_C pin. The second is thermal shutdown that disables both output drivers and pulls the V_C pin low in the event of excessive chip temperature. The third is undervoltage lockout that also disables both outputs and pulls the V_C pin low whenever V_{IN} drops below 2.5V.

APPLICATIONS INFORMATION

Reducing EMI from switching power supplies has traditionally invoked fear in designers. Many switchers are designed solely on efficiency and as such produce waveforms filled with high frequency harmonics that then propagate through the rest of the power supply.

The LT1534 provides control over two of the more important variables for controlling EMI with switching inductive loads: switch voltage slew rate and switch current slew rate. The use of this part will reduce noise and EMI over conventional switch mode controllers. Because these variables are under control, a supply built with this part will exhibit far less tendency to create EMI and less chance of wandering into problems during production.

It is beyond the scope of this data sheet to get into EMI fundamentals. AN70 contains much information concerning noise in switching regulators and should be consulted.

Oscillator Frequency

The oscillator determines the switching frequency and therefore the fundamental positioning of all harmonics. The use of good quality external components is important to ensure oscillator frequency stability. The oscillator is a sawtooth design. A current defined by external resistor R_T is used to charge and discharge the capacitor C_T. The discharge rate is approximately ten times the charge rate.

By allowing the user to have control over both components, trimming of oscillator frequency can be more easily achieved.

The external capacitance C_T is chosen by:

$$C_{T(nF)} = 2180/[f_{OSC(kHz)} \bullet R_{T(k\Omega)}]$$

where f_{OSC} is the desired oscillator frequency in kHz.

For R_T equal to 16.9k, this simplifies to:

$$C_{T(nF)} = 129/f_{OSC(kHz)}$$

(e.g., C_T = 1.29nF for f_{OSC} = 100kHz)

A good quality temperature stable capacitor should be chosen.

Nominally R_T should be 16.9k. Since it sets up current, its temperature coefficient should be selected to compliment the capacitor. Ideally, both should have low temperature coefficients.

APPLICATIONS INFORMATION

If the FB pin is below 0.4V the oscillator discharge time will increase, causing the oscillation frequency to decrease by approximately 6:1. This feature helps minimize power dissipation during start-up and short-circuit conditions.

Oscillator frequency is important for noise reduction in two ways: 1) the lower the oscillator frequency the lower the harmonics of waveforms are, making it easier to filter them, 2) the oscillator will control the placement of output frequency harmonics which can aid in specific problems where you might be trying to avoid a certain frequency bandwidth that is used for detection elsewhere.

Oscillator Sync

If a more precise frequency is desired (e.g., to accurately place harmonics) the oscillator can be synchronized to an external clock. Set the RC timing components for an oscillator frequency 10% lower than the desired sync frequency.

Drive the SYNC pin with a square wave (with greater than 1.4V amplitude). The rising edge of the sync square wave will initiate clock discharge. The sync pulse should have a minimum of 0.5µs pulse width.

Be careful in synchronizing to frequencies much different from the part since the internal oscillator charge slope determines slope compensation. It would be possible to get into subharmonic oscillation if the sync doesn't allow for the charge cycle of the capacitor to initiate slope compensation. In general, this will not be a problem until the sync frequency is greater than 1.5 times the oscillator free-run frequency.

Slew Rate Setting

Setting the voltage and current slew rates is easy. External resistors to ground on the R_{VSL} and R_{CSL} pins determine the slew rates. Determining what slew rate to use is more difficult. There are several ways to approach the problem.

First start by putting a 50k resistor pot with a 3.9k series resistance on each pin. In general, the next step will be to monitor the noise that you are concerned with. Be careful in measurement technique (consult AN70). Keep probe ground leads very short.

Usually it will be desirable to keep the voltage and current slew resistors approximately the same. There are circumstances where a better optimization can be found by adjusting each separately, but as these values are separated further, a loss of independence of control will occur.

Starting from the lowest resistor setting adjust the pots until the noise level meets your guidelines. Note that slower slewing waveforms will dissipate more power so that efficiency will drop. You can also monitor this as you make your slew adjustment.

It is possible to use a single slew setting resistor. In this case the R_{VSL} and R_{CSL} pins are tied together. A resistor with a value of 2k to 34k (one half the individual resistors) can then be tied from these pins to ground.

Emitter Inductance

A small inductance in the power ground minimizes a potential dip in the output current falling edge that can occur under fast slewing, 25nH is usually sufficient. Greater than 50nH may produce unwanted oscillations in the voltage output. The inductance can be created by wire or board trace with the equivalent of one inch of straight length. A spiral board trace will require less length.

Positive Output Voltage Setting

Sensing of a positive output voltage is usually done using a resistor divider from the output to the FB pin. The positive input to the error amp is connected internally to a 1.25V bandgap reference. The FB pin will regulate to this voltage.

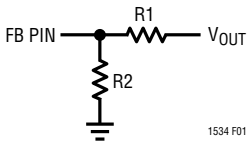


Figure 2

Referring to Figure 2, R1 is determined by:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1\right)$$

The FB bias current represents a small error and can usually be ignored for values of R1||R2 up to 10k.

APPLICATIONS INFORMATION

One word of caution. Sometimes a feedback zero is added to the control loop by placing a capacitor across R1 above. If the feedback zero capacitively pulls the FB pin above the internal regulator voltage (2.4V typ), output regulation may be disrupted. A series resistance with the feedback pin can eliminate this potential problem.

Negative Output Voltage Setting

Negative output voltage can be sensed using the NFB pin. In this case regulation will occur when the NFB pin is at –2.5V. The input bias current for the NFB pin is –25µA (I_{NFB}) and must be accounted for when selecting divider resistor values.

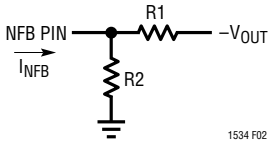


Figure 3

Referring to Figure 3, R1 is chosen such that:

$$R1 = R2 \bullet \frac{\left|V_{OUT}\right| - 2.5}{2.5 + R2 \bullet 25\mu A}$$

A suggested value for R2 is 2.5k. The NFB pin is normally left open if the FB pin is being used.

Dual Polarity Output Voltage Sensing

Certain applications may benefit from sensing both positive and negative output voltages. When doing this each output voltage resistor divider is individually set as previously described. When both FB and NFB pins are used, the LT1534 will act to prevent either output from going beyond its set output voltage. The highest output (lightest load) will dominate control of the regulator. This technique would prevent either output from going unregulated high at no load. However, this technique will also compromise output load regulation.

Shutdown

If the shutdown pin is pulled low, the regulator will turn off. The supply current will be reduced to less than 20µA.

Thermal Considerations

Computing power dissipation for this IC requires careful attention to detail. Reduced output slewing causes the part to dissipate more power than would occur with fast edges. However, much improvement in noise can be produced with modest decrease in supply efficiency.

Power dissipation is a function of topology, input voltage, switch current and slew rates. It is impractical to come up with an all-encompassing formula. It is therefore recommended that package temperature be measured in each application. The part has an internal thermal shutdown to prevent device destruction, but this should not replace careful thermal design.

1. Dissipation due to input current:

$$P_{VIN} = V_{IN}\left(11mA + \frac{I}{60}\right)$$

where I is the average switch current.

2. Dissipation due to the driver saturation:

$P_{VSAT} = (V_{SAT})(I)(DC_{MAX})$

where V_{SAT} is the output saturation voltage which is approximately 0.1 + (0.2)(I), DC_{MAX} is the maximum duty cycle.

3. Dissipation due to output slew using approximations for slew rates:

$$P_{SLEW} = \left(\frac{(V_{IN})\left(I^2 + \frac{\Delta I^2}{4}\right)}{(33)(10^9)}(R_{CSL}) + \frac{(I)\left(V_{IN}^2 - \frac{V_{SAT}^2}{4}\right)}{(220)(10^9)}(R_{VSL})\right)(f_{OSC})$$

Note if V_{SAT} and ΔI are small with respect to V_{IN} and I, then:

$$P_{SLEW} = \left(\frac{(I)(R_{CSL})}{(33)(10^9)} + \frac{(V_{IN})(R_{VSL})}{(220)(10^9)}\right)(f_{OSC})(V_{IN})(I)$$

APPLICATIONS INFORMATION

where ΔI is the ripple current in the switch, R_{CSL} and R_{VSL} are the slew resistors and f_{OSC} is the oscillator frequency.

Power dissipation P_D is the sum of these three terms. Die junction temperature is then computed as:

$$T_J = T_{AMB} + (P_D)(\theta_{JA})$$

where T_{AMB} is ambient temperature and θ_{JA} is the package thermal resistance. For the 16-pin SO with fused leads the θ_{JA} is 50°C/W.

For example, with f_{OSC} = 40kHz, 0.4A average current and 0.1A of ripple, the maximum duty cycle is 88%. Assume slew resistors are both 17k and V_{SAT} is 0.26V, then:

$$P_D = 0.176W + 0.094W + 0.158W = 0.429W$$

In an S16 fused lead package the die junction temperature would be 21°C above ambient.

Frequency Compensation

Loop frequency compensation is accomplished by way of a series RC network on the output of the error amplifier (V_C pin). Referring to Figure 4, the main pole is formed by capacitor C_{VC} and the output impedance of the error amplifier (approximately 400kΩ). The series resistor R_{VC} creates a "zero" which improves loop stability and transient response. A second capacitor C_{VC2}, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_{CPIN\ RIPPLE} = \frac{(1.25)(V_{RIPPLE})(g_m)(R_{VC})}{V_{OUT}}$$

where V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance
R_{VC} = Series resistor on V_C pin
V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below 50mV_{P-P}. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047μF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_{VC} will also reduce V_C pin ripple, but loop phase margin may be inadequate.

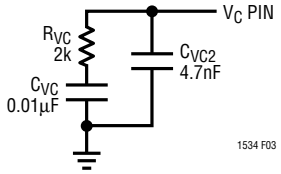


Figure 4

Capacitors

While the IC reduces the source of switcher noise, it is essential for the lowest noise, that the filter capacitors should have low parasitic impedance. Sanyo OS-CON, Panasonic Specialty Polymer and tantalum capacitors are the preferred types. Aluminum electrolytics are not suitable for this application. In general, ESR is more critical than capacitance. At higher frequencies, ESL can also be important. Paralleling capacitors can reduce both ESR and ESL.

Design Note 95 offers more information about capacitor selection. The following is a brief summary:

Solid tantalum capacitors have small size and low impedance. Typically they are available for voltages below 50V. They may have a problem with surge currents (AVX TPS line addresses this issue).

OS-CON capacitors have very low impedance but are only available for 25V or less. Form factor may be a problem. Sometimes their very low ESR can cause loop stability problems.

Ceramic capacitors are generally used for high frequency and high voltage bypass. They too can have such a low ESR as to cause loop stability problems. Often they can resonate with their ESL before ESR becomes effective.

Specialty Polymer Aluminum: Panasonic has come out with their series CD capacitors. While they are only available for voltages below 16V, they have very low ESR and good surge capability.

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Input Capacitor

The ESR of this capacitor acts with high frequency current components to produce much of the conducted noise of the switcher. Values of 1μF to 47μF are typical with ESR less than 0.3Ω. Place the capacitor close to the IC and inductor.

The input capacitor can see a high surge current when a battery of high capacitance source is connected "live." Some solid tantalum capacitors can fail under this condition. Several manufacturers have developed a line of solid tantalum capacitors specially tested for surge capability (e.g., AVX TPS series). However, even these units may fail if the input voltage approaches the maximum voltage rating of the capacitor. AVX recommends derating capacitor voltage by 2:1 for high surge applications.

Output Filter Capacitor

Output capacitors are usually chosen on the basis of ESR since this will determine output ripple. However, low ESR is also needed for low output noise and this will typically be the tougher requirement. Typically required ESR will be less than 0.2Ω . Typical capacitance values are in the 47μF to 500μF range. Again keep connection length as short as possible. Table 1 shows some typical surface mount capacitors.

Table 1

SIZE	CAPACITOR	ESR (MAX Ω)
E CASE	AVX TPS, Sprague 593D	0.1 to 0.3
	AVX TAJ	0.7 to 0.9
D CASE	AVX TPS, Sprague 593D	0.1 to 0.3
	AVX TAJ	0.9 to 2.0
	Panasonic CD	0.05 to 0.18
C CASE	AVX TPS	0.2 (Typ)
	AVX TAJ	1.8 to 3.0
B CASE	AVX TAJ	2.5 to 10

Fast Voltage Slew Edges

A very fast voltage slew under certain operating conditions may produce ringing on the COL voltage waveform. While there is small harmonic energy in this, it can be eliminated by placing an RC network of 10Ω in series with 1000pF from the COL pin to ground.

Switching Diodes

In general, switching diodes should be Schottky diodes such as 1N5817-19 or MBR320-330.

Choosing the Inductor

For a boost converter, inductor selection involves trade-offs of size, maximum output power, transient response and filtering characteristics. Higher inductor values provide more output power and lower input ripple. However, they are physically larger and can impede transient response. Low inductor values have high magnetizing current, which can reduce maximum power and increase input current ripple.

The following procedure can be used to handle these trade-offs:

1. Assume that the average inductor current for a boost converter is equal to load current times V_{OUT}/V_{IN} and decide whether the inductor must withstand continuous overload conditions. If average inductor current at maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Also be aware that boost converters are not short-circuit protected, and under output short conditions, only the available current of the input supply limits inductor current.

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2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core material falls in between. The following formula assumes continuous mode operation but it errors only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT}\left(\frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}\left(V_{OUT} - V_{IN}\right)}{2 \bullet L \bullet f \bullet V_{OUT}}\right)$$

L = inductance value
V_{IN} = supply voltage
V_{OUT} = output voltage
I = output current
f = oscillator frequency

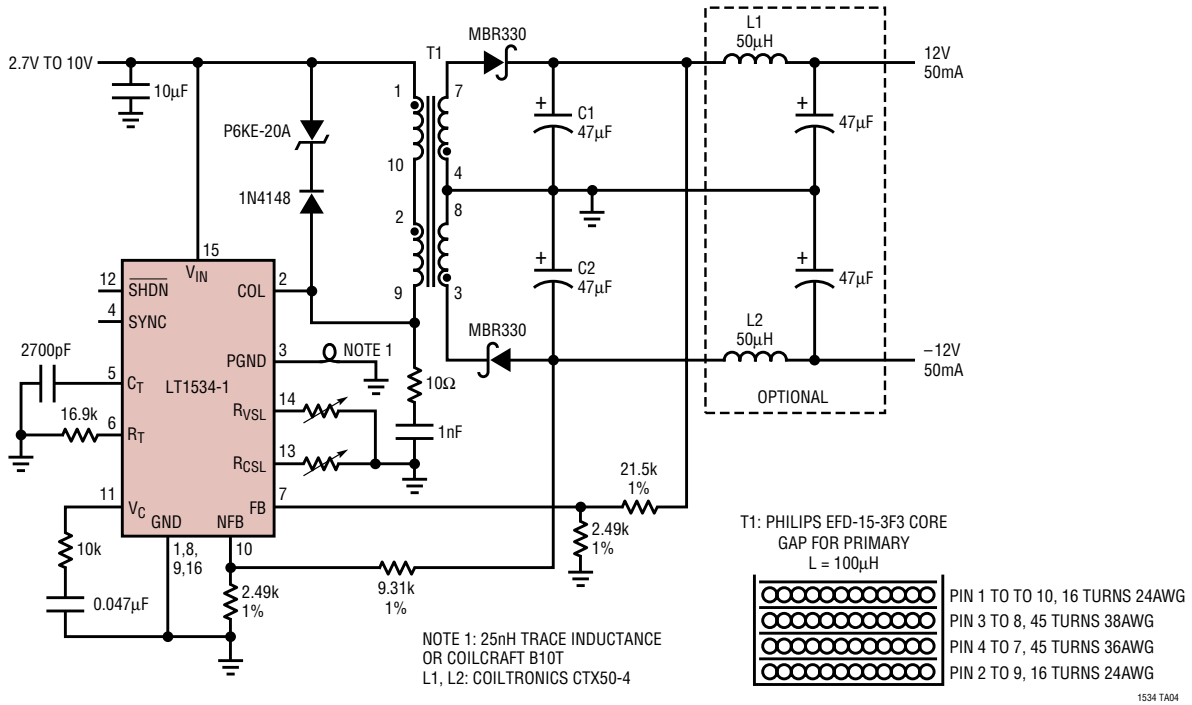
3. Choose a core geometry. For low EMI problems a closed structure should be used such as a pot core, ER core, E core or toroid (see AN70 appendix I).
4. Select an inductor that can handle peak current, average current (heating effects) and fault current.
5. Finally, double check output voltage ripple. The experts in the Linear Technology Applications department have experience with a wide range of inductor types and can assist you in making a good choice.

Further Help

AN70 has more information on noise in switching regulators and its measurement. AN19 has general information on switcher design. The Linear Technology applications group is always ready to lend a helping hand.

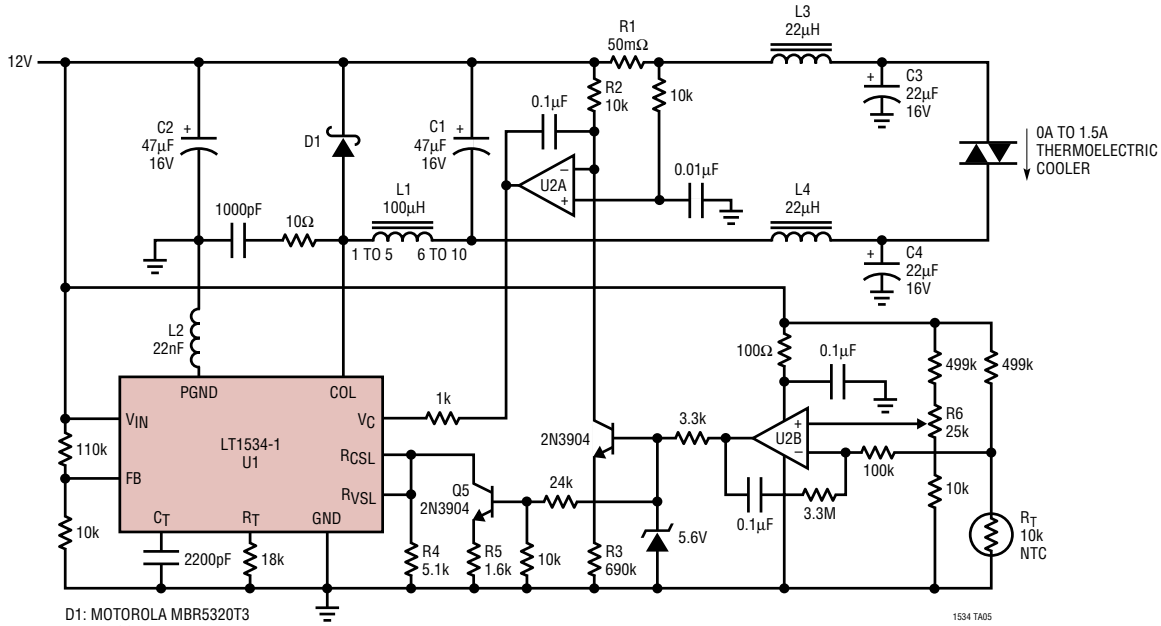
TYPICAL APPLICATIONS

Low Noise ±12V Dual Output Flyback Converter with Dual Polarity Output Voltage Sensing



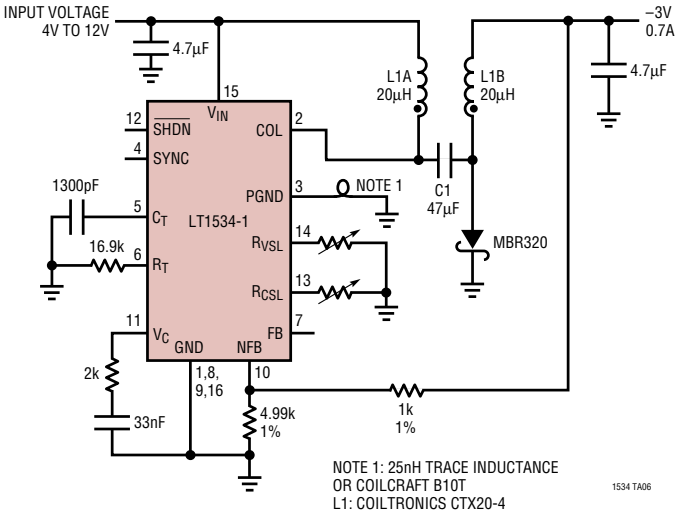
TYPICAL APPLICATIONS

Ultralow Noise Regulator for a Thermo-Electric Cooler, Maintaining Sensitive Electronics at Low Temperatures



D1: MOTOROLA MBR5320T3
L1: MIDCOM 38440
L2: COILCRAFT B07T
L3, L4: SUMIDA CD43-220
U2A, U2B: LT1490

Ultralow Noise 5V to –3V Cuk Converter

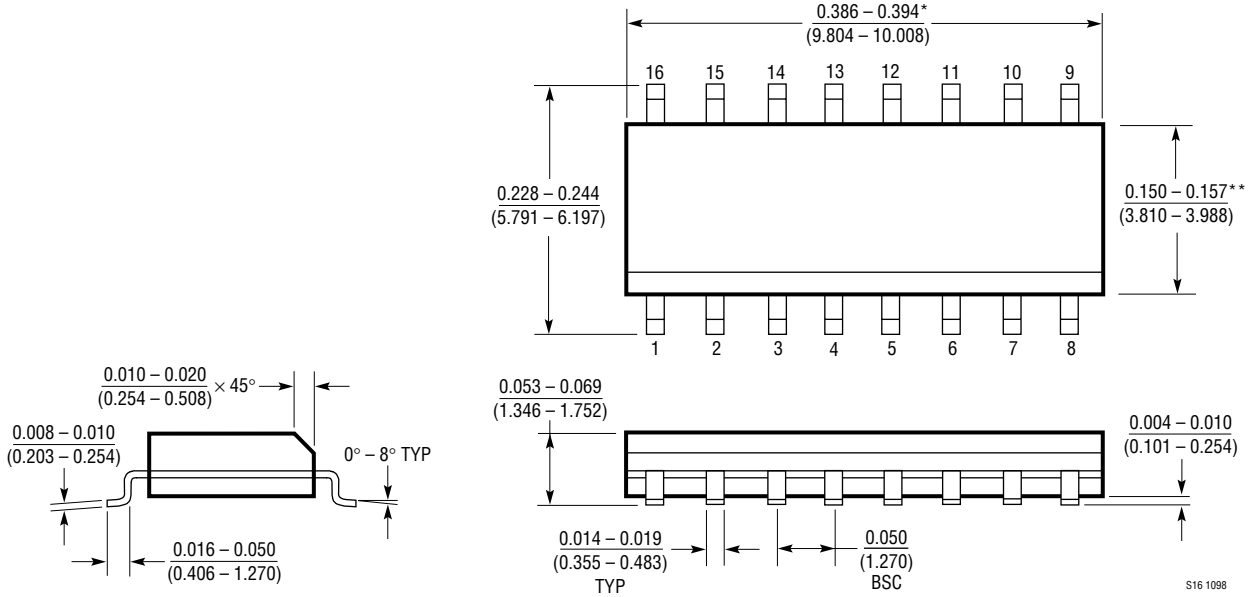


A Cuk converter is a natural topology for a low noise converter. The Cuk converter is a dual of a buck boost converter. C1 is the primary means of storing and transferring energy. Like a buck boost, the DC transfer function is approximately V_{OUT}/V_{IN} = DC/(1 – DC). The output voltage, though negative, can be higher or lower in magnitude from the input. The two inductors can be separate however, by placing them on the same winding input and output current ripple can be greatly reduced. The additional slew control provided by the LT1534 will reduce the high frequency content even further.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

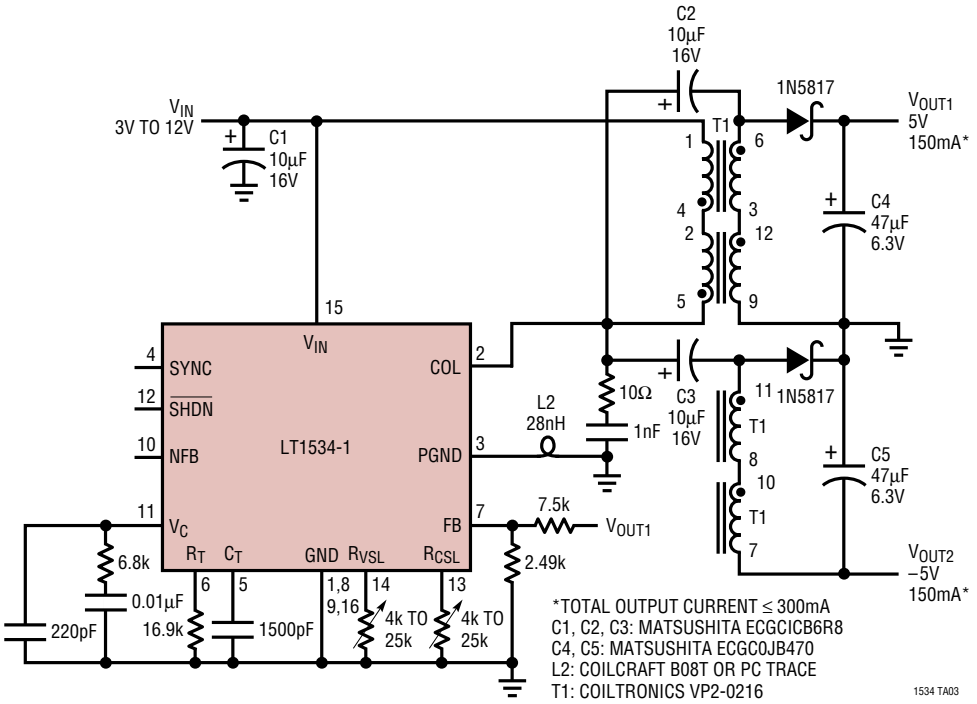


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Low Noise Wide Input Range ±5V Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA Micropower Low Dropout Regulator	0.4V Dropout Voltage, Reverse Battery Protection
LT1175	500mA Negative Low Dropout Micropower Regulator	Positive or Negative Shutdown Logic
LT1370	500kHz High Efficiency 6A Switching Regulator	90% Efficiency, Constant Frequency, High Power
LT1371	500kHz High Efficiency 3A Switching Regulator	90% Efficiency, Constant Frequency, Synchronizable
LT1377	1MHz High Efficiency 1.5A Switching Regulator	High Frequency, Small Inductor
LT1425	Isolated Flyback Switching Regulator	Excellent Regulation Without Transformer “Third Winding”
LT1533	Ultralow Noise 1A Switching Regulator	Push-Pull Design for Low Noise Isolated Supplies
LT1763	500mA Low Noise Micropower LDO	20µV_{RMS}(10Hz to 100kHz), 30µA Quiescent Current
LT1777	700mA Low Noise Step-Down Switching Regulator	Programmable dI/dt Limit, 48VMax V_{IN}

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