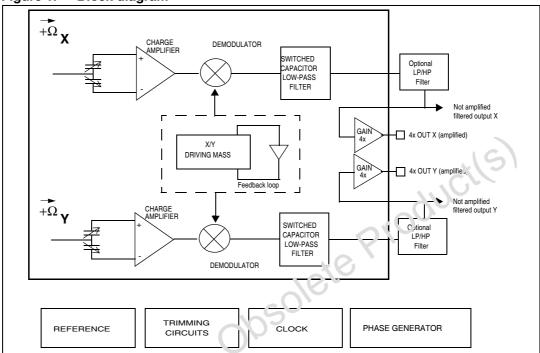
Contents

1	Bloc	Block diagram and pin description					
	1.1	Pin description 3					
2	Mec	hanical and electrical specifications					
	2.1	Mechanical characteristics					
	2.2	Electrical characteristics					
	2.3	Absolute maximum ratings					
3	Term	ninology					
	3.1	Sensitivity 7 Zero-rate level 7					
	3.2	Zero-rate level					
	3.3	Self-test					
	3.4	Self-test 7 High pass filter reset (HP) 7					
4	Арр	lication hints 8					
	4.1	Output response vs. rotation					
	4.2	Soldering information					
5	Pack	kage information10					
6	Povi	eion history 11					

Block diagram and pin description 1

Figure 1. **Block diagram**



Pin description 1.1

Figure 2. Pin connection

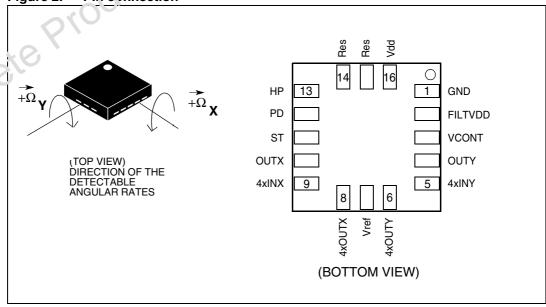


Table 2. Pin description

Pin # Pin name Analog function 1 GND OV supply voltage 2 FILTVDD PLL filter connection pin #2 3 VCONT PLL filter connection pin #1 4 OUTY Not amplified output 5 4xINY Input of 4x amplifier 6 4xOUTY Y rate signal output voltage (amplified) 7 Vref Reference voltage 8 4xOUTX X rate signal output voltage (amplified) 9 4xINX Input of 4x amplifier 10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode; logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter reset (logic 0: normal operation mode; logic1: existence in pink pass filter is reset) 14,15 Res Free size O. Connect to Vdd 16 Vdd Fower supply	Table 2.	Fill description	
2 FILTVDD PLL filter connection pin #2 3 VCONT PLL filter connection pin #1 4 OUTY Not amplified output 5 4xINY Input of 4x amplifier 6 4xOUTY Y rate signal output voltage (amplified) 7 Vref Reference voltage 8 4xOUTX X rate signal output voltage (amplified) 9 4xINX Input of 4x amplifier 10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode, logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter reset (logic 0: normal operation mode; logic1: extense high pass filter is reset) 14,15 Res Teserved. Connect to Vdd	Pin #	Pin name	Analog function
3	1	GND	0V supply voltage
4 OUTY Not amplified output 5 4xINY Input of 4x amplifier 6 4xOUTY Y rate signal output voltage (amplified) 7 Vref Reference voltage 8 4xOUTX X rate signal output voltage (amplified) 9 4xINX Input of 4x amplifier 10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode; logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter reset (logic 0: normal operation mode; logic1: extense, high pass filter is reset) 14,15 Res Self-text (Connect to Vdd	2	FILTVDD	PLL filter connection pin #2
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4xOUTY Y rate signal output voltage (amplified) 7	4	OUTY	Not amplified output
7 Vref Reference voltage 8 4xOUTX X rate signal output voltage (amplified) 9 4xINX Input of 4x amplifier 10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode, logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter recet (logic 0: normal operation mode; logic1: extense high pass filter is reset) 14,15 Res Secret d. Connect to Vdd	5	4xINY	Input of 4x amplifier
8 4xOUTX X rate signal output voltage (amplified) 9 4xINX Input of 4x amplifier 10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode, logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter recet (logic 0: normal operation mode; logic1: extense high pass filter is reset) 14,15 Res Tiederved. Connect to Vdd	6	4xOUTY	Y rate signal output voltage (amplified)
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10 OUTX Not amplified output 11 ST Self-test (logic 0: normal mode, logic 1: self-test) 12 PD Power-down (logic 0: normal mode; logic 1: power-down mode) 13 HP High pass filter recet (logic 0: normal operation mode; logic1: external high pass filter is reset) 14,15 Res Geverus d. Connect to Vdd	8	4xOUTX	X rate signal output voltage (amplified)
11 ST Self-test (logic 0: normal mode, logic 1: self-test) Power-down (logic 0: normal mode; logic 1: power-down mode) High pass filter recet (logic 0: normal operation mode; logic1: extense high pass filter is reset) 14,15 Res Theoryeld. Connect to Vdd	9	4xINX	Input of 4x amplifier
Power-down (logic 0: normal mode; logic 1: power-down mode) High pass filter recet (logic 0: normal operation mode; logic1: external high pass filter is reset) 14,15 Res Theory d. Connect to Vdd	10	OUTX	Not amplified output
mode) High pass filter recet (logic 0: normal operation mode; logic1: externer high pass filter is reset) 14,15 Res Served. Connect to Vdd	11	ST	Self-test (logic 0: normal moc'e, logic 1: self-test)
logic1: externer high pass filter is reset) 14,15 Res Served. Connect to Vdd	12	PD	Power-down (logic 0: norma' mode; logic 1: power-down mode)
	13	HP	
16 Vdd Fower supply	14,15	Res	ภียะ ราv∈d. Connect to Vdd
Product(s)	16	Vdd	Fower supply
	O,	oduci(s)	

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 3 V, T = 25 °C unless otherwise noted⁽¹⁾

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
FSA	Measurement range	4x OUT (amplified)		±100		°/s
FS	weasurement range	OUT (not amplified)		±400		°/s
SoA	Sensitivity ⁽³⁾	4x OUT (amplified)		10		mV/ °/s
So	Sensitivity	OUT (not amplified)		2.5		m\'/ °/s
SoDr	Sensitivity change vs temperature	Delta from 25°C		0.03		%/°C
Voff	Zero-rate level ⁽³⁾			1.23	AU	V
Vref	Reference voltage			1.23	20,	V
OffDr	Zero-rate level change Vs temperature	Delta from 25°C		0. 12	<i>-</i>	°/s/°C
NL	Non linearity	Best fit straight line		±1		% FS
BW	Bandwidth ⁽⁴⁾		0/9	140		Hz
Rn	Rate noise density		15	0.017		°/s / √Hz
Тор	Operating temperature range	,0	-40		+85	°C

^{1.} The product is factory calibrated at 3 V. The op atic nal power supply range is specified in *Table 4*.

577

Doc ID 15811 Rev 2

^{2.} Typical specifications are not guaranteed

^{3.} Sensitivity and zero-rate level are not ratio netric to supply voltage

^{4.} The product is capable of measuring angular rates extending from DC to the selected BW.

2.2 **Electrical characteristics**

Electrical characteristics @ Vdd =3 V, T=25 °C unless otherwise noted(1) Table 4.

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit	
Vdd	Supply voltage		2.7	3	3.6	V	
ldd	Supply current	PD pin connected to GND		6.8		mA	
IddPdn	Supply current in power-down mode	PD pin connected to Vdd		1	5	μΑ	
Vst	Colf toot input	Logic 0 level	0		0.2*Vdd	V	
VSI	Self-test input	Logic 1 level	0.8*Vdd		Vdd		
VPD	Power-down input	Logic 0 level	0		0.2*\'לוני	9	
VPD	Power-down input	Logic 1 level	0.8*Vdd	_	/ˈdr.	V	
Тор	Operating temperature range		-40	010C	+85	°C	
The product is factory calibrated at 3 V							
2. Typical specifications are not guaranteed							
 The product is factory calibrated at 3 V Typical specifications are not guaranteed Absolute maximum ratings 							

^{1.} The product is factory calibrated at 3 V

Absolute maximum ratings 2.3

Stresses above those listed as "Abso ute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

	Symbol	Ratings	Maximum value	Unit
	Vdd	Supply voltage	-0.3 to 6	V
	√in	Input voltage on any control pin (PD, ST)	-0.3 to Vdd +0.3	V
	T _{STG}	Storage temperature range	-40 to +125	°C
Opso	А	Acceleration	3000 g for 0.5 ms	
		Acceleration	10000 g for 0.1 ms	
	ESD	Electrostatic discharge protection	2 (HBM)	kV



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part



This is an ESD sensitive device, improper handling can cause permanent damage to the part

57 Doc ID 15811 Rev 2 6/12

^{2.} Typical specifications are not guaranteed

LPR510AL Terminology

3 Terminology

3.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going output voltage for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

3.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

3.3 Self-test

Self-test allows testing of the mechanical and electrical part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. The self-test function is off when the ST pin is connected to GND. When the ST pin is tied to Vdd, an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output will exhibit a voltage change in its DC level which is also dependent on the supply voltage. When ST is active, the device output level is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the mechanical element is working properly and the parameters of the interface chip are within the defined specifications.

3.4 Yoh pass filter reset (HP)

The LPR510AL provides the possibility to reset the optional external high pass filter by applying a high logic value to the HP pad. This procedure ensures faster response, especially during overload conditions. Moreover, this operation is suggested each time the device is powered.

Application hints LPR510AL

Application hints 4

C2 10nF GND GND Vdd 10kOhm 470nF (TOP VIEW) DIRECTION OF THE DETECTABLE ANGULAR RATES R1 100 nF 10 uF C1 116| | | | 114| GND <u>13</u> J ∟ J L JNot amplified LPR510AL Not amplified 51 filtered output X filtered output Y (Top View) ú 5 1611 118 R1 GND Vref Vref GÑD Recomended Optional Vref Low-pass filter High-pass filter Typical values: R1 = 1MOhm C1 = 4.7 uF R2 = 33kOhm $C2 = 2.2 \text{ nF to } 2.2 \text{ } \mu\text{F}$

Figure 3. LPR510AL electrical connections and external components values

Power supply decoupling capacitors (100 nF ceramic or polyester + 10 µF aluminum) should be placed as near as possible to the device (common design practice).

The LFn5.0AL allows band limiting of the output rate response through the use of an externa low pass filter (suggested) and/or high pass filter (optional) in addition to the າກາຣedded low pass filter ($f_t = 140 \text{ Hz}$).

AxOUTX and 4xOUTY are respectively OUTX and OUTY amplified outputs lines, internally buffered to ensure low output impedance.

If external high pass or low pass filtering is not applied it is mandatory to short-circuit respectively pad 4 to pad 5 and pad 9 to pad 10 when amplified outputs are used.

When only not-amplified outputs are used (OUTX/Y), it is suggested to set pads 5 and 9 to fixed reference voltage (GND/Vref).

When high pass filter is applied to not amplified output (OUTx), it is recommended to buffer the line before entering ADC for performance optimization.

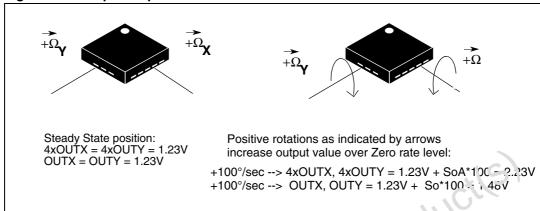
The LPR510AL IC includes a PLL (phase locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be added at the FILTVDD and VCONT pins (as shown in *Figure 3*) to implement a low-pass filter.

577

LPR510AL Application hints

4.1 Output response vs. rotation

Figure 4. Output response vs. rotation



4.2 Soldering information

The LGA package is compliant with the ECOPACK[®], Fight and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave "pin 1 indicator" unconnected during soldering.

Land pattern and soldering recomme rida, ich sare available at www.st.com.

5/

Doc ID 15811 Rev 2

Package information LPR510AL

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

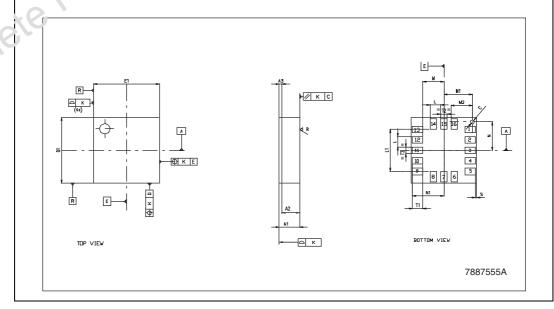
Figure 5. LGA-16: mechanical data and package dimensions

Dimensions						
Ref.	mm			inch		
Kei.	Min.	Тур.	Max.	Min.	Тур.	Max.
A1	1.46	1.5	1.6	0.057	0.059	0.063
A2			1.33			0.052
АЗ	0.16	0.2	0.24	0.006	0.008	0.009
С		0.3			0.012	
D1	4.85	5	5.15	0.191	0.197	0.203
E1	4.85	5	5.15	0.191	0.197	0.203
L		0.8			0.031	
L1		3.2			0.126	
М		1.6			0.062	
M1	2.15	2.175	2.20	0.085	0.086	0.087
M2		1.625			0.064	10
N		2.175			0.086	
N1		2.4			0.094	
T1		0.8			0.031	
T2	0.475	0.5	0.525	(.019	0.020	0.021
R	1.2		1,0	0.047	,	0.063
S		0.1	O.		0.004	
h		บ.15			0.006	
k	a ()	Ū.05			0.002	
K()	1	0.1			0.004	

Outline and mechanical data



LGA-16 (5x5x1.5mm) Land Grid Array Package



10/12 Doc ID 15811 Rev 2

LPR510AL Revision history

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
04-Jun-2009	1	Initial release
06-Jul-2009	2	Small text changes to improve readability. Updated <i>Table 4</i>



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12/12 Doc ID 15811 Rev 2

