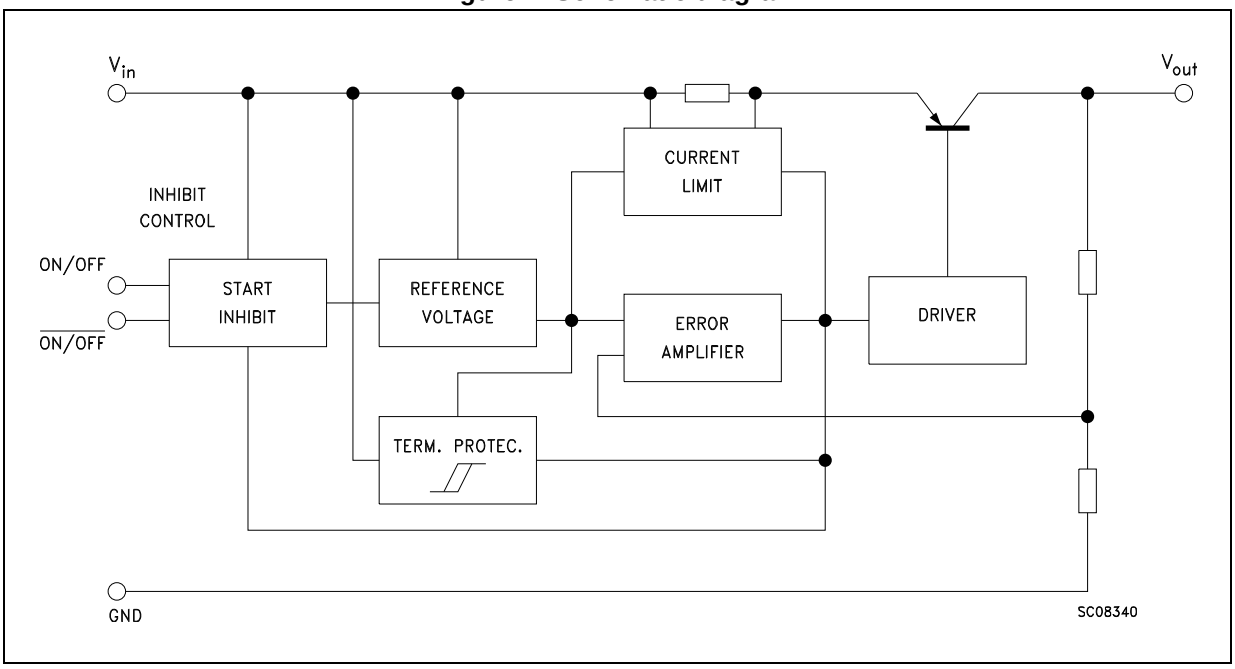
Contents

1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connection (top view)

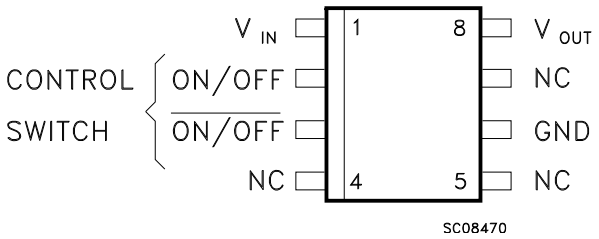


Table 2. Truth table

ON/$\overline{\text{OFF}}$ (pin 2)	$\overline{\text{ON/OFF}}$ (pin 3)	Status
H	L	ON
H	H	OFF
L	L	OFF
L	H	Not allowed

Note: Logic levels are those defined in the electrical characteristics.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	20	V
I_O	Output current	Internally limited	
P_{TOT}	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-40 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

4 Test circuits

Figure 3. Supply current (ON mode)

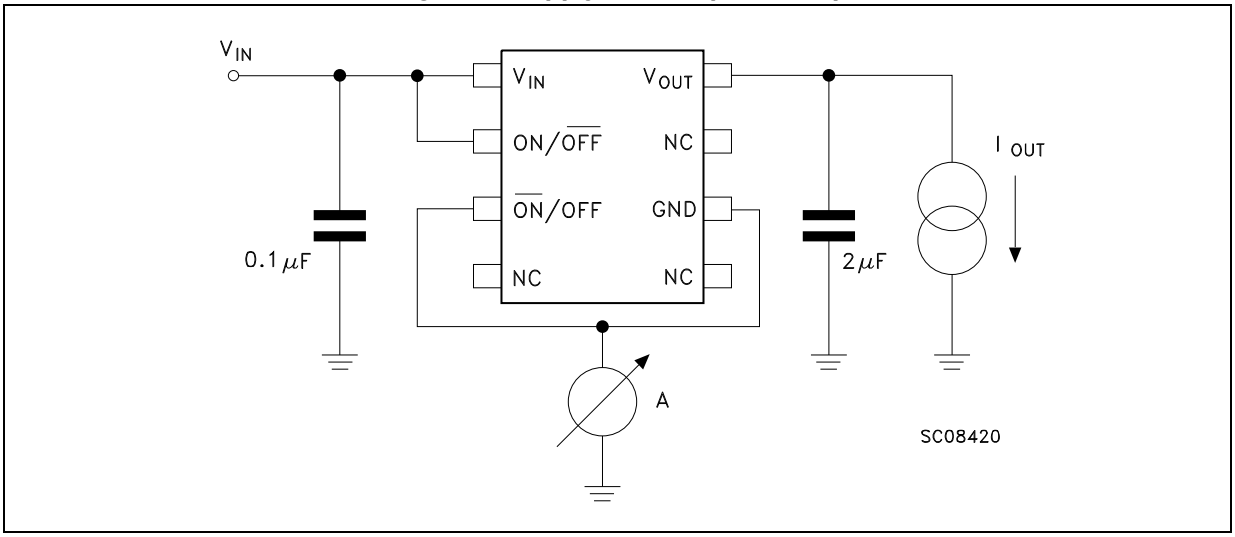
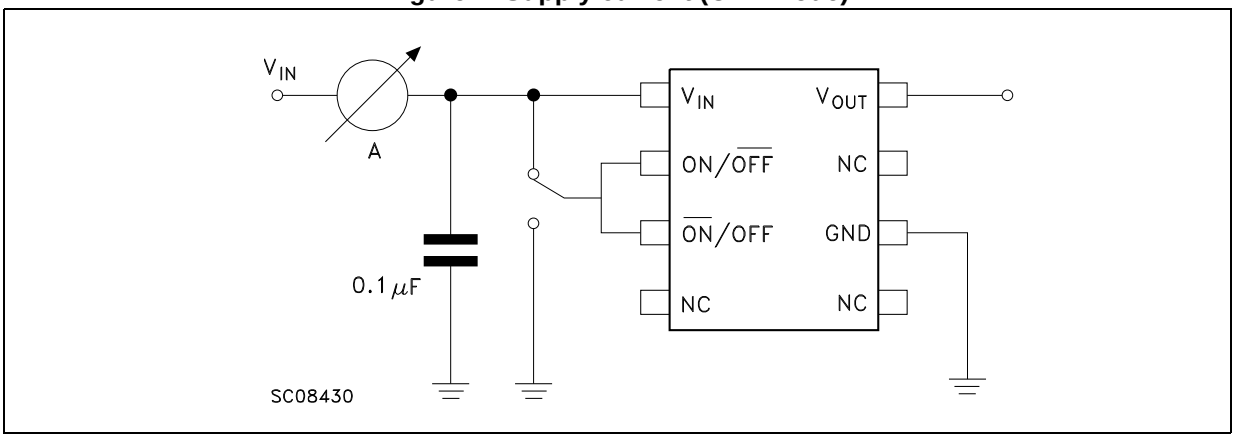


Figure 4. Supply current (OFF mode)



Note: The switch emulates two possibilities to set the regulator in OFF mode.

5 Electrical characteristics

(Refer to test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified)

Table 4. LK115D33 electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 5.3 V		3.2	3.3	3.4	V
		I_O = 10 mA, V_I = 5.3 V, T_a= -40 to 125 °C		3.135		3.465	
V_I	Operating input voltage	I_O = 100 mA				20	V
I_{out}	Output current limit			120	200		mA
ΔV_O	Line regulation	V_I = 4.3 to 20 V, I_O = 0.5 mA			2	10	mV
ΔV_O	Load regulation	V_I = 4.3 V, I_O = 0.5 to 100 mA			4	20	mV
I_d	Quiescent current (ON mode)	V_I = 4.3 to 20 V, I_O = 0			0.28	0.5	mA
		V_I = 4.3 to 20 V, I_O = 100 mA			1.5	3	
	(OFF mode)	V_I = 4.3 to 20 V			0.01	2	µA
SVR	Supply voltage rejection	I_O = 5 mA V_I = 5.3 V ± 1 V	f = 120 Hz		79		dB
			f = 1 kHz		74		
			f = 10 kHz		57		
eN	Output noise voltage (RMS)	B = 10 Hz to 100 kHz			72.6		µV
V_d	Dropout voltage	I_O = 60 mA			0.17		V
V_{HIc}	ON/$\overline{OFF}$ control (pin 2)	Pin 3 to GND, OFF		0		0.5	V
		Pin 3 to GND, ON		2.4		V_{in}	
V_{LIc}	$\overline{ON}$/OFF control (pin 3)	Pin 2 to V_{in}, OFF		V_{in}-0.2		V_{in}	V
		Pin 2 to V_{in}, ON		0		V_{in}-2.4	
C_O	Output bypass capacitance	ESR = 0.5 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

(Refer to test circuits, T_J = 25 °C, C_I = 0.1 µF, C_O = 2.2 µF unless otherwise specified)

Table 5. LK115D50 electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 10 mA, V_I = 7 V		4.85	5	5.15	V
		I_O = 10 mA, V_I = 7 V, T_a= -40 to 125 °C		4.75		5.25	
V_I	Operating input voltage	I_O = 100 mA				20	V
I_{out}	Output current limit			120	200		mA
ΔV_O	Line regulation	V_I = 6 to 20 V, I_O = 0.5 mA			3	15	mV
ΔV_O	Load regulation	V_I = 6 V, I_O = 0.5 to 100 mA			4	20	mV
I_d	Quiescent current (ON mode)	V_I = 6 to 20 V, I_O = 0			0.28	0.5	mA
		V_I = 6 to 20 V, I_O = 100 mA			1.5	3	
	(OFF mode)	V_I = 6 to 20 V			0.01	2	µA
SVR	Supply voltage rejection	I_O = 5 mA V_I = 7 V ± 1 V	f = 120 Hz		75		dB
			f = 1 kHz		70		
			f = 10 kHz		55		
eN	Output noise voltage (RMS)	B = 10 Hz to 100 kHz			110		µV
V_d	Dropout voltage	I_O = 60 mA			0.17		V
V_{HIc}	ON/$\overline{OFF}$ control (pin 2)	Pin 3 to GND, OFF		0		0.5	V
		Pin 3 to GND, ON		2.4		V_{in}	
V_{LIc}	$\overline{ON}$/OFF control (pin 3)	Pin 2 to V_{in}, OFF		V_{in}-0.2		V_{in}	V
		Pin 2 to V_{in}, ON		0		V_{in}-2.4	
C_O	Output bypass capacitance	ESR = 0.5 to 10 Ω, I_O = 0 to 100 mA		2	10		µF

6 Package mechanical data

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Figure 5. SO-8 drawings

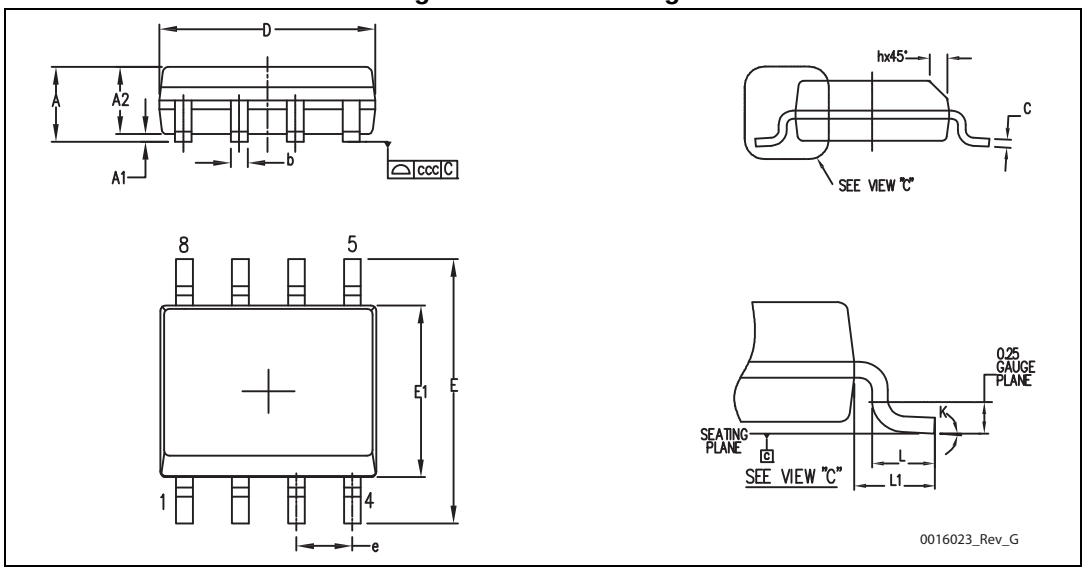

Table 6. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

7 Packaging mechanical data

Figure 6. SO-8 tape and reel dimensions

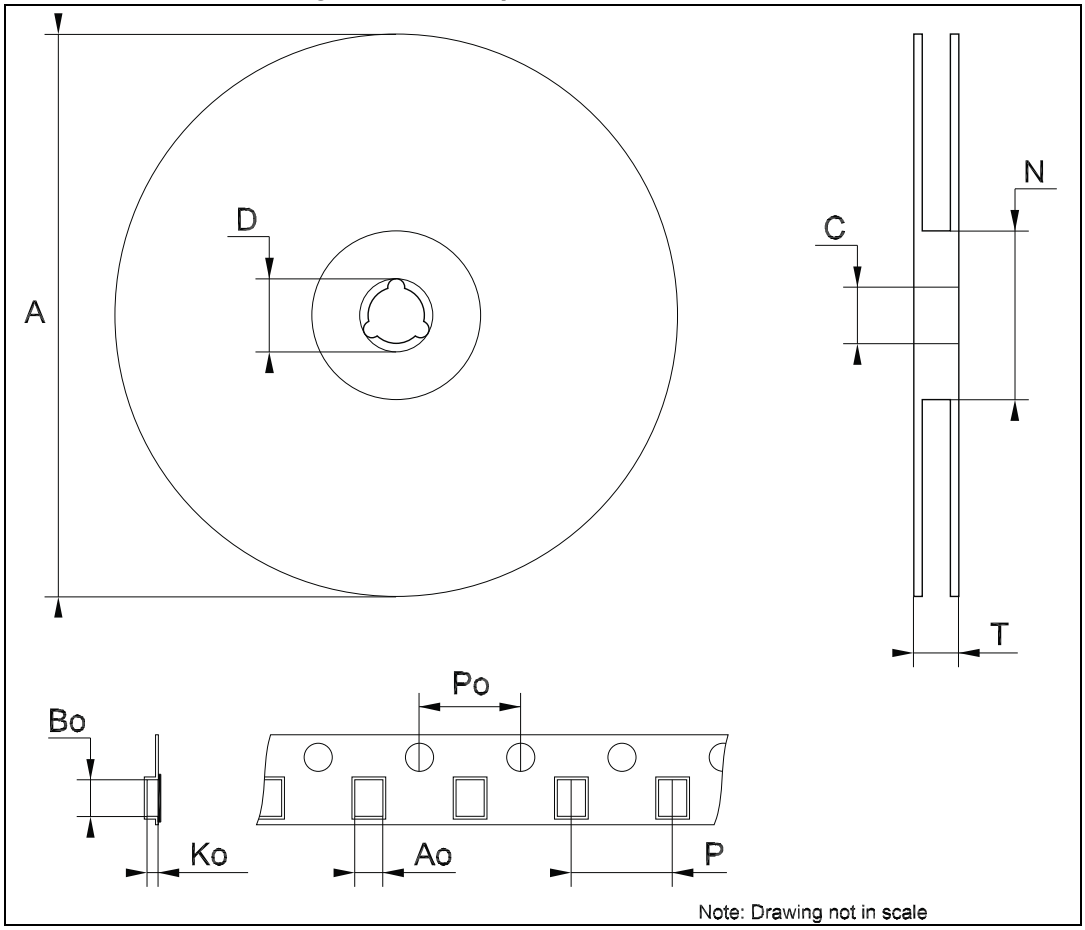

Table 7. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
07-Jun-2006	3	Order codes updated.
07-Jul-2008	4	Added *Table 1 on page 1*.
31-Jan-2014	5	Changed the LK115xx30, LK115xx33, LK115xx50 to LK115. Updated the description in cover page. Updated *Section 5: Electrical characteristics*, *Section 6: Package mechanical data*. Added *Section 7: Packaging mechanical data*. Minor text changes.

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