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PRODUCT DESCRIPTION

The Zarlink family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. Zarlink SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and video telephony applications.

The Zarlink SLIC devices offer support of BORSHT (battery feed, overvoltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, Tip Open, and loop-current detection. These features allow reduction of linecard cost by minimizing component count, conserving board space, and supporting automated manufacturing.

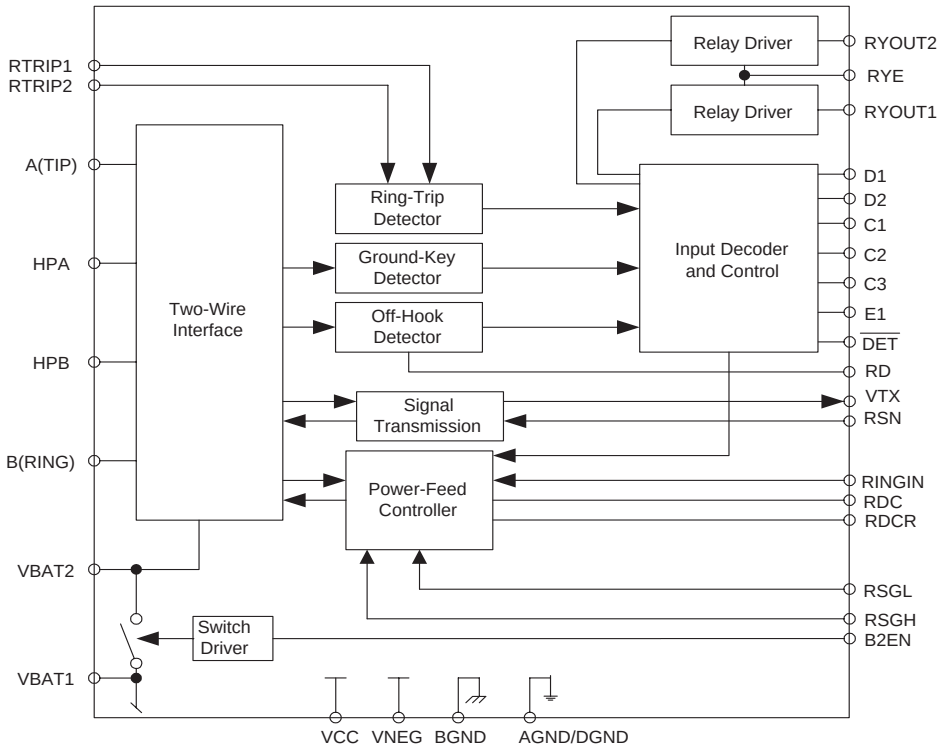
The Zarlink SLIC devices provide the two- to four-wire hybrid function, DC-loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion Zarlink codec/filter, such as the Le58QL0xx Quad SLAC (QLSLAC™) device.

The Le79R79 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications would be ISDN terminal adaptors, fiber-in-the-loop, radio-in-the-loop, hybrid fiber/coax and video telephony (home-side) boxes. The Le79R79 Ringing SLIC can provide sufficient voltage to meet the stringent LSSGR five-ringer equivalent specification. Using a CMOS-compatible input waveform and wave shaping R-C network, the Le79R79 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.

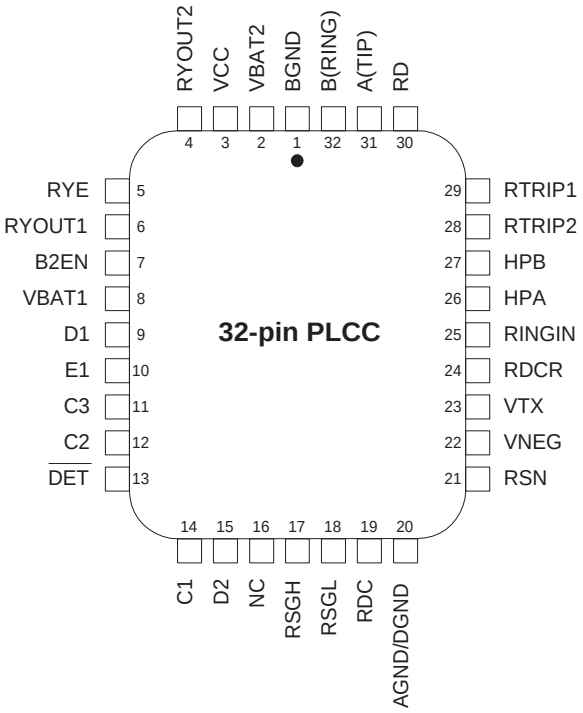
In order to further enhance the suitability of this device in short-loop, distributed switching applications, Zarlink has maximized power savings by incorporating battery switching on chip. The Le79R79 Ringing SLIC device switches between two battery supplies such that in the off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC device automatically switches to a higher voltage in the On-hook (Standby) state.

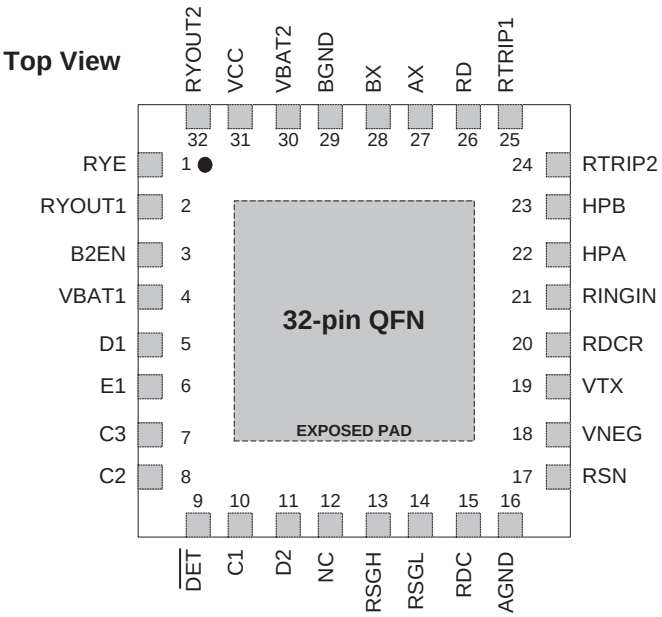
Like all of the Zarlink SLIC devices, the Le79R79 Ringing SLIC device supports on-hook transmission, ring-trip detection, programmable loop-detect threshold, and is available with on-chip polarity reversal. The Le79R79 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. Several performance grades are available to meet both CCITT and LSSGR requirements, including various longitudinal balance options.

Figure 1. Le79R79 Block Diagram



CONNECTION DIAGRAMS





Note:

1. *Pin 1 is marked for orientation.*
2. *NC = No connect.*
3. *The thermally enhanced QFN package features an exposed pad on the underside which must be electrically tied to VBAT1.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Ground	Analog and digital ground
A(TIP)	Output	Output of A(TIP) power amplifier
B2EN	Input	V_{BAT2} Enable. Logic Low enables operation from V_{BAT2}. Logic High enables operation from V_{BAT1}. TTL compatible.
BGND	Ground	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C3–C1	Input	Decoder. SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
D1	Input	Relay1 Control. TTL compatible. Logic Low activates the Relay1 relay driver.
D2	Input	Relay2 Control. (Option) TTL compatible. Logic Low activates the Relay2 relay driver.
$\overline{\text{DET}}$	Output	Hook switch detector. When enabled, a logic Low indicates that the selected detector is tripped. The logic inputs C3–C1 and E1 select the detector. The output is open collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key Enable. (Option) A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-Pass Filter. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter. B(RING) side of high-pass filter capacitor.
NC	—	Not internally connected.
RD	Resistor	Detect Resistor. Detector threshold set and filter pin.
RDC	Output	DC Feed Resistor. Connection point for the DC-feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is negative for normal polarity and positive for reverse polarity.
RDCR	—	Connection point for feedback during ringing.
RINGIN	Input	Ring Signal. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input.
RSGH	Input	Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V_{BAT1}.
RSGL	Input	Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both $V_{BAT1 \text{ and } }V_{BAT2}$.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
RTRIP1	Input	Ring-Trip Detector. Ring-trip detector threshold set and filter pin.
RTRIP2	Input	Ring-Trip Detector. Ring-trip detector threshold offset (switch to V_{BAT1}). For power conservation in any nonringing state, this switch is open.
RYE	Output	Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.
RYOUT1	Output	Relay/Switch Driver. Open collector driver with emitter internally connected to RYE.
RYOUT2	Output	Relay/Switch Driver. (Option) Open collector driver with emitter internally connected to RYE.
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect to off-hook battery through a diode.
VCC	Power	Positive analog power supply
VNEG	Power	Negative analog power supply. This pin is the return for the internal V_{EE} regulator.
VTX	Output	Transmit Audio. This output is a 0.5066 gain version of the A(TIP) and B(RING) metallic AC voltage. VTX also sources the two-wire input impedance programming network.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–55 to +150º C
V_{CC} with respect to AGND/DGND	0.4 to +7 V
V_{NEG} with respect to AGND/DGND	0.4 V to V_{BAT2}
V_{BAT2}	V_{BAT1} to GND
V_{BAT1} with respect to AGND/DGND: Continuous 10 ms	 +0.4 to –80 V +0.4 to –85 V
BGND with respect to AGND/DGND:	+3 to –3 V
A(TIP) or B(RING) to BGND: Continuous 10 ms (F = 0.1 Hz) 1 µs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	 V_{BAT1} –5 to +1 V V_{BAT1} –10 to +5 V V_{BAT1} –15 to +8 V V_{BAT1} –20 to +12 V
Current from A(TIP) or B(RING)	±150 mA
RYOUT1, RYOUT2 current	75 mA
RYOUT1, RYOUT2 voltage	RYE to +7 V
RYOUT1, RYOUT2 transient	RYE to +10 V
RYE voltage	BGND to V_{BAT1}
C3–C1, D2–D1, E1, B2EN, and RINGIN: Input voltage	 –0.4 V to V_{CC} + 0.4 V
Maximum power dissipation, continuous, T_A = 70º C, No heat sink (see note) In 32-pin PLCC package In 32-pin QFN package	 1.67 W 3.00 W
Thermal data: In 32-pin PLCC package In 32-pin QFN package	θ_{JA} 45° C/W 25° C/W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Note:

1. *Thermal limiting circuitry on the chip will shut down the circuit at a junction temperature of about 165ºC. Continuous operation above 145ºC junction temperature may degrade device reliability.*
2. *The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.*

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial
	–40 to +85 °C extended temperature
Ambient Relative Humidity	15 to 85%

Electrical Ranges

V_{CC}	4.75 to 5.25 V
V_{NEG}	–4.75 V to V_{BAT2}
V_{BAT1}	–40.5 to –75 V
V_{BAT2}	–19 V to V_{BAT1}
AGND/DGND	0 V
BGND with respect to AGND/DGND	–100 to +100 mV
Load resistance on VTX to ground	20 kΩ minimum

SPECIFICATIONS

Transmission Performance

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
2-wire return loss	200 Hz to 3.4 kHz (See Figure 6.)	26			dB	1, 4, 6
Z_{VTX}, analog output impedance			3	20	Ω	4
V_{VTX}, analog output offset voltage	0 to +70° C	–35		+35	mV	
	–40 to +85° C	–40		+40		4
Z_{RSN}, analog input impedance			1	20	Ω	
Overload level, 2-wire and 4-wire, Off hook	Active state	2.5			Vpk	2a
Overload level, 2-wire	On hook, R_{LAC} = 600 Ω	0.88			Vrms	2b
THD (Total Harmonic Distortion)	+3 dBm, BAT 2 = –24 V		–64	–50	dB	5
THD, On hook, OHT state	0dBm, R_{LAC} = 600 Ω BAT1 = –75 V			–40		

Longitudinal Performance

(See Figure 8.)

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz	–1, –3*	52			dB	
	normal polarity	–2, –4	63				
	reverse polarity	–2	54				
	normal polarity, –40° C to +85 ° C	–2, –4	58				4
	1 kHz to 3.4 kHz	–1, –3*	52				
	normal polarity	–2, –4	58				
	reverse polarity	–2	54				
	normal polarity, –40° C to +85° C	–2, –4	54				4
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity		42				
Longitudinal current per pin (A or B)	Active or OHT state		12	28		mArms	4
Longitudinal impedance at A or B	0 to 100 Hz, T_A = +25° C			25		Ω/pin	

Idle Channel Noise

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
C-message weighted noise	0 to +70° C		+7	+11	dBrnC	
	–40 to +85° C			+12		4
Phosphometric weighted noise	0 to +70° C		–83	–79	dBmp	
	–40 to +85° C			–78		

Insertion Loss and Four-to-Four-Wire Balance Return Signal

(See Figure 6 and Figure 7.)

Description	Test Conditions (See Note 1)		Min	Typ	Max	Unit	Note
Gain accuracy, 4-to-2-wire	0 dBm, 1 kHz		–0.20	0	+0.20	dB	
Gain accuracy, 2-to-4-wire 4-to-4-wire	0 dBm, 1 kHz		–6.22	–6.02	–5.82		
Gain accuracy, 4-to-2-wire	OHT state, on hook		–0.35	0	+0.35		3
Gain accuracy, 2-to-4-wire 4-to-4-wire	OHT state, on hook		–6.37	–6.02	–5.77		
Gain accuracy over frequency	300 to 3400 Hz	0 to +70° C	–0.10		+0.10		
	relative to 1 kHz	–40 to +85° C	–0.15		+0.15		
Gain tracking	+3 dBm to –55 dBm	0 to +70° C	–0.10		+0.10		
	relative to 0 dBm	–40 to +85° C	–0.15		+0.15		3, 4
Gain tracking OHT state, on hook	0 dBm to –37	0 to +70° C	–0.10		+0.10		
		–40 to +85° C	–0.15		+0.15		
	+3 dBm to 0 dBm		–0.35		+0.35		3
Group delay	0 dBm, 1kHz			3		µs	1, 4, 6

Line Characteristics

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_L, Loop-current accuracy	I_L in constant-current region, B2EN=0	$0.87I_L$	I_L	$1.085I_L$	mA	
I_L, Long Loops, Active state	R_{LDC} = 600 Ω, RSGL = open	20	21.7			
	R_{LDC} = 750 Ω, RSGL = short	20				
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT1}\rvert - 10\ V}{R_L + 400}$	$0.8I_L$	I_L	$1.2I_L$		
	I_L = constant-current region TA = 25° C	18	27	39		
	–40 to +85° C	18	27			4
I_LLIM	Active, A and B to ground		55	110		
	OHT, A and B to ground		55			4
I_L, Loop current, Open Circuit state	R_L = 0			100	µA	
I_A, Pin A leakage, Tip Open state	R_L = 0			100		
I_B, Pin B current, Tip Open state	B to ground		34		mA	
VA, Standby, ground start signaling	A to –48 V = 7 kΩ, B to ground = 100 Ω	–7.5	–5		V	4
V_{AB}, Open Circuit voltage		42.8				8

Power Supply Rejection Ratio

(V_{RIPPLE} = 100 mVrms), Active Normal State

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{CC}	50 to 3400 Hz	33	50		dB	5
V_{NEG}	50 to 3400 Hz	30	40			
V_{BAT1}	50 to 3400 Hz	30	50			
V_{BAT2}	50 to 3400 Hz	30	50			

Power Dissipation

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
On hook, Open Circuit state	V_{BAT1}		48	100	mW	
On hook, Standby state	V_{BAT2}		55	80		10
On hook, OHT state	V_{BAT1}		200	300		
On hook, Active state	V_{BAT1}		220	350		
Off hook, Standby state	V_{BAT1} or V_{BAT2} R_L = 300 Ω		2000	2800		10
Off hook, OHT state	V_{BAT1} R_L = 300 Ω		2000	2200		
Off hook, Active state	V_{BAT2} R_L = 300 Ω		550	750		

Supply Currents

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_{CC}, On-hook V_{CC} supply current	Open Circuit state		3.0	4.5	mA	
	Standby state		3.2	5.5		
	OHT state		6.2	8.0		
	Active state-normal		6.5	9.0		
I_{NEG}, On-hook V_{NEG} supply current	Open Circuit state		0.1	0.2		
	Standby state		0.1	0.2		
	OHT state		0.7	1.1		
	Active state-normal		0.7	1.1		
I_{BAT}, On-hook V_{BAT} supply current	Open Circuit state		0.45	1.0		
	Standby state		0.6	1.5		
	OHT state		2.0	4.0		
	Active state-normal		2.7	5.0		

Logic Inputs

(Applies to C3–C1, D2–D1, E1, and B2EN).

Description	Test Conditions	Min	Typ	Max	Unit	Note
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				

Logic Output

($\overline{DET}$)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{OL}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				

Ring-Trip Detector Input

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Ring detect accuracy	$IRTD = \left(\frac{\lvert BAT1\rvert - 1}{RRT1} + 24\ \mu A\right) \bullet 335$		–10		+10	%

Ring Signal

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{AB}, Ringing	BAT1 = –75 V, Ringload = 1570 Ω	66	69		Vpk	7
V_{AB}, Ringing offset	V_{RINGIN} = 2.5 V	–10	0	10	V	
$\Delta V_{AB} / \Delta V_{RINGIN}$(RINGIN gain		150	180	210		

Ground-Key Detector Thresholds

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Ground-key resistive threshold	B to ground	2	5	10	kΩ	
Ground-key current threshold	B to ground		11		mA	

Loop Detector

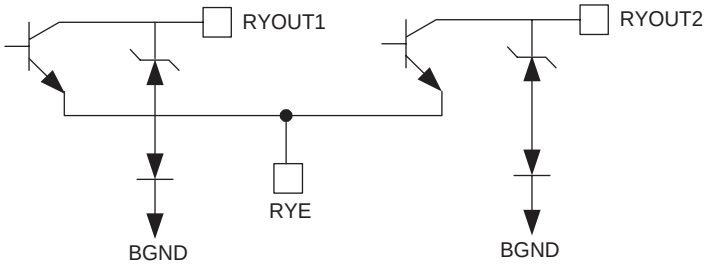
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
R_{LTH}, Loop-resistance detect threshold	Active, V_{BAT1}	–20		20	%	9
	Active, V_{BAT2}	–20		20		
	Standby	–15		15		

Relay Driver Output

(Relay 1 and 2)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{OL}, On voltage (each output)	I_{OL} = 30 mA		+0.25	+0.4	V	
V_{OL}, On voltage (each output)	I_{OL} = 40 mA		+0.30	+0.8		4
I_{OH}, Off leakage (each output)	V_{OH} = +5 V			100	µA	
Zener breakover (each output)	I_Z = 100 µA	6.6	7.9		V	
Zener on voltage (each output)	I_Z = 30 mA		11			

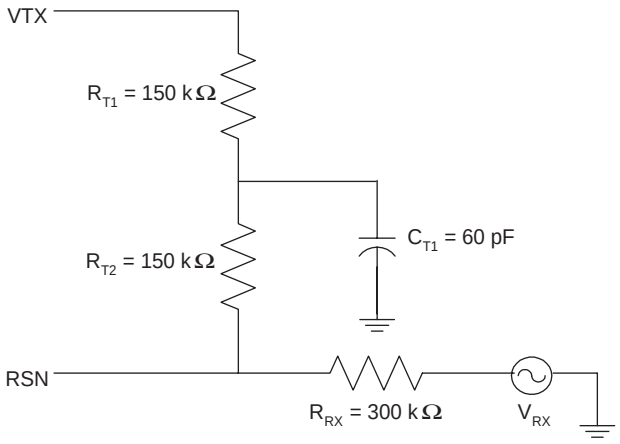
RELAY DRIVER SCHEMATIC



Note:

1. *Unless otherwise noted, test conditions are BAT1 = –75 V, BAT2 = –24 V, V_{CC} = +5 V, V_{NEG} = –5 V, R_L = 600 Ω, R_{DC1} = 80 kΩ, R_{DC2} = 20 kΩ, R_D = 75 kΩ, no fuse resistors, C_{HP} = 0.018 µF, C_{DC} = 1.2 µF, D_1 = D_2 = 1N400x, two-wire AC input impedance (ZSL) is a 600 Ω resistance synthesized by the programming network shown below. R_{SGL} = open, R_{SGH} = open, R_{DCR1} = 15 kΩ, R_{DCR2} = 2 kΩ, C_{DCR} = 10 nF, R_{RT1} = 430 kΩ, R_{RT2} = 12 kΩ, C_{RT} = 1.5 µF, R_{SLEW} = 100 kΩ, C_{SLEW} = 0.33 µF.*

Figure 2. AC Input Impedance Programming Network



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.*
7. *70 Vpk provides 50 Vrms with a crest factor of 1.25 to a load of 1400 Ω with 2 • Rf = 100, and Rline = 70 Ω (1570 Ω).*
8. *Open Circuit V_{AB} can be modified using R_{SGH}.*
9. *R_D must be greater than 56 kΩ. See User-Programmable Components, on page 14. for typical value of R_{LTH}.*
10. *Lower power is achieved by switching into low-battery state in standby. Standby loop current is returned to V_{BAT1} regardless of the battery selected.*

SLIC Device Decoding

State	C3	C2	C1	Two-Wire Status	$\overline{\text{DET}}$ Output E1 = 1	$\overline{\text{DET}}$ Output E1 = 0	Battery
0	0	0	0	Open Circuit	Ring trip	Ring trip	B2EN
1	0	0	1	Ringing	Ring trip	Ring trip	
2	0	1	0	Active	Loop detector	Ground key	
3	0	1	1	On-hook TX (OHT)	Loop detector	Ground key	
4	1	0	0	Reserved	Loop detector	Ground key	B2EN = 1**
5	1	0	1	Standby	Loop detector	Ground key	V_{BAT1}
6*	1	1	0	Active Polarity Reversal	Loop detector	Ground key	B2EN
7*	1	1	1	OHT Polarity Reversal	Loop detector	Ground key	

Note:

** Only –1 and –2 performance grade device supports polarity reversal.*

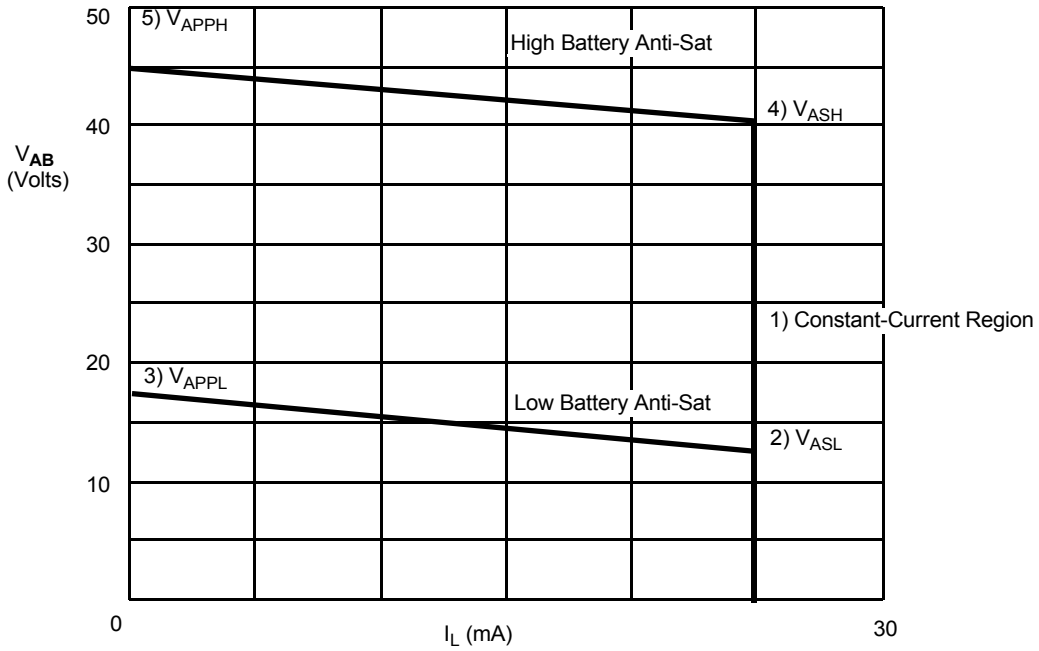
*** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.*

User-Programmable Components

$Z_T = 500(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 500(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{LOOP}}$ $R_{DCR1} + R_{DCR2} = \frac{3000}{I_{RINGLIM}}$ $C_{DC} = 19\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$ $C_{DCR} = \frac{R_{DCR1} + R_{DCR2}}{R_{DCR1}R_{DCR2}} \bullet 150\ \mu s$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. I_{LOOP} is the desired loop current in the constant-current region. $R_{\mathbf{DCR1}}$, $R_{\mathbf{DCR2}}$, and $C_{\mathbf{DCR}}$ form the network connected to the R**DCR** pin. See *Application Circuit*, on page 21. for these components. $C_{\mathbf{DCR}}$ sets the ringing time constant, which can be between 15 µs and 150 µs.
$R_D = R_{LTH} \bullet 12.67$ for high battery state	R_D is the resistor connected from the RD pin to GND and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection. R_D should be greater than 56 kΩ to guarantee detection occurs in the Standby state. Choose the value of $R_{\mathbf{D}}$ for high battery state; then use the equation for $R_{\mathbf{LTH}}$ to find where the threshold is for low battery.
Loop-Threshold Detect Equations	
$R_{LTH} = \frac{R_D}{12.67}$ for high battery state	This is the same equation as for $R_{\mathbf{D}}$ above, except solved for $R_{\mathbf{LTH}}$.
$R_{LTH} = \frac{R_D}{11.37}$ for Active state	For low battery, the detect threshold is slightly higher, which avoids oscillating between states.
$R_{LTH} = \frac{\lvert V_{BAT1}\rvert - 10}{915} \bullet R_D - 400 - 2R_F$	R_{LTH} Standby < R_{LTH} Active V_{BAT1} < $R_{\mathbf{LTH}}$ Active V_{BAT2}, which guarantees no unstable states under all operating conditions. This equation shows at what resistance the Standby threshold is; it is actually a current threshold rather than a resistance threshold, which is shown by the V_{BAT} dependency.

DC FEED CHARACTERISTICS

Figure 3. Typical V_{AB} vs. I_L DC Feed Characteristics



$R_{DC} = R_{DC1} + R_{DC2} = 20\ k\Omega + 80\ k\Omega = 100\ k\Omega$

$(V_{BAT1} = -75\ V, V_{BAT2} = -24\ V)$

Notes:

1. *Constant-current region:* $V_{AB} = I_L R_L = \frac{2500}{RDC} R_L$; *where* $R_L = R_L + 2R_F$,

2. *Low battery* $V_{ASL} = \frac{1000 \bullet (104 \bullet 10^3 + R_{SGL})}{6720 \bullet 10^3 + (80 \bullet R_{SGL})}$; *where R_{SGL} = resistor to GND, B2EN = logic Low.*

   Anti-sat region: $V_{ASL} = \frac{1000 \bullet (R_{SGL} - 56 \bullet 10^3)}{6720 \bullet 10^3 + (80 \bullet R_{SGL})}$; *where R_{SGL} = resistor to V_{CC}, B2EN = logic Low.*

   R_{SGL} to V_{CC} must be greater than 100 kΩ.

3. $V_{APPL} = 4.17 + V_{ASL}$

   $I_{LOOPL} = \frac{V_{APPL}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$

4. *High battery* $V_{ASH} = V_{ASHH} + V_{ASL}$

   Anti-sat region: $V_{ASHH} = \frac{1000 \bullet (70 \bullet 10^3 + R_{SGH})}{1934 \bullet 10^3 + (31.75 \bullet R_{SGH})}$; *where R_{SGH} = resistor to GND, B2EN = logic High.*

   $V_{ASHH} = \frac{1000 \bullet (R_{SGH} + 2.75 \bullet 10^3)}{1934 \bullet 10^3 + (31.75 \bullet R_{SGH})}$; *where R_{SGH} = resistor to V_{CC}, B2EN = logic High.*

   R_{SGH} to V_{CC} must be greater than 100 kΩ.

5. $V_{APPH} = 4.17 + V_{ASH}$

   $I_{LOOPH} = \frac{V_{APPH}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$

RING-TRIP COMPONENTS

R_{RT2} = 12 kΩ

C_{RT} = 1.5 µF

$$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 3.5 - (15\ \mu A \bullet 300 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

where R_{LRT} = Loop-detection threshold resistance for ring trip and CF = Crest factor of ringing signal (≈ 1.25)

R_{SLEW}, C_{SLEW}

Ring waveform rise time ≈ 0.214 • (R_{SLEW} • C_{SLEW}) ≈ tr.

For a 1.25 crest factor @ 20 Hz, tr ≈ 10 mS.

∴ (R_{SLEW} = 150 kΩ, C_{SLEW} = 0.33 µF.)

C_{SLEW} should be changed if a different crest factor is desired.

Figure 4. Ringing Waveforms

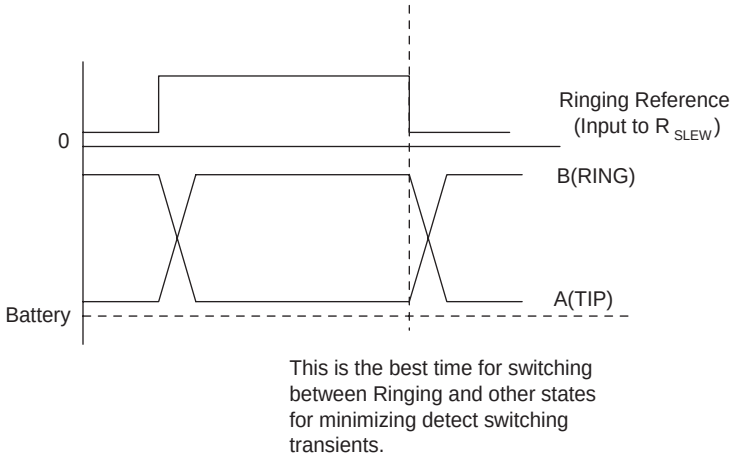
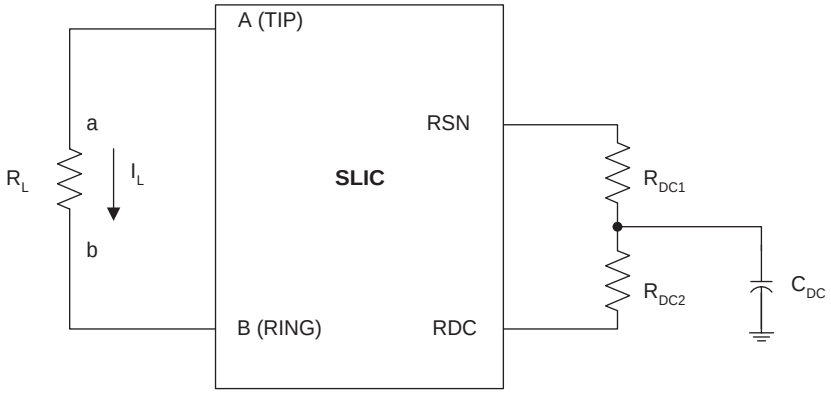


Figure 5. Feed Programming



Feed current programmed by R_{DC1} and R_{DC2}

TEST CIRCUITS

Figure 6. Two-to-Four-Wire Insertion Loss

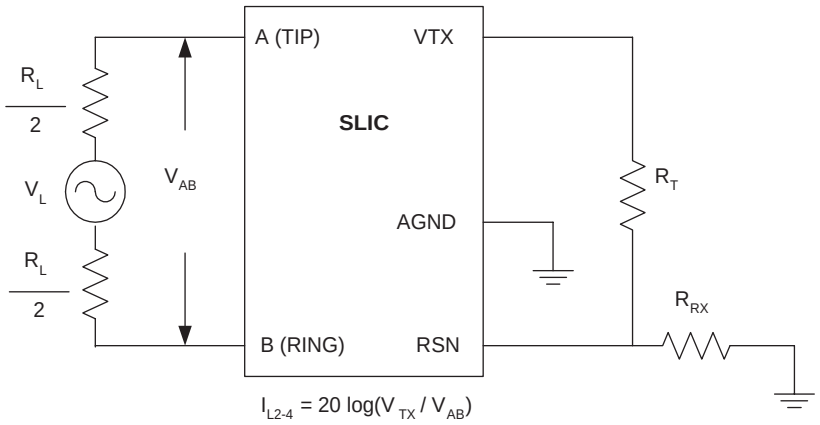


Figure 7. Four-to-Two-Wire Insertion Loss and Four-to-Four-Wire Balance Return Signal

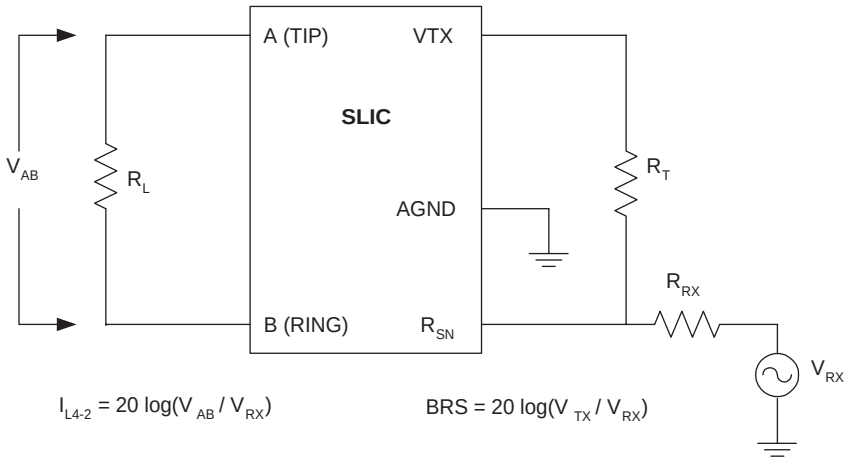


Figure 8. Longitudinal Balance

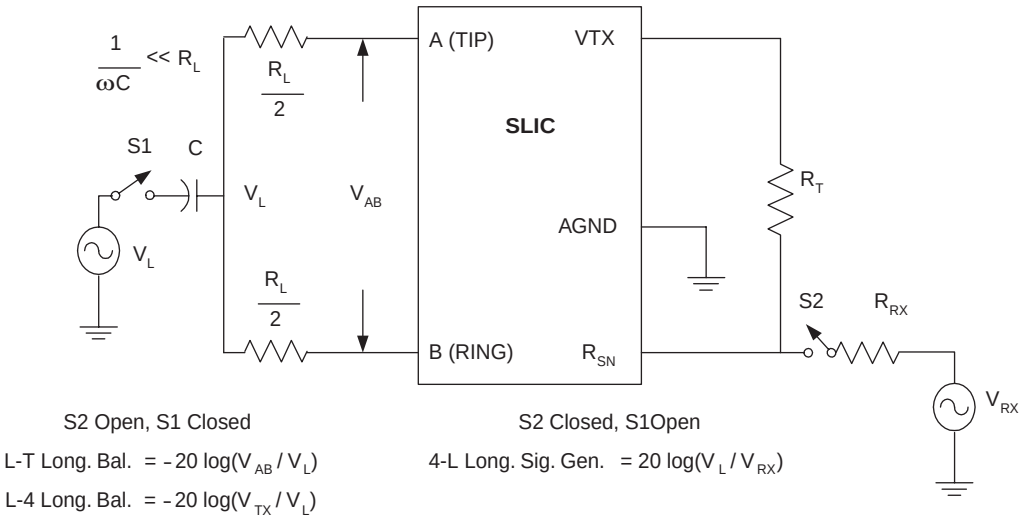


Figure 9. Two-Wire Return Loss Test Circuit

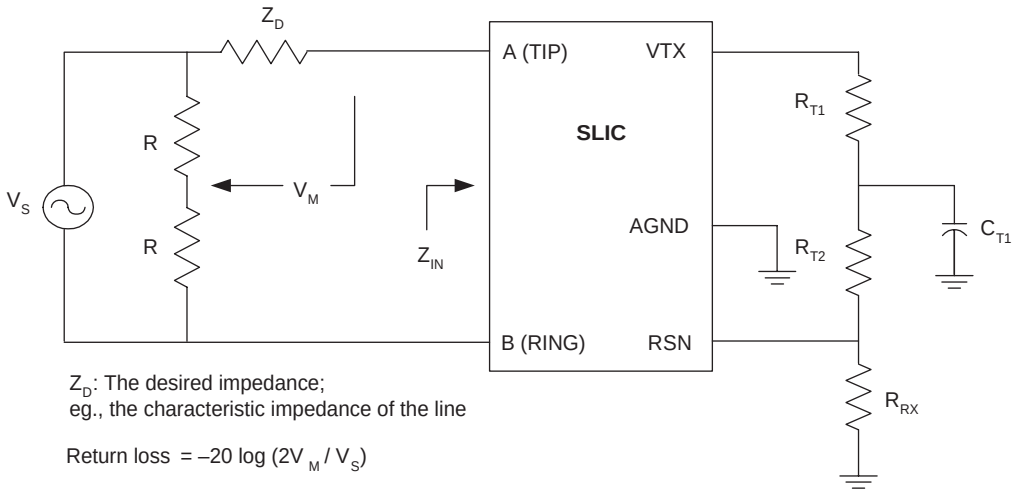


Figure 10. Loop-Detector Switching

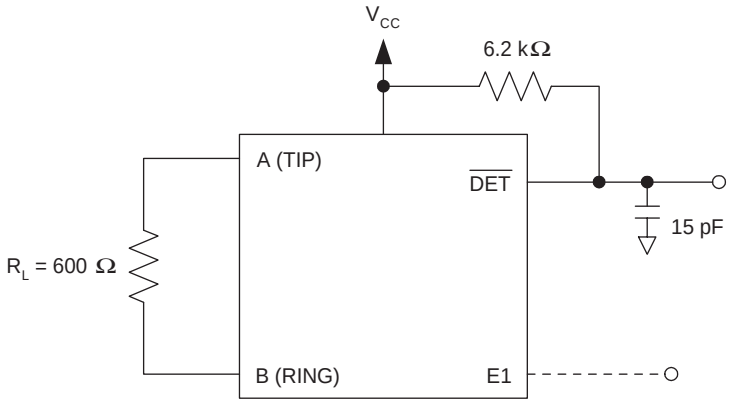


Figure 11. Ground-Key Switching

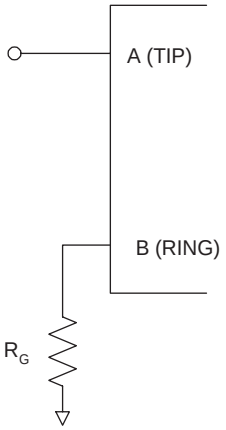
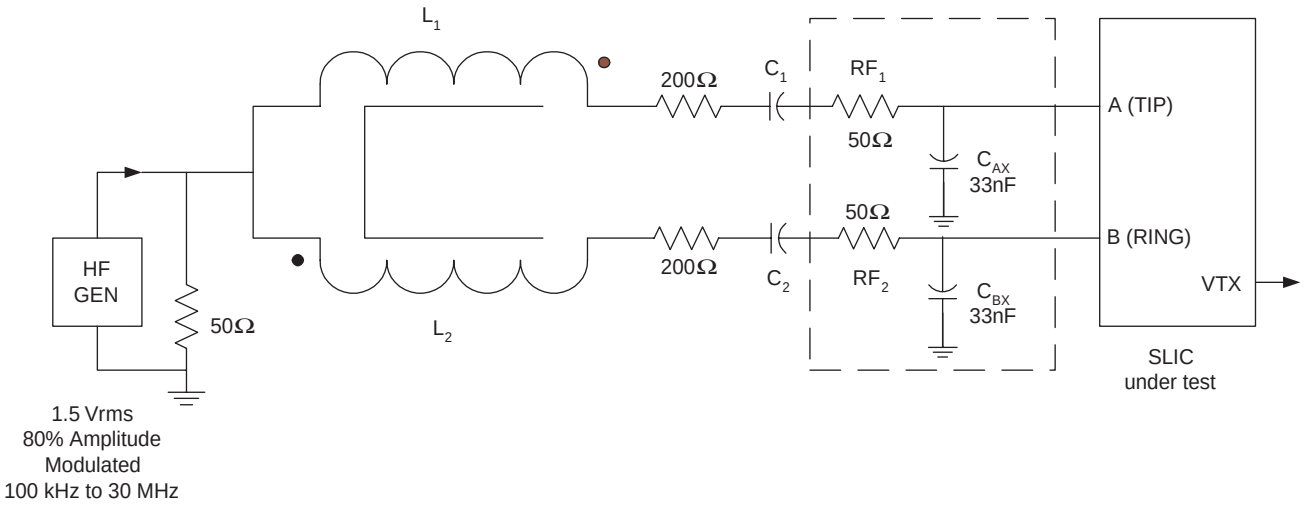
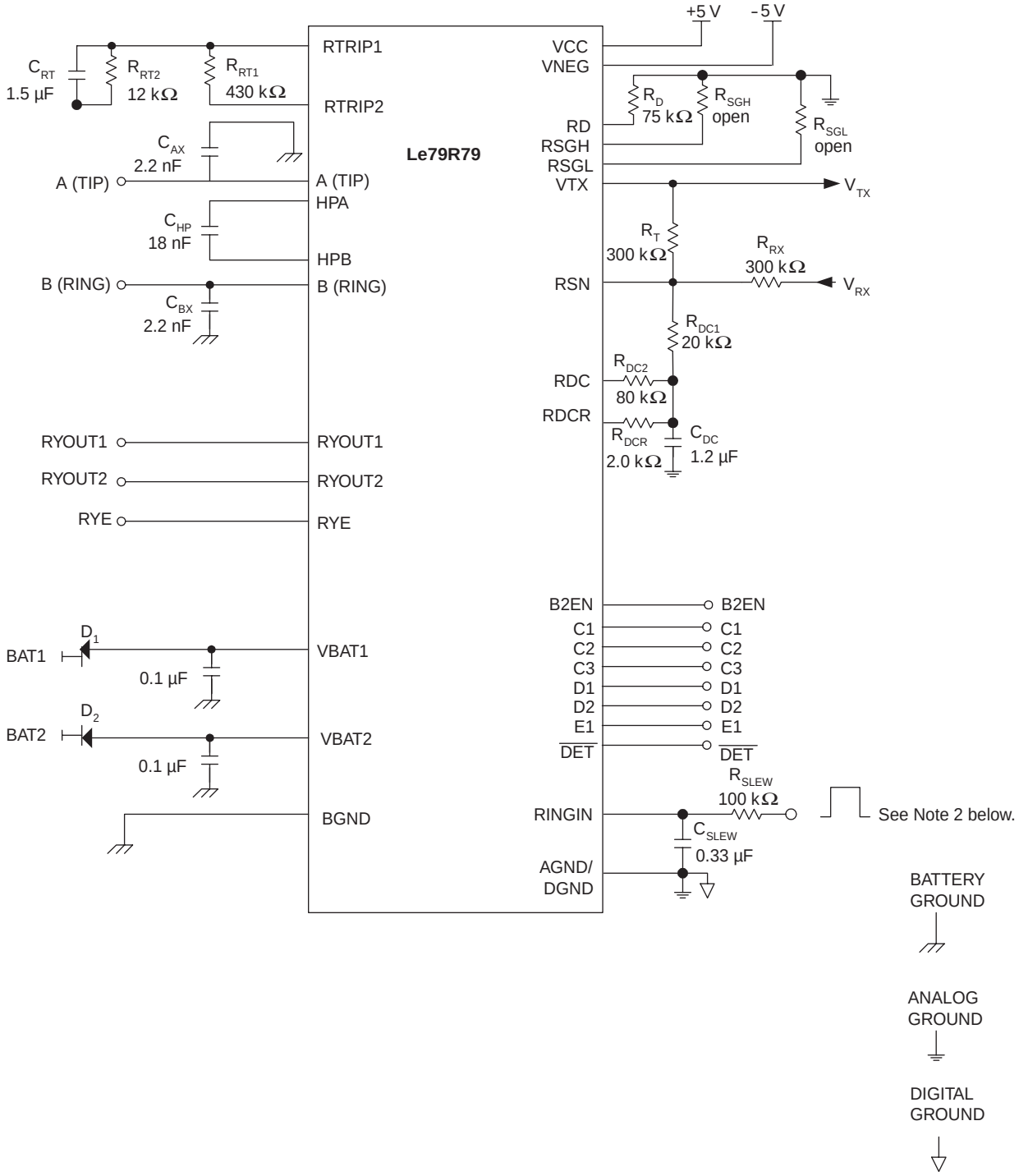


Figure 12. RFI Test Circuit



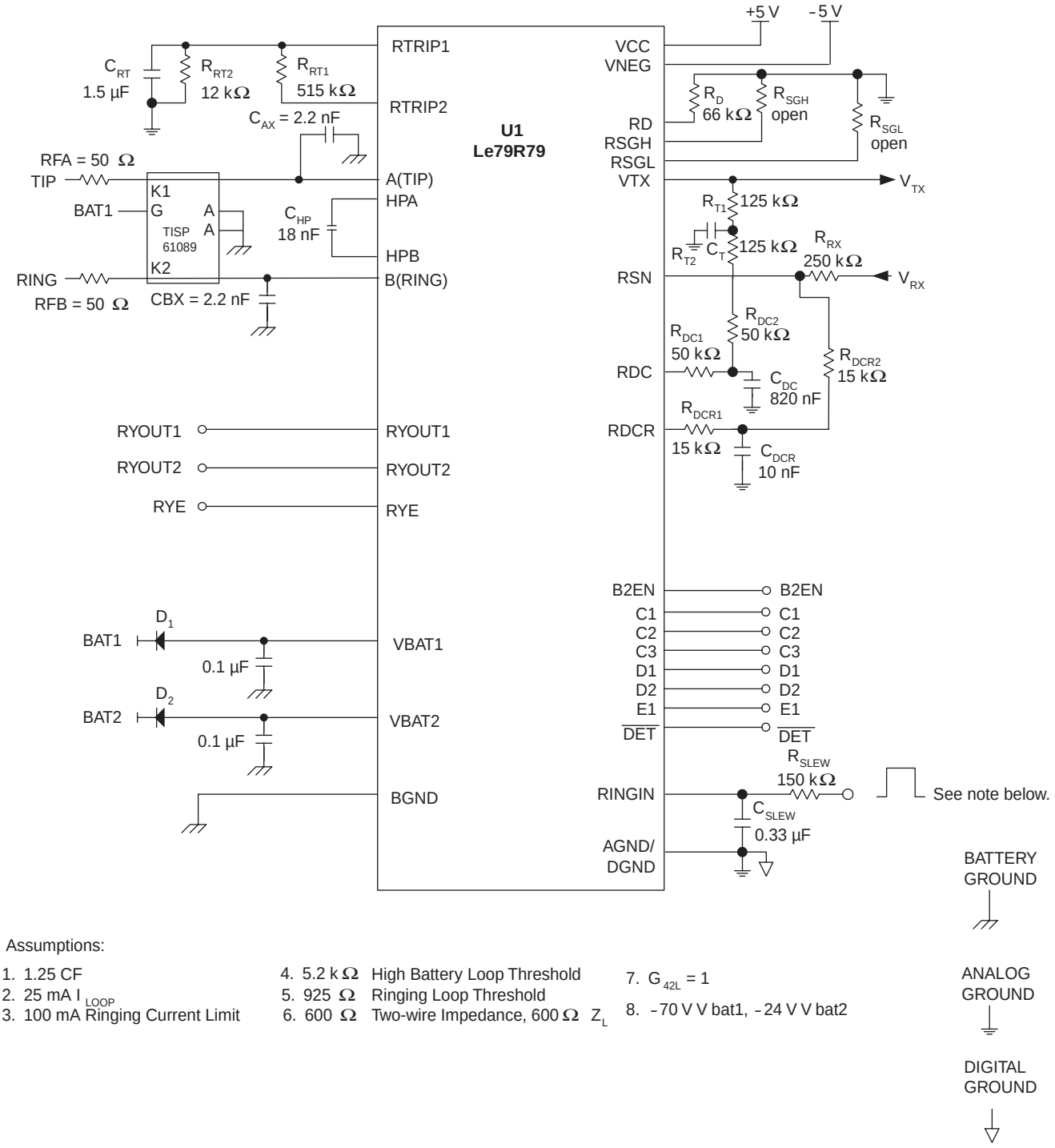
Le79R79 TEST CIRCUIT



Note:

1. *Refer to the Applications Circuit on the next page for recommended configuration.*
2. *The input should be 50% duty cycle CMOS-compatible input.*

APPLICATION CIRCUIT



Assumptions:

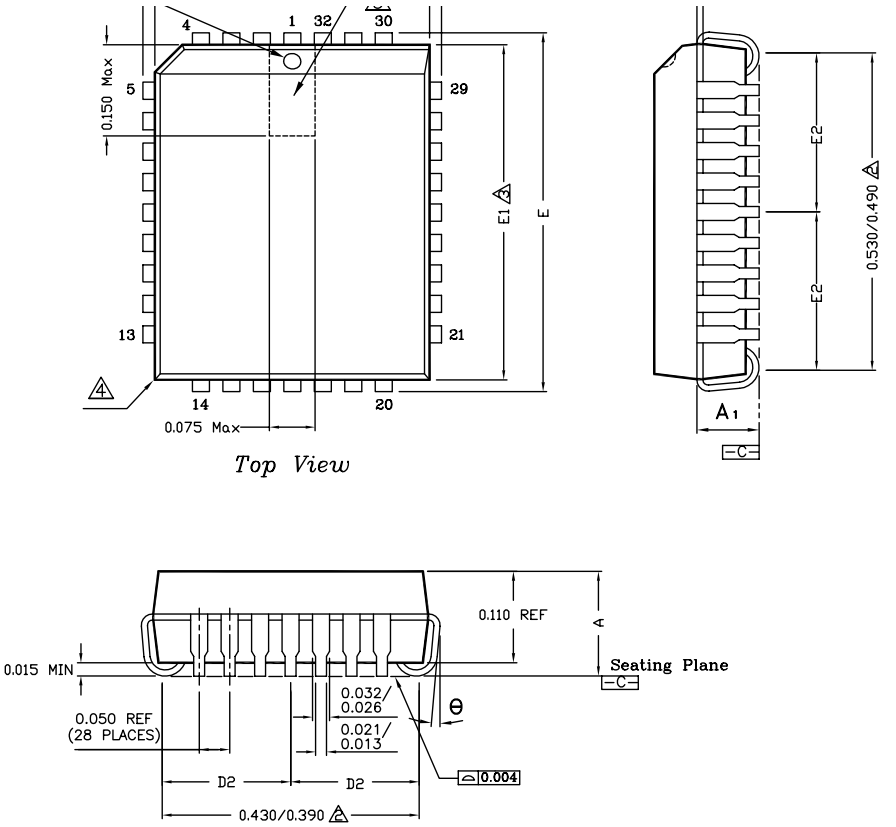
1. 1.25 CF
2. 25 mA I_{LOOP}
3. 100 mA Ringing Current Limit
4. 5.2 kΩ High Battery Loop Threshold
5. 925 Ω Ringing Loop Threshold
6. 600 Ω Two-wire Impedance, 600 Ω Z_L
7. $G_{42L} = 1$
8. -70 V V bat1, -24 V V bat2

Note:

The input should be 50% duty cycle CMOS-compatible input.

PHYSICAL DIMENSIONS

32-pin PLCC



32-Pin PLCC			
JEDEC # MS-016			
Symbol	**Min**	**Nom**	**Max**
A	0.125	--	0.140
A1	0.075	0.090	0.095
D	0.485	0.490	0.495
D1	0.447	0.450	0.453
D2		0.205 REF	
E	0.585	0.590	0.595
E1	0.547	0.550	0.553
E2		0.255 REF	
Θ	0 deg	--	10 deg

NOTES:

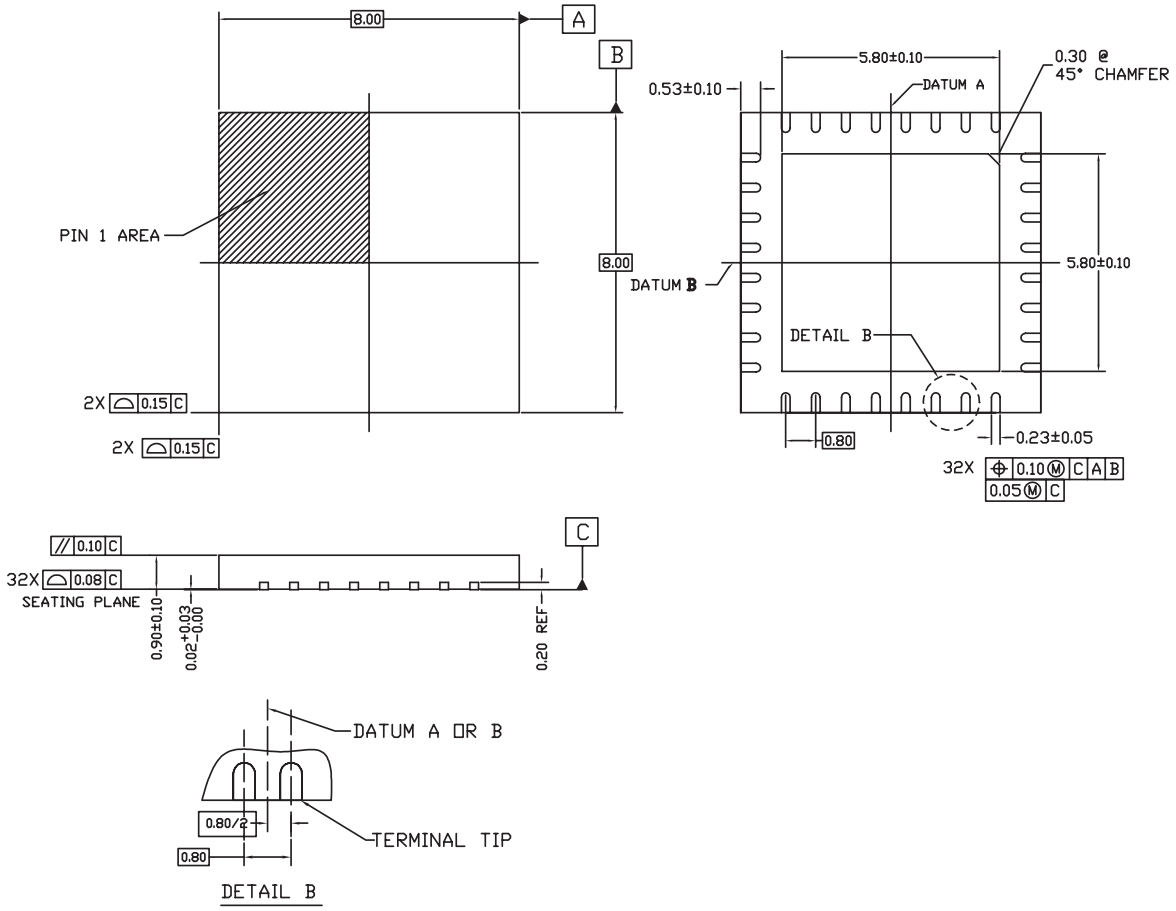
1. Dimensioning and tolerancing conform to ASME Y14,5M-1994.
2. To be measured at seating plan - C - contact point.
3. Dimensions “D1” and “E1” do not include mold protrusion. Allowable mold protrusion is 0.010 inch per side. Dimensions “D” and “E” include mold mismatch and determined at the parting line; that is “D1” and “E1” are measured at the extreme material condition at the upper or lower parting line.
4. Exact shape of this feature is optional.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Sum of DAM bar protrusions to be 0.007 max per lead.
7. Controlling dimension : Inch.
8. Reference document : JEDEC MS-016

32-Pin PLCC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

32-pin QFN



Symbol	32 LEAD QFN		
	Min	Nom	Max
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0.00	0.02	0.05
A3		0.20 REF	
aaa		0.20	
bbb		0.10	
ccc		0.10	

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. ⌖ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

32-Pin QFN

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision B to C

- Minor changes were made to the data sheet style and format to conform to Zarlink standards.
- Electrical Characteristics; Last row under Ring Signal, min changed from 130 to 150, typ changed from 160 to 180, and max changed from 190 to 210.
- SLIC Decoding Table; Added B2EN reference to the Battery Selection column and its corresponding note to the notes section.
- Applications Circuit; Revised

Revision C to D

- Minor changes were made to the data sheet style and format to conform to Zarlink standards.

Revision D to E

- On pages 17 and 18, R_{DC1} and R_{DC2} were switched.

Revision E to F

- The physical dimensions (PL032) were added to the Physical Dimensions section.
- Deleted the Ceramic DIP and Plastic DIP packages and references to them.
- Updated the Pin Description table to correct inconsistencies.

Revision F to G

- The equation on page 13 was changed:

from: $$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 3.5 - (15\ \mu A \bullet 300 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

to: $$R_{RT1} = 320 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 5 - (24\ \mu A \bullet 320 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

Revision G to H

- In “Ordering Information” section, added description for wafer foundry facility optional character.

Revision H to I

- Updated document format
- Added OPNs for QFN package to Ordering Information table
- Added physical dimensions for 8x8 QFN package

Revision I to J1

- Added green package OPN to *Ordering Information*, on page 1
- Added *Package Assembly*, on page 7
- Updated document format

Revision J1 to K1

- Added Note 3 to *Connection Diagrams*, on page 5

Revision K1 to L1

- Added "Packing" column and Note 2 and 4 to *Ordering Information*, on page 1
- Updated 32QFN drawing in *Physical Dimensions*, on page 22

Revision L1 to M1

- Added option for PLCC green package to *Ordering Information*, on page 1
- Added option for QFN green package for dash grades 2 through 4 in *Ordering Information*, on page 1
- Added note to *Physical Dimensions*, on page 22

Revision M1 to N1

- Removed OPNs for all non-green packaged parts from *Ordering Information*, on page 1
- Removed 79R79-3QC, 79R79-4JC and 79R79-4QC from *Ordering Information*, on page 1

Revision N1 to N2

- Removed reference to Le79R79-4 option from *Ordering Information*, on page 1

Revision N2 to O1

- Changed I_L Loop-Current Accuracy from 0.915 to 0.87 in *Electrical Characteristics*.

Revision O1 to O2

- Enhanced format of package drawings in *Physical Dimensions*, on page 22
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com