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PRODUCT DESCRIPTION

The VE790 series voice chip sets integrate all functions of the subscriber line for four subscriber lines. One or more of two chip types are used to implement the line card; a VE790 series ISLIC device and a Le79228 Quad ISLAC device. These provide the following basic functions:

1. The VE790 series ISLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le79228 Quad ISLAC device: A low voltage CMOS IC that provides conversion and DSP functions for all four channels.

Complete schematics of line cards using the Le79228 Quad ISLAC device for internal and external ringing are shown in *Application Circuits*, on page 28.

The VE790 series ISLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the Quad ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The VE790 series ISLIC device is designed to be used exclusively with the Le79228 Quad ISLAC device as part of a multiple-line chip set.

The VE790 series ISLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the VE790 series ISLIC chip by dissipating excess power in external resistors.

Each Le79228 Quad ISLAC device contains high-performance analog circuits that provide A/D and D/A conversion for voice (codec/filter), DC-feed and supervision signals for four subscriber channels. The Le79228 Quad ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all four channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Le79228 Quad ISLAC device provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge and allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The VE790 series ISLIC device interface unit inside the Le79228 Quad ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the Le79228 Quad ISLAC device to place several key VE790 series ISLIC device performance parameters under software control.

The main functions that can be observed and/or controlled through the Le79228 Quad ISLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the VE790 series ISLIC device collects the following information and feeds it, in analog form, to the Le79228 Quad ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltages

The outputs supplied by the Le79228 Quad ISLAC device to the VE790 series ISLIC device are then:

- A voltage (VHL_i*) that provides control for the following high-level VE790 series ISLIC device outputs:
- DC loop current

- Internal ringing signal
- 12- or 16-kHz metering signal
- A low-level voltage proportional to the voice signal ($VOUT_i$)
- A voltage that controls longitudinal offset for test purposes (VLB_i)

The Le79228 Quad ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC™ software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

Besides the codec/filter functions, the Le79228 Quad ISLAC device provides all the sensing, feedback, and clocking necessary to completely control VE790 series ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The Le79228 Quad ISLAC device supplies complete mode control to the VE790 series ISLIC device using the control bus and (P1-P3) tri-level load signal (LD_i).

The Le79228 Quad ISLAC device provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

Note:

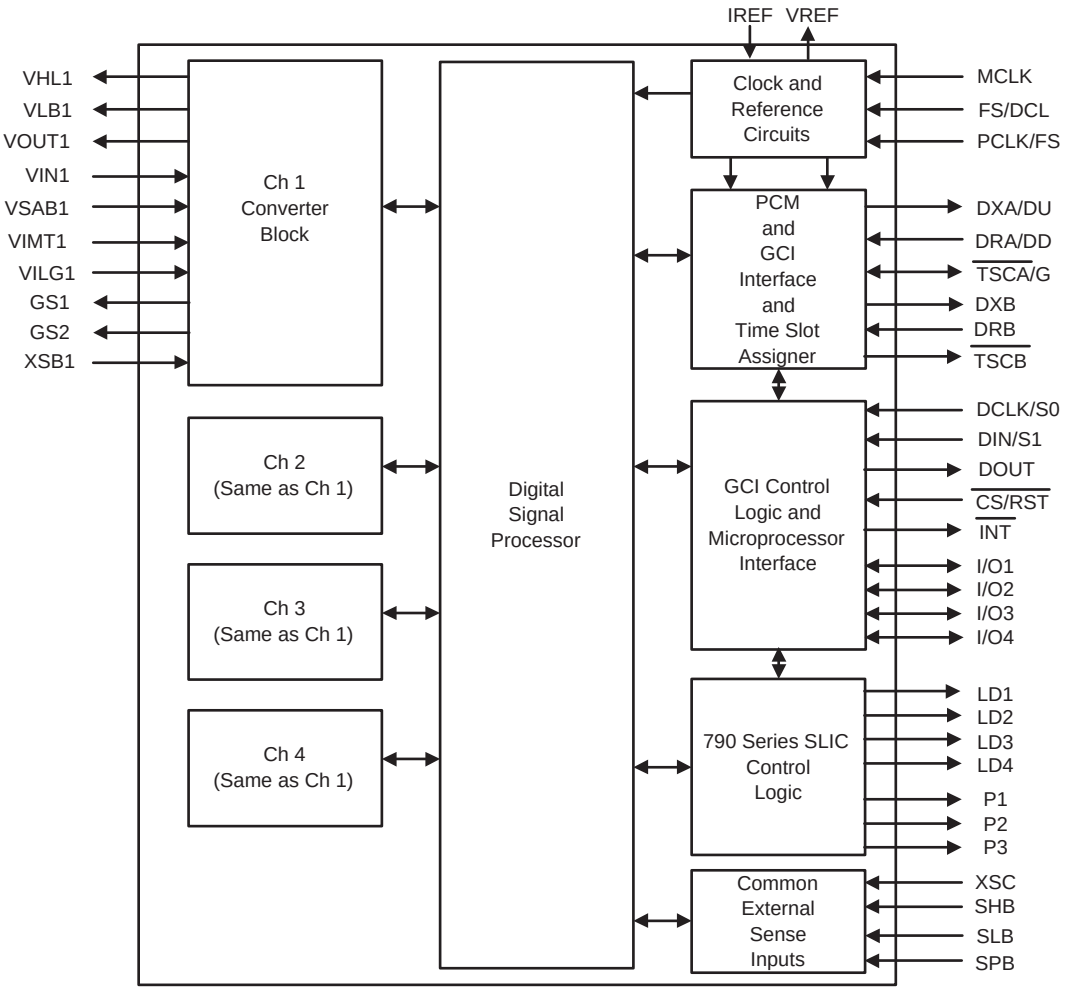
"i" denotes channel number

OPTIONAL VCP FEATURES

Optional Voice Control Processor (VCP) features provide the following solutions to the VE790 series intelligent chip sets:

- Integrated test software routines
- DTMF detection
- Aggregated codec/filter control

Le79228 Quad ISLAC™ Device Internal Block Diagram (80-Pin LQFP)



Features of the Le79228 Quad ISLAC™ Chip Set

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency (for balanced ringing)
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
    - –Off-hook debounce circuit
    - –Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/μ-law and linear selection
- Supports internal and external battery-backed or earth-backed ringing
  - Self-contained ringing generation and control
  - Supports external ringing generator and ring relay
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Tone generation
  - DTMF
  - FSK
  - Random noise
  - Arbitrary tone
- Built-in voice path test modes
- Power-cross, fault, and foreign voltage detection
- Meets GR-909 and GR-844 test requirements
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Small physical size
- Up to three relay drivers per VE790 series ISLIC device
  - Configurable as test load switches

CONNECTION DIAGRAMS

Figure 1. 64-Pin TQFP Connection Diagram

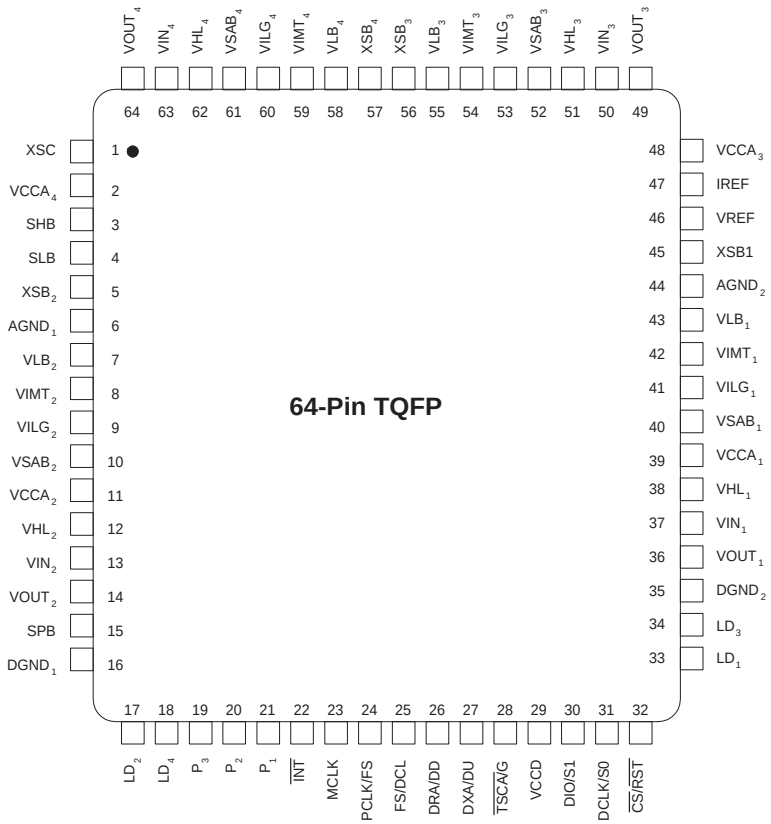
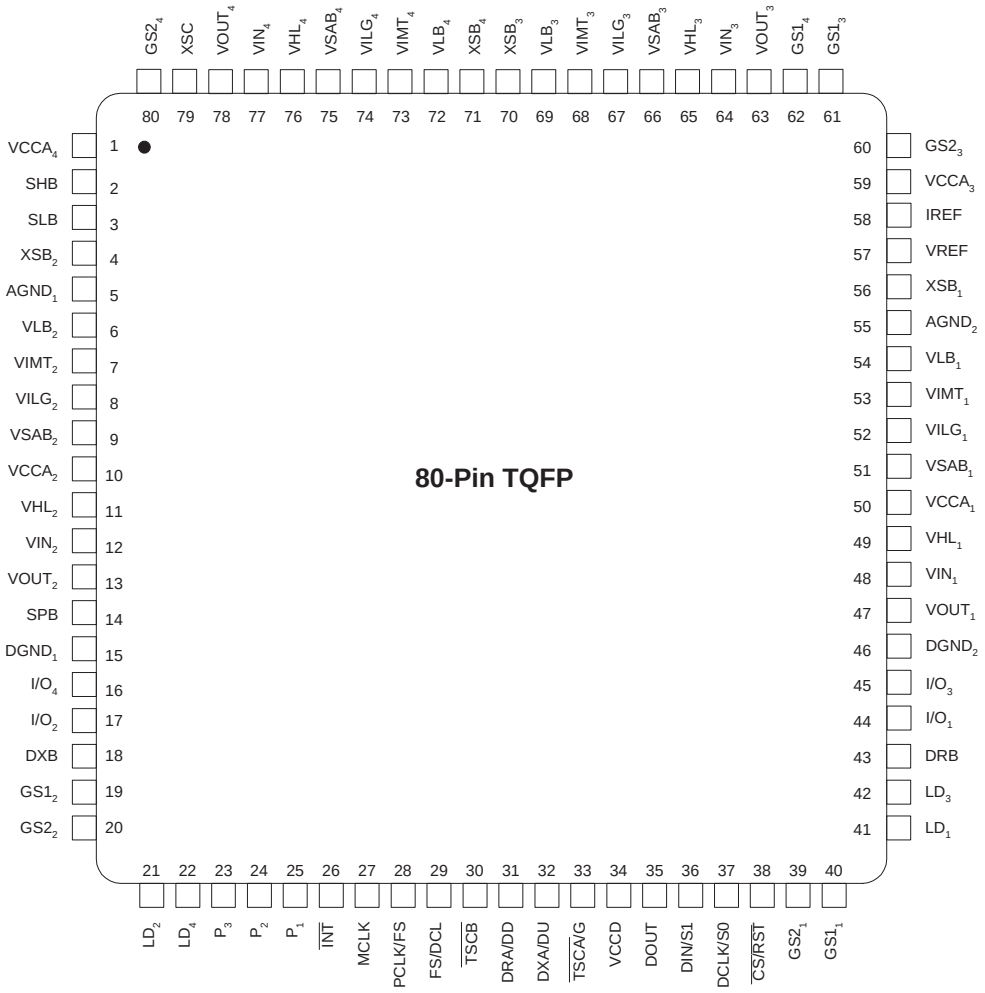


Figure 2. 80-Pin LQFP Connection Diagram



PIN DESCRIPTIONS

Pin Name	Type	Description
$AGND_1$, $AGND_2$	Ground	Analog circuitry ground returns
$\overline{CS}/\overline{RST}$	Input	For PCM backplane operation, a logic Low on this pin for 16 or more DCLK cycles resets the sequential logic in the Le79228 Quad ISLAC device into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into or out of the DIO port. For GCI operation, a logic low on this pin for 1 µs or longer resets the sequential logic into a known mode. This pin is 5-V tolerant.
DCLK/S0	Input	Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0. This pin is 5-V tolerant.
$DGND_1$, $DGND_2$	Ground	Digital ground returns
DIN/S1	Input	For PCM backplane operation, control data is serially written into the Le79228 Quad ISLAC device via the DIN pin with the MSB first. The data clock (DCLK) determines the data rate. For GCI operation, this pin is device address bit 1. This pin is 5 V tolerant. DIN/S1 is available only on the 80-pin LQFP package.
DIO/S1	Input/ Output	For PCM backplane operation, control data is serially written into and read out of the Le79228 Quad ISLAC device via the DIO pin with the MSB first. The data clock (DCLK) determines the data rate. DIO is high impedance except when data is being transmitted from the Le79228 Quad ISLAC device under control of $\overline{CS}/\overline{RST}$. For GCI operation, this pin is device address bit 1. This pin is 5-V tolerant. DIO/S1 is available only on the 64-pin TQFP package.
DOUT	Output	For PCM backplane operation, control data is serially read out of the Le79228 Quad ISLAC device via the DOUT pin with the MSB first. The data clock (DCLK) determines the data rate. DOUT is high impedance except when data is being transmitted from the Le79228 Quad ISLAC device under control of $\overline{CS}/\overline{RST}$. This pin is 5-V tolerant. DOUT is available only on the 80-pin LQFP package.
DRA/DD, DRB	Input	For the PCM highway, the receive PCM data is input serially through the DRA or DRB pins. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the VE790 series ISLIC device. This mode is selected in Device Configuration Register 2 (RTSEN=1, RTSMD=1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. This pin is 5 V tolerant. The DRB pin is available only on the 80-pin LQFP package.
DXA/DU, DXB	Output	For the PCM highway, the transmit PCM data is transmitted serially through the DXA or DXB pins. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN= 1, RTSMD=1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. This pin is 5 V tolerant. The DXB pin is available only on the 80-pin LQFP package.
FS/DCL	Input	For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The Le79228 Quad ISLAC device references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the data rate is 2 MHz and DCL must be either 2 or 4 MHz. This pin is 5-V tolerant.
$GS1_1$–$GS1_4$, $GS2_1$–$GS2_4$	Output	Gain select nodes for VILG and VIMT inputs. This node provides a switched tie point to VREF. The GS pins are available only on the 80-pin LQFP package.
$VILG_1$–$VILG_4$	Input	Longitudinal current input from ISLIC device. Voltage generated by RLG is sensed by this pin. Tie pin to VREF if channel unused.
$VIMT_1$–$VIMT_4$	Input	Metallic current input from ISLIC device. Voltage generated by RMT is sensed by this pin. Tie pin to VREF if channel unused.
$\overline{INT}$	Output	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at channel configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs.
I/O_1–I/O_4	Input/ Output	General purpose, logic input/output connection for each of 4 channels. These control lines can be programmed as an input or output in the Global I/O Direction Register. When programmed as outputs, they can control an external logic device. When programmed as inputs, they can monitor external logic circuits. Data for these pins can be written or read individually (from the channel specific I/O Register) or as a group (from the Global I/O Data Register). The I/O pins are available only on the 80-pin LQFP package.
IREF	Input	External resistor (R_{REF}) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the Le79228 Quad ISLAC device.

Pin Name	Type	Description
LD_1–LD_4	Output	The LD pins output 3-level voltages. When LD_i is a logic 0 (< 0.4 V), the destination of the code on P_1–P_3 is the relay control latches in the VE790 series ISLIC device control register. When LD_i is a logic 1 (>V_{CC}–0.4 V), the destination of P_1–P_3 is the mode control latches. LD_i is driven to VREF when the contents of the VE790 series ISLIC device control register must not change.
MCLK	Input	For PCM backplane operation, the DSP master clock may connect here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies, but must be synchronous to FS. Upon initialization, the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. This pin is 5-V tolerant.
PCLK/FS	Input	For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see above). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any integer multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The Le79228 Quad ISLAC device references individual timeslots with respect to this input, which must be synchronized to DCL. This pin is 5-V tolerant.
P_1–P_3	Output	Control the operating modes of the VE790 series ISLIC devices connected to the Le79228 Quad ISLAC device.
SHB, SLB, SPB	Input	Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both negative battery resistors to the same supply. If two negative batteries are used, SHB must be connected to the battery intended to supply on-hook voltage, whether BATH or BATL. If the positive battery is not used, leave the SPB pin unconnected. These pins are current inputs whose voltage is held at VREF.
$\overline{\text{TSCA}}$/G	Output (PCM) Input (GCI)	For PCM backplane operation, $\overline{\text{TSCA}}$ is active low when PCM data is output on the DXA or DXB pins, respectively. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{\text{TSCA}}$/G to DGND or VCCD.
$\overline{\text{TSCB}}$	Output	For PCM backplane operation, $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is active low when PCM data is output on the DXA or DXB pins, respectively. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. $\overline{\text{TSCB}}$ is only available on the 80 pin LQFP package. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{\text{TSCA}}$/G to DGND or VCCD. $\overline{\text{TSCB}}$ is available only on the 80-pin LQFP package.
$VCCA_1$–$VCCA_4$	Supply	+3.3 VDC supplies to the analog sections in each of the four channels.
VCCD	Supply	+3.3 VDC supply to all digital sections.
VHL_1–VHL_4	Output	High-level loop control. Voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each VE790 series ISLIC device.
VIN_1–VIN_4	Input	Analog transmit signals (VTX) from each VE790 series ISLIC device connect to these pins. The Le79228 Quad ISLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU or DXB pin. Tie pin to VREF if channel unused.
$VOUT_1$–$VOUT_4$	Output	Analog receive voltage signals are sent out of the Le79228 Quad ISLAC device from these pins. A resistor converts these signals to currents which drive the VE790 series ISLIC device.
VLB_1–VLB_4	Output	Normally connected to VCCA internally. They supply longitudinal reference voltages to the VE790 series ISLIC devices during certain test procedures. These outputs are connected internally to VCCA during VE790 series ISLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A.
VREF	Output	This pin provides a 1.4-V, single-ended reference to the VE790 series ISLIC devices to which the Le79228 Quad ISLAC device is connected.
$VSAB_1$–$VSAB_4$	Input	Connect to the VSAB pins of four VE790 series ISLIC device channels.
XSB_1–XSB_4	Input	External ringing sense pin. This pin senses the current through R_{SRB} to measure the ringing voltage on the line.
XSC	Input	External ring generator sense. This pin senses the current R_{SRC} to measure the ringing bus voltage.

Pin Options	Package Type	
	80 pin	64 pin
I/O_1–I/O_4	√	x
DRB, DXB, $\overline{\text{TSCB}}$	√	x
DIN/S1	√	x
DOUT	√	x
DIO/S1	x	√
$GS1_1$–$GS1_4$, $GS2_1$–$GS2_4$	√	x

Note: For the 80-pin LQFP package, DOUT and DIN/S1 can be connected together.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–60ºC ≤ T_A ≤ +125ºC
Ambient Temperature, under Bias	–40ºC ≤ T_A ≤ +85ºC
Ambient relative humidity (non condensing)	5 to 95%
V_{CCA} with respect to (AGND or DGND)	–0.4 to + 4.0 V
V_{CCD} with respect to (AGND or DGND)	–0.4 to + 4.0 V
V_{CCA} with respect to V_{CCD}	±0.4V
VIN, VIMT, VILG, VSAB with respect to (AGND or DGND)	–0.4 to (V_{CCA} + 0.4 V)
5-V tolerant pins	–0.4 to (V_{CCD} + 2.37) or 5.5 V, whichever is less
AGND	DGND ± 0.4 V
Latch up immunity, 25ºC (any pin)	±100 mA
Latch up immunity, 85ºC (pin I/O_4)	±50 mA
Latch up immunity, 85ºC (all other pins)	±100 mA
Any other pin with respect to DGND	–0.4 V to V_{CC}

Package Assembly

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Operating Ranges

Legerity guarantees the performance of this device over commercial (0º to 70ºC) and industrial (–40º to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40 to +85ºC
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Analog Supply V_{CCA}	+3.3 V + 5%, - 10%
Digital Supply V_{CCD}	+3.3 V ± 5%
DGND	0 V
AGND	DGND ±10 mV
5-V tolerant pins with respect to DGND	DGND to 5.25V

DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Input Low Voltage, I/O_1–I/O_4		–0.05	—	1.36 V	V	
	All other digital inputs		–0.50	—-	0.80 V		
	Digital input capacitance				4	pF	2.
2	Input High Voltage, I/O_1–I/O_4		2.46	—-	V_{CC}+0.4	V	
	All other digital inputs		2.0	—	5.25		
3	Input Leakage Current, I/O_1–I/O_4	0 to V_{CC}	–10	—-	+10	µA	
	All other digital inputs	0 to 5.25 V	–120	—-	+180		
4	Input hysteresis (PCLK/FS, FS/DCL, MCLK, DIO, DRA, DRB)		0.15	0.225	0.30	V	2.
	Input hysteresis (I/O_1–I/O_4)		0.16	0.25	0.34		
5	Ternary output voltages, LD_1–LD_4					V	
	High voltage	Iout = 1 mA	V_{CC}–.4	—	—		
	Low voltage	Iout = 2 mA	—	—	0.4		
	Medium voltage	±10 µA	—	VREF	—		
6	Output Low Voltage (DXA/DU, DIO, I/O_1–I/O_4, $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$, DXB)	Iol = 10mA	—	—-	0.4	V	
7	Output Low Voltage (P_1-P_3)	Iol = 5 mA	—	—	0.4		
8	Output High Voltage (All digital outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$, $\overline{TSCB}$)	Ioh = 400 µA	V_{CC}–0.4	—	—		
9	Input Leakage Current (VIN_1–VIN_4, $VSAB_1$–$VSAB_4$, $VILG_1$–$VILG_4$, $VIMT_1$–$VIMT_4$, $GS1_1$–$GS1_4$, $GS2_1$–$GS2_4$)		–1	±0.2	1	µA	
10	Full scale input voltage (VIN_1–VIN_4)					V	
	µ-law	3.205 dBm0	—	VREF ±1.02	—		
	A-law	3.14 dBm0					
11	Input Voltage ($VSAB_1$–$VSAB_4$ or $VIMT_1$–$VIMT_4$ or $VILG_1$–$VILG_4$)	|Vov–VREF| where Vov is input overload voltage	—	1.02	—		
12	Offset voltage allowed on VIN_1–VIN_4		–50	—	+50	mV	4.
13	$VOUT_1$–$VOUT_4$ offset Voltage	DISN off	–40	—	+40		
		DISN on	–80	—	+80		
14	VHL_1–VHL_4 D/A absolute error	% of D/A code	–15 -2%		+15 +2%	mV	
15	Output voltage, VREF	Load current = 0 to 10 mA, Source or Sink	1.32	1.4	1.48	V	
16	Capacitance load on VREF and $GS1_1$–$GS1_4$, $GS2_1$–$GS2_4$ or $VOUT_1$–$VOUT_4$		0	—	200	pF	2.
17	Output drive current, $VOUT_1$–$VOUT_4$ or VLB_1–VLB_4	Source or Sink	–1	—	+1	mA	
18	Maximum output voltage, $VOUT_1$–$VOUT_4$	|VOUT–VREF| with peak digital input	—	1.02	—	V	8.
19	VLB_1–VLB_4 operating voltage	Source current < 250µA Sink current < 25 µA.	VREF –1.02	—	VREF +1.02		
20	Maximum output voltage on VHL	|VHL–VREF| with peak digital input, VFD = 0	—	1.02	—		
21	$VSAB_1$–$VSAB_4$, $VIMT_1$–$VIMT_4$, $VILG_1$–$VILG_4$ A/D absolute error	% of input voltage	–5 –2%	—	+5 +2%	mV	9.
22	Battery read A/D absolute error	% of input voltage	–2 –6%	—	+2 +6%	V	9.

No.	Item	Condition	Min	Typ	Max	Unit	Note
23	Gain from $VSAB_1$–$VSAB_4$ to VHL_1–VHL_4 (KRFB)	VFD = 1	–4.8	–5	–5.2	V/V	
24	$VSAB_1$–$VSAB_4$ to VHL_1–VHL_4 output offset (KRFB)		–50	0	50	mV	
25	Gain from $VSAB_1$–$VSAB_4$ to VHL_1–VHL_4	VFD = 0, hook bit feedback	–	–0.128	–	V/V	
26	% error of VLB_1–VLB_4 voltage (For VLB equation, see the *Chip Set User's Guide*)	% of input voltage	–5	0	+5	%	
27	Capacitance load on VLB_1–VLB_4		0	—	120	pF	2.
28	Capacitance load on XSB_1–XSB_4, XSC		0	—	400		
29	Power Dissipation	One channel active (VE790 series ISLIC state register set to active); three channels inactive (VE790 series ISLIC state register set to Standby)	—	183	235	mW	
		All channels active (VE790 series ISLIC state register set to Active)	—	264	340		
		All channels inactive (VE790 series ISLIC state register set to Standby)	—	143	188		

Transmission Specifications

Table 1. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

Signal at Digital Interface	Transmit	Receive	Unit
A-law digital mW or equivalent (0 dBm0)	0.5026	0.5026	Vrms
μ-law digital mW or equivalent (0 dBm0)	0.4987	0.4987	
±5,800 peak linear coded sine wave	0.5026	0.5025	

Note: Expressed voltage levels on VOUT or input to VIN are equivalent to a digital milliwatt on the digital interface.

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Insertion Loss A-D, D-A	Input: 1014Hz, 0dBm0 AR = AX = GR = GX = 0 dB, DISN, R, X, B and Z disabled	–0.25	0	+0.25	dB	3., 7.
	A-D + D-A	Temperature = 25°C	–0.15	0	+0.15		
		Variation over temperature	–0.1	0	+0.1		
2	Level set error (Error between setting and actual value)	A-D AX + GX D-A AR + GR	–0.1	0	0.1		
3	DR to DX gain in full digital loopback mode	DR Input: 1014 Hz, –10 dBm0 AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters default	–0.3	0	+0.3		
4	Idle Channel Noise, Psophometric Weighted (A-law)	A-D (PCM output)	—	—	–69	dBm0p	5.
		D-A (V_{OUT})	—	—	–78		
5	Idle Channel Noise, C Message weighted (µ-law)	A-D (PCM output)	—	—	+19	dBrnC0	
		D-A (V_{OUT})	—	—	+12		
6	Coder Offset decision value, Xn	A-D, Input signal = 0 V	–7	0	+7	Bits	2.
7	PSRR Image frequency (VCC) A-D	Input: 4.8 to 7.8 kHz, 200 mVp-p	37	—	—	dB	1
8	PSRR Image frequency (VCC) D-A	Measure at: 8000 Hz – Input frequency	37	—	—		
9	DISN gain accuracy	Gdisn = –0.9375 to 0.9375 Vin = 0 dBm0		+0.2		dB	
10	End-to-end group delay	1014Hz; –10dBm0 B = Z = 0; X = R = 1	—	—	525	µS	2., 6., 8.
11	Crosstalk TX to RX same channel RX to TX	0 dBm0 300 Hz to 3400 Hz	—	—	–75	dBm0	2.
		0 dBm0 300 Hz to 3400 Hz	—	—			
12	Crosstalk TX or RX to TX other channel TX or RX to RX	0 dBm0 1014 Hz	—	—	–76	dBm0	
		0 dBm0 1014 Hz	—	—	–78		

Notes:

1. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
2. *Guaranteed by design.*
3. *Overall 1.014 kHz insertion loss error of the Le79228 Quad ISLAC device is guaranteed to be 0.34 dB*
4. *These voltages are referred to VREF.*
5. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.*
6. *Group delay spec valid only when Channels 1–4 occupy consecutive slots in the frame. Programming channels in non-consecutive timeslots can add up to 1 frame delay in the Group delay measurements. The Group delay specification is defined as the sum of the minimum values of the group delays for transmit and the receive paths when the B, X, R, and Z filters are disabled with null coefficients. See* Figure 5, on page 16.
7. *Requires that the calibration command (7Ch) must be performed to achieve this performance.*
8. *An additional frame of delay can be added if PCLK frequencies less than 1.536 MHz are used.*
9. *In the absence of any error, the analog level of VREF + 1.02 V represents a digital code of 7FFFh, and the analog level of VREF - 1.02 V represents a digital code of 8000h.*

Transmit and Receive Paths

In this section, the transmit path is defined as the analog input to the Le79228 Quad ISLAC device (VIN_n) to the PCM voice output of the Le79228 Quad ISLAC device A-law/µ-law speech compressor. The receive path is defined as the PCM voice input to the Le79228 Quad ISLAC device speech expander to the analog output of the Le79228 Quad ISLAC device ($VOUT_n$). All limits defined in this section are tested with B = 0, Z = 0 and X = R = GR = 1.

When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.

When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.

These transmission characteristics are valid for 0 to 70° C.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 3 and Figure 4. The reference signal level is –10 dBm0. The minimum transmit attenuation at 60 Hz is 24 dB.

Figure 3. Transmit Path Attenuation vs. Frequency

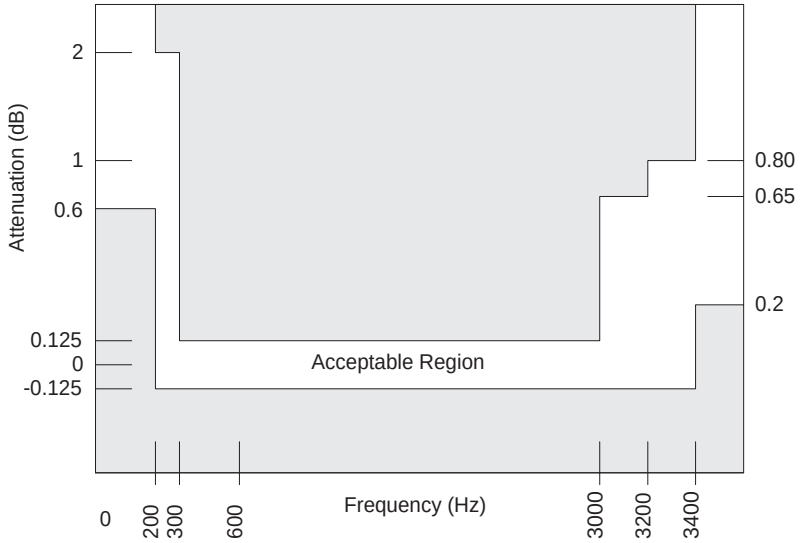
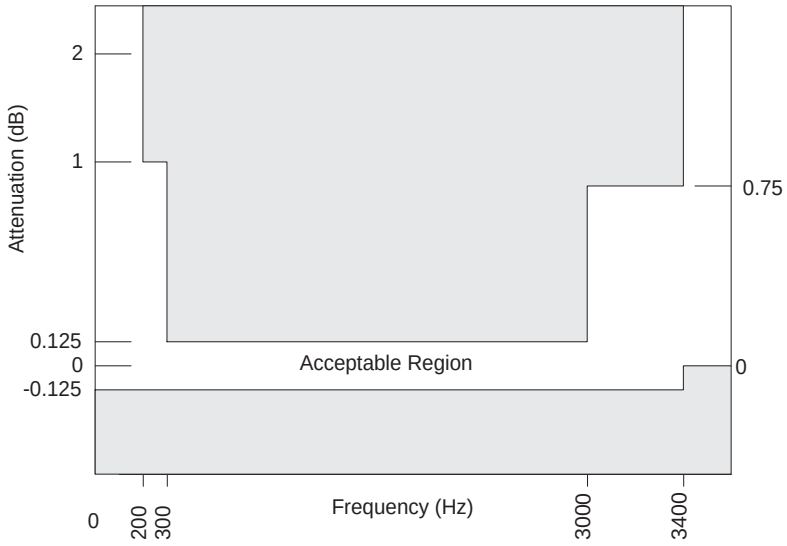


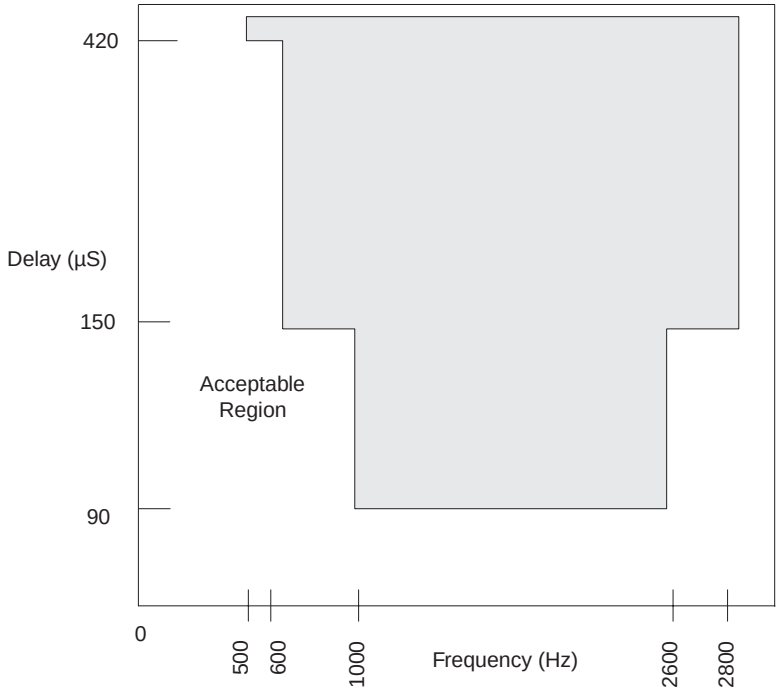
Figure 4. Receive Path Attenuation vs. Frequency



Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 5. The minimum value of the group delay is taken as the reference. The signal level is –10 dBm0.

Figure 5. Group Delay Distortion



Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 6 (A-law) and Figure 7 (μ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

Figure 6. A-law Gain Linearity with Tone Input (Both Paths)

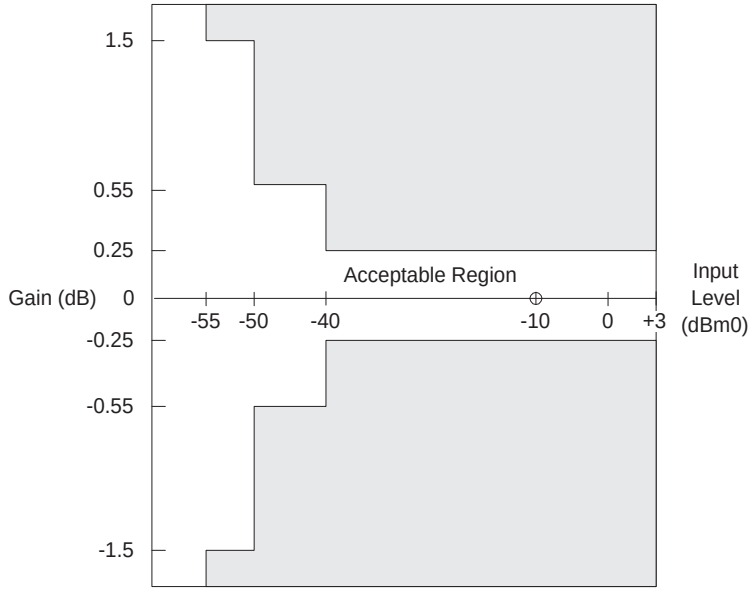
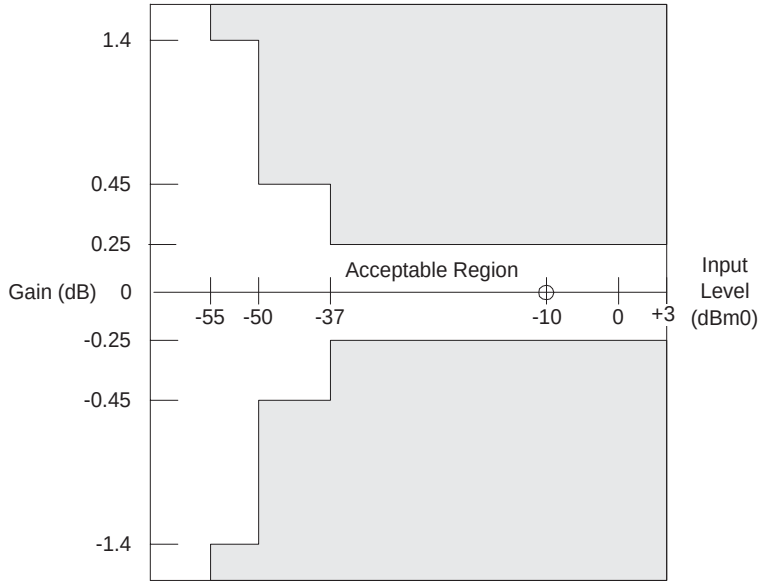


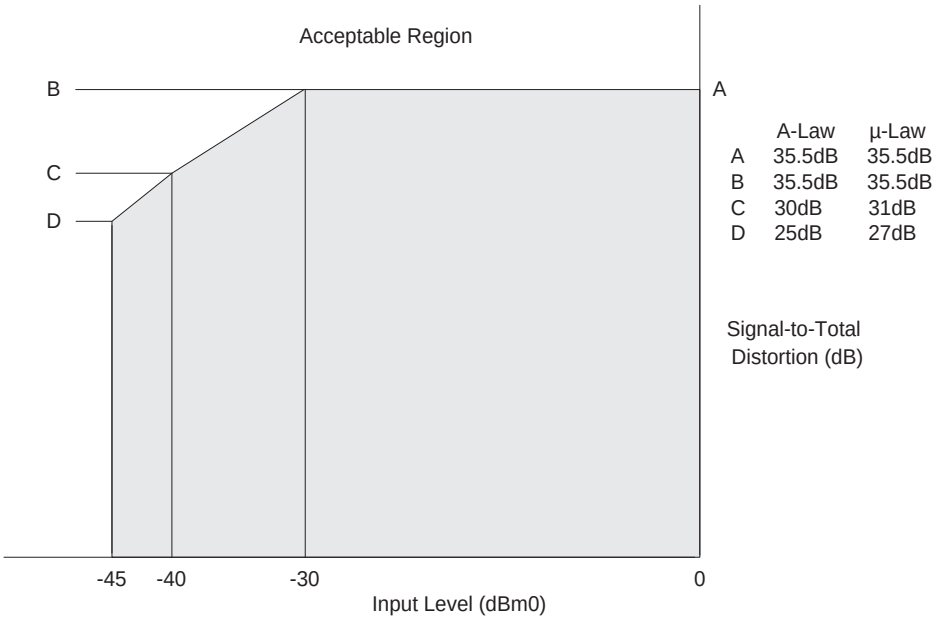
Figure 7. μ-law Gain Linearity with Tone Input (Both Paths)



Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 8 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Figure 8. Total Distortion with Tone Input, Both Paths

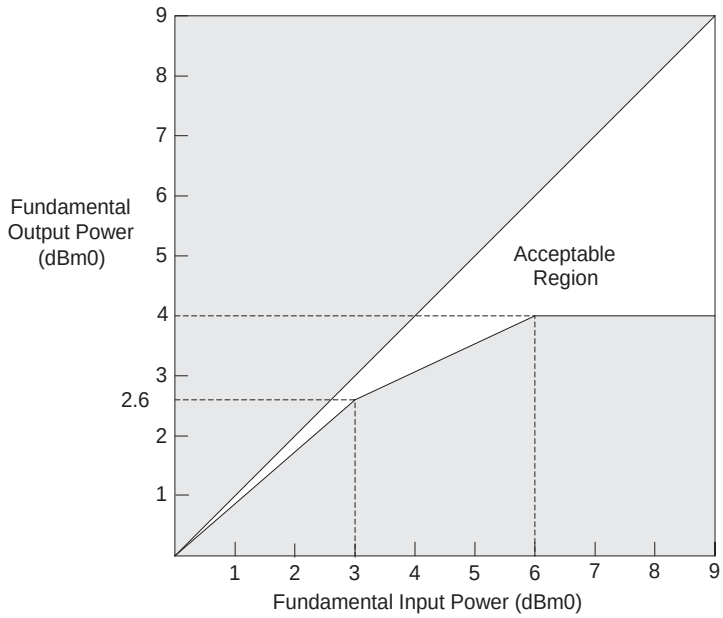


Overload Compression

Figure 9 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) 1 dB < GX ≤ +12 dB; (2) –12 dB ≤ GR < –1 dB; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

Figure 9. A/A Overload Compression



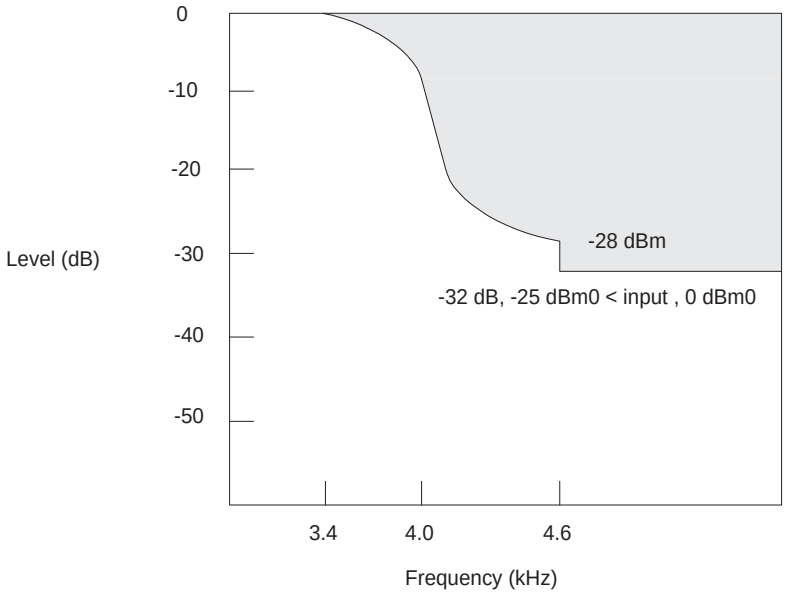
Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table

Table 2. Minimum Specifications for Out-of-Band Input Signals

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 10
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB

Figure 10. Discrimination Against Out-of-Band Signals



Note:

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (db)} = 14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)$$

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

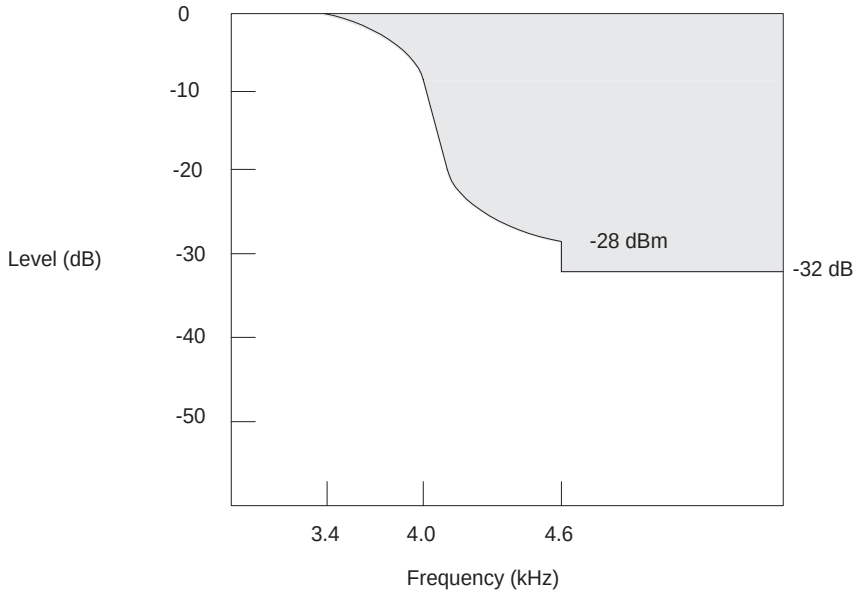
Table 3. Limits for Spurious Out-of-Band Signals

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 11. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

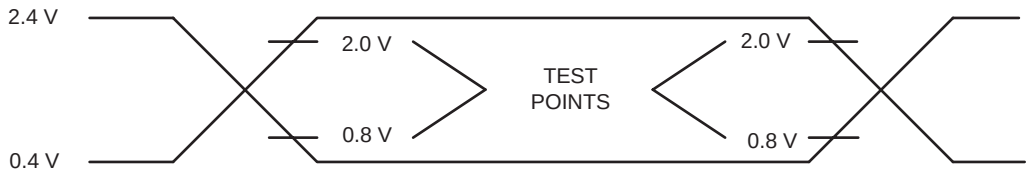
$$A = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

Figure 11. Spurious Out-of-Band Signals



SWITCHING CHARACTERISTICS

Figure 12. Switching Characteristics



VCC = 3.3 V ±5%, AGND = DGND = 0 V.

Microprocessor Interface

Min and max values are valid for all digital outputs with a 150 pF load. Pictorial definitions for these parameters can be found in Figure 14, on page 23 and Figure 15, on page 24.

No.	Symbol	Parameter	Min	Typ	Max	Unit	Note
1	t_{DCY}	Data clock period	122	—	—	ns	
2	t_{DCH}	Data clock HIGH pulse width	48	—	—		1.
3	t_{DCL}	Data clock LOW pulse width	48	—	—		1.
4	t_{DCR}	Rise time of clock	—	—	25		
5	t_{DCF}	Fall time of clock	—	—	25		
6	t_{ICSS}	Chip select setup time, Input mode	30	—	t_{DCY}–10		
7	t_{ICSH}	Chip select hold time, Input mode	0	—	t_{DCY}–20		
8	t_{ICSL}	Chip select pulse width, Input mode	—	$8t_{DCY}$	—		7.
9	t_{ICSO}	Chip select off time, Input mode	2000	—	—		1., 6.
10	t_{IDS}	Input data setup time	25	—	t_{DCY}–10		
11	t_{IDH}	Input data hold time	30	—	t_{DCY}–10		
13	t_{OCSS}	Chip select setup time, Output mode	30	—	t_{DCY}–10		
14	t_{OCSH}	Chip select hold time, Output mode	0	—	t_{DCH}–20		
15	t_{OCSL}	Chip select pulse width, Output mode	—	$8t_{DCY}$	—		
16	t_{OCSO}	Chip select off time, output Mode	2000	—	—		1., 6.
17	t_{ODD}	Output data turn on delay	—	—	35		5.
18	t_{ODH}	Output data hold time	3	—	—		
19	t_{ODOF}	Output data turn off delay	3	—	35		
20	t_{ODC}	Output data valid	3	—	35		

PCM Interface

Min and max values are valid for $\overline{TSCA}$ and $\overline{TSCB}$ with an 150 pF load and are valid for DXA and DXB with an 80 pF load. Pictorial definitions for these parameters can be found on Figure 16, on page 24 and Figure 17, on page 25.

No.	Symbol	Parameter	Min.	Typ	Max	Unit	Note
22	t_{PCY}	PCM clock period	122	—	7812.5	ns	2., 9.
23	t_{PCH}	PCM clock HIGH pulse width	48	—	—		
24	t_{PCL}	PCM clock LOW pulse width	48	—	—		
25	t_{PCF}	Fall time of clock	—	—	15		
26	t_{PCR}	Rise time of clock	—	—	15		
27	t_{FSS}	FS setup time	30	—	t_{PCY}–30		
28	t_{FSH}	FS hold time	50	—	125000-$3t_{PCY}$-30		
29	t_{TSD}	Delay to $\overline{TSCX}$ valid	5	—	40		3.
30	t_{TSO}	Delay to $\overline{TSCX}$ off	5	—	40		4.
31	t_{DXD}	PCM data output delay	5	—	40		
32	t_{DXH}	PCM data output hold time	5	—	40		
33	t_{DXZ}	PCM data output delay to high-Z	10	—	40		4.
34	t_{DRS}	PCM data input setup time	25	—	t_{PCY}–10		
35	t_{DRH}	PCM data input hold time	5	—	t_{PCY}–20		
36	t_{FST}	PCM or frame sync jitter time	–97	—	97		

Master Clock

Master Clock can be sourced by MCLK or PCLK input by appropriate configuration of DCRI (see Figure 13). For a 2.048 mHz ± 100 PPM, 4.096 mHz ± 100 PPM, or 8.192 ± 100 PPM operation:

No.	Symbol	Parameter	Min	Typ	Max	Unit	No
37	t_{MCY}	Period	122	—	7812	ns	2., 8., 9.
38	t_{MCR}	Rise time of clock	—	—	15		
39	t_{MCF}	Fall time of clock	—	—	15		
40	t_{MCH}	Master Clock HIGH pulse width	48	—	—		
41	t_{MCL}	Master Clock LOW pulse width	48	—	—		

Note:

1. *DCLK may be stopped in the High or Low state indefinitely without loss of information. When $\overline{CS}$ makes a transition to the High state, the last byte received will be interpreted by the Microprocessor Interface logic.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency and synchronous to the MCLK frequency. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 mHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz.*
3. *$\overline{TSCX}$ is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time/clock slot register.*
4. *$\overline{TSCX}$ is an open drain driver. t_{TSO} is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCX}$ is 150 pF and the minimum pull-up resistance is 360 Ω.*
5. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
6. *The Le79228 Quad ISLAC device requires 2.0 µs between MPI operations. If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 µs is required when accessing coefficient RAM. Immediately after reset, $t_{ICSO} = \frac{2\mu s \cdot 8.192\ MHz}{f_{PCLK}}$, where f_{PCLK} is the applied PCLK frequency. Once DCR1 is programmed for the applied PCLK and MCLK, t_{ICSO} is per table specification.*
7. *If chip select is held low for 16 or more DCLK cycles, the part will reset.*
8. *Master Clock's frequency can range from 512 kHz to 8.192 MHz and can be set with: Write/Read Device Configuration Register 1, and if necessary Write/Read Master Clock Correction Register.*
9. *If PCLK is greater or equal to 512 kHz, the preferred configuration is Master Clock derived from PCLK. If a separate MCLK is used, it must be synchronous to PCLK. If PCLK is less than 512 kHz, a separate MCLK (synchronous with PCLK) with f_0 greater or equal to 512 kHz must be used.*

WAVEFORMS

Figure 13. Master Clock Timing

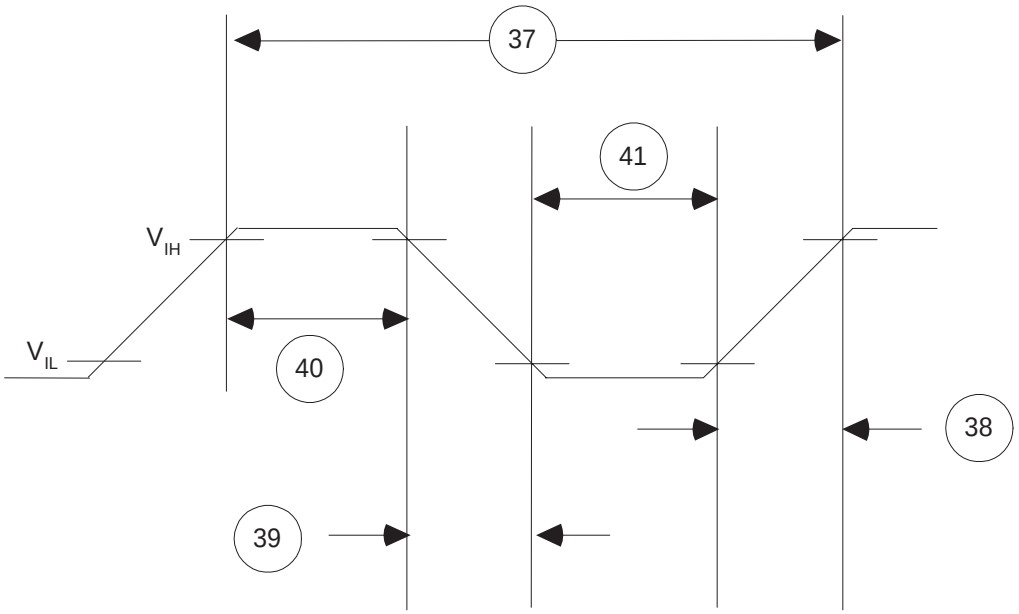


Figure 14. Microprocessor Interface (Input Mode)

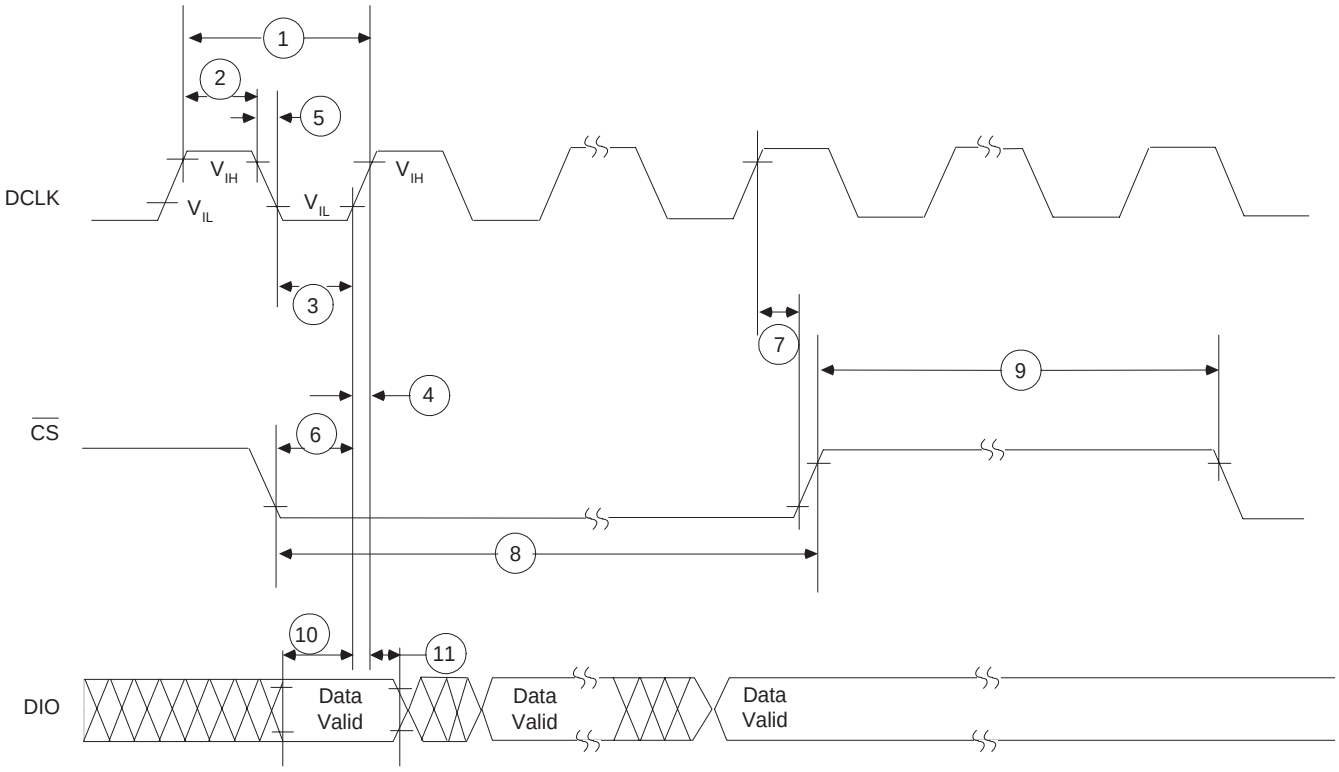


Figure 15. Microprocessor Interface (Output Mode)

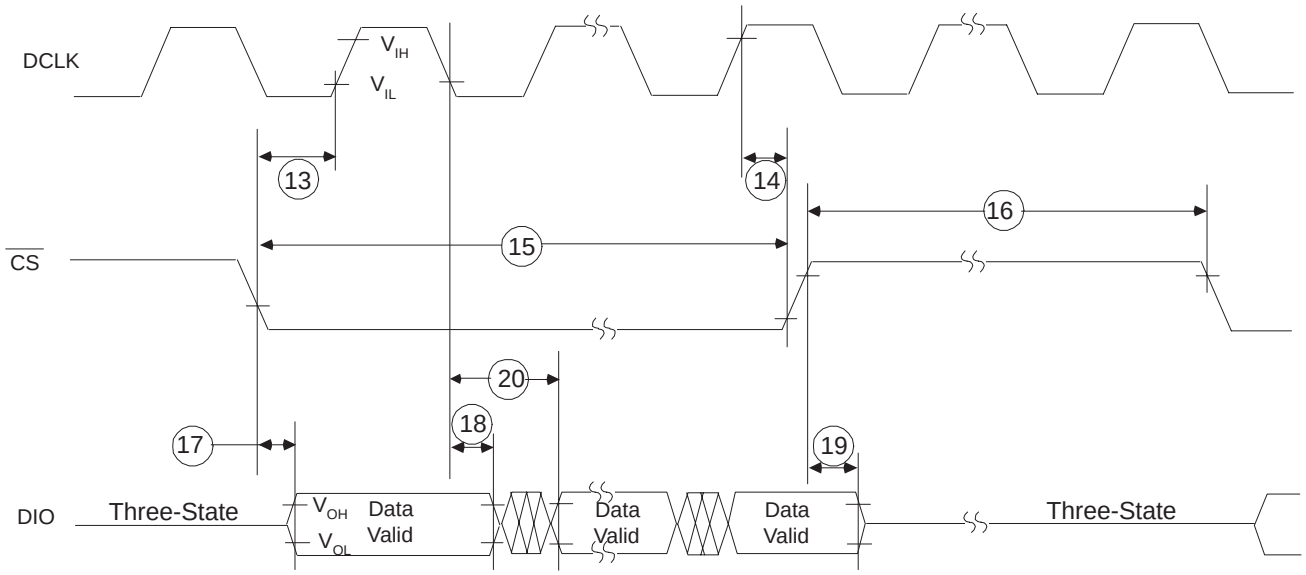


Figure 16. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)

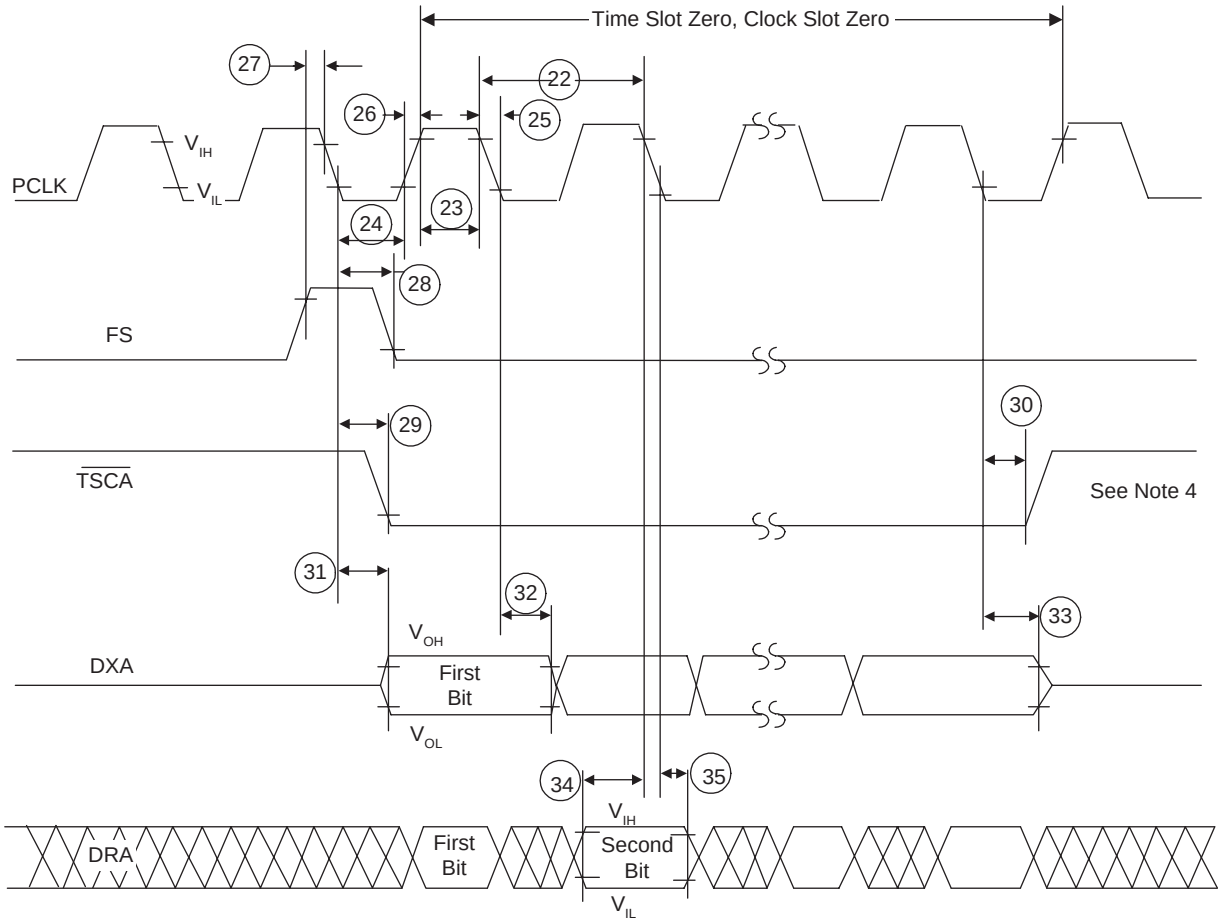
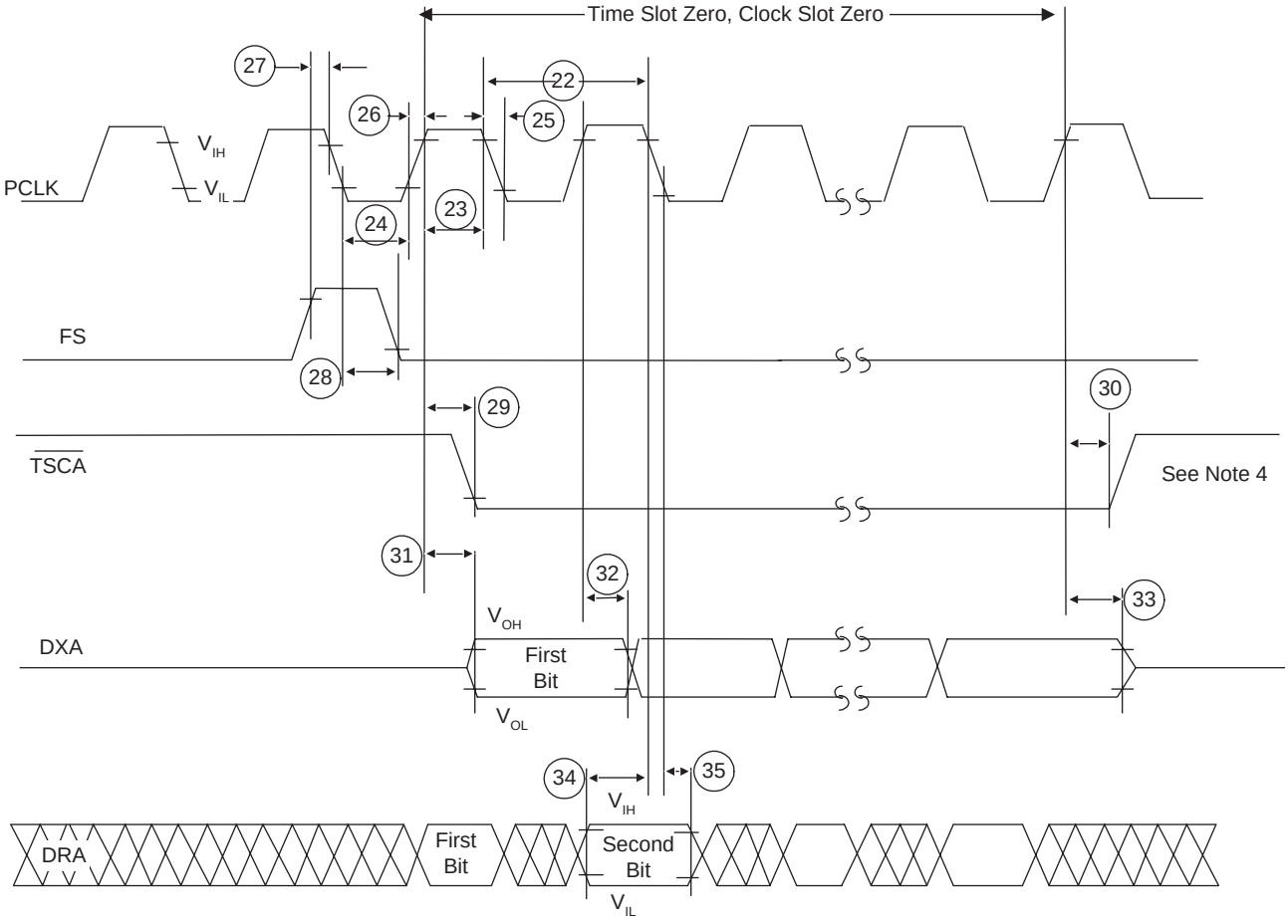


Figure 17. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

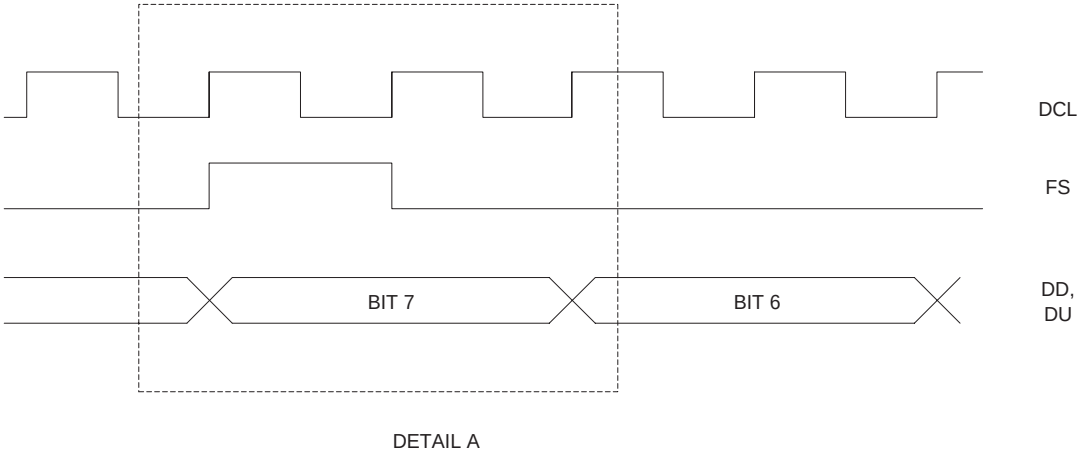


GCI Timing Specifications

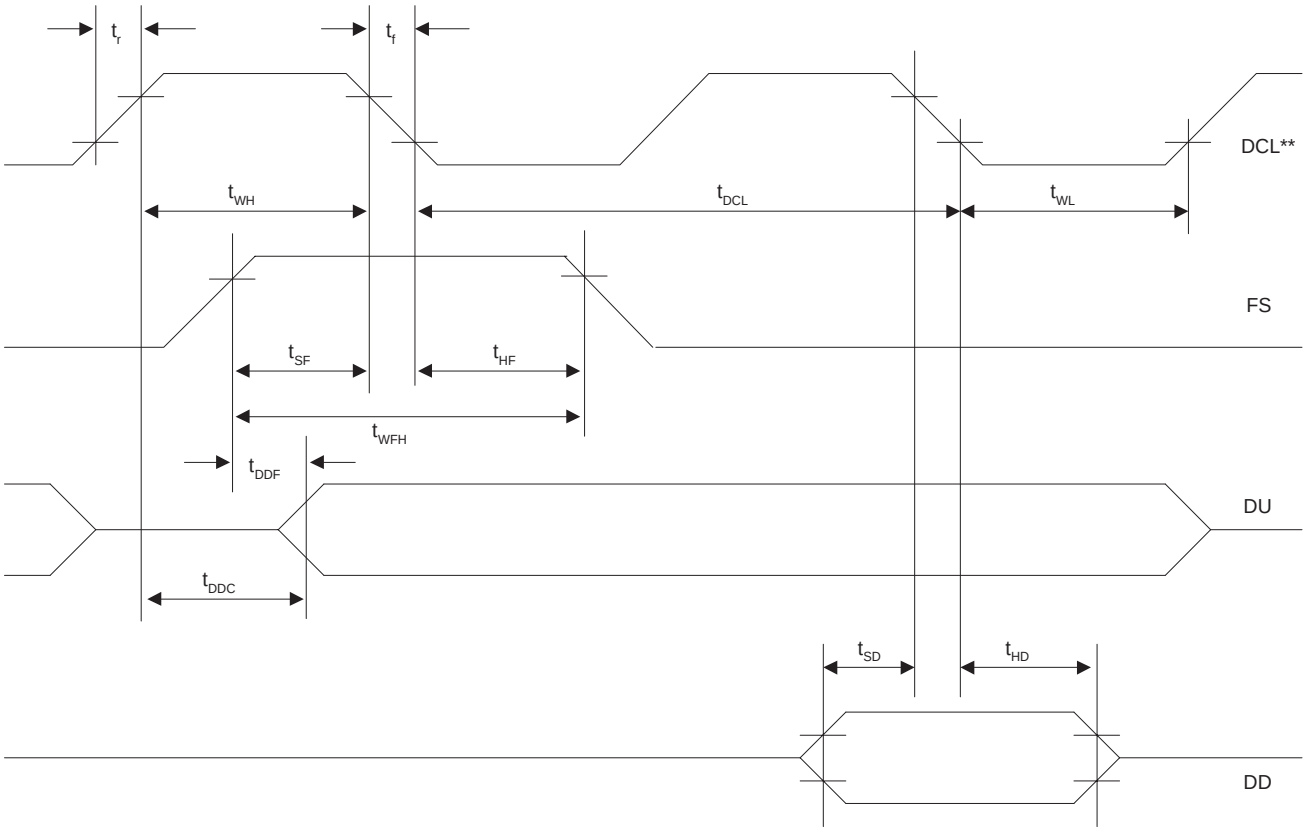
For a 2.048 mHz ± 100 PPM, 4.096 mHz ± 100 PPM, or 8.192 ± 100 PPM operation:

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_R, t_F	DCL	Rise/fall time	—	—	60	ns
t_{DCL}	DCL	Period, F_{DCL} = 2048 kHz F_{DCL} = 4096 kHz	478 239	—	498 249	
t_{WH}, t_{WL}	DCL	Pulse width	90	—	—	
t_R, t_F	FS	Rise/fall time	—	—	60	
t_{SF}	FS	Setup time	70	—	t_{DCL}–50	
t_{HF}	FS	Hold time	50	—	—	
t_{WFH}	FS	High pulse width	130	—	—	
t_{DDC}	DU	Delay from DCL edge	—	—	100	
t_{DDF}	DU	Delay from FS edge	—	—	150	
t_{SD}	DD	Data setup	20	—	—	
t_{HD}	DD	Data hold	50	—	—	

GCI Waveforms



DETAIL A



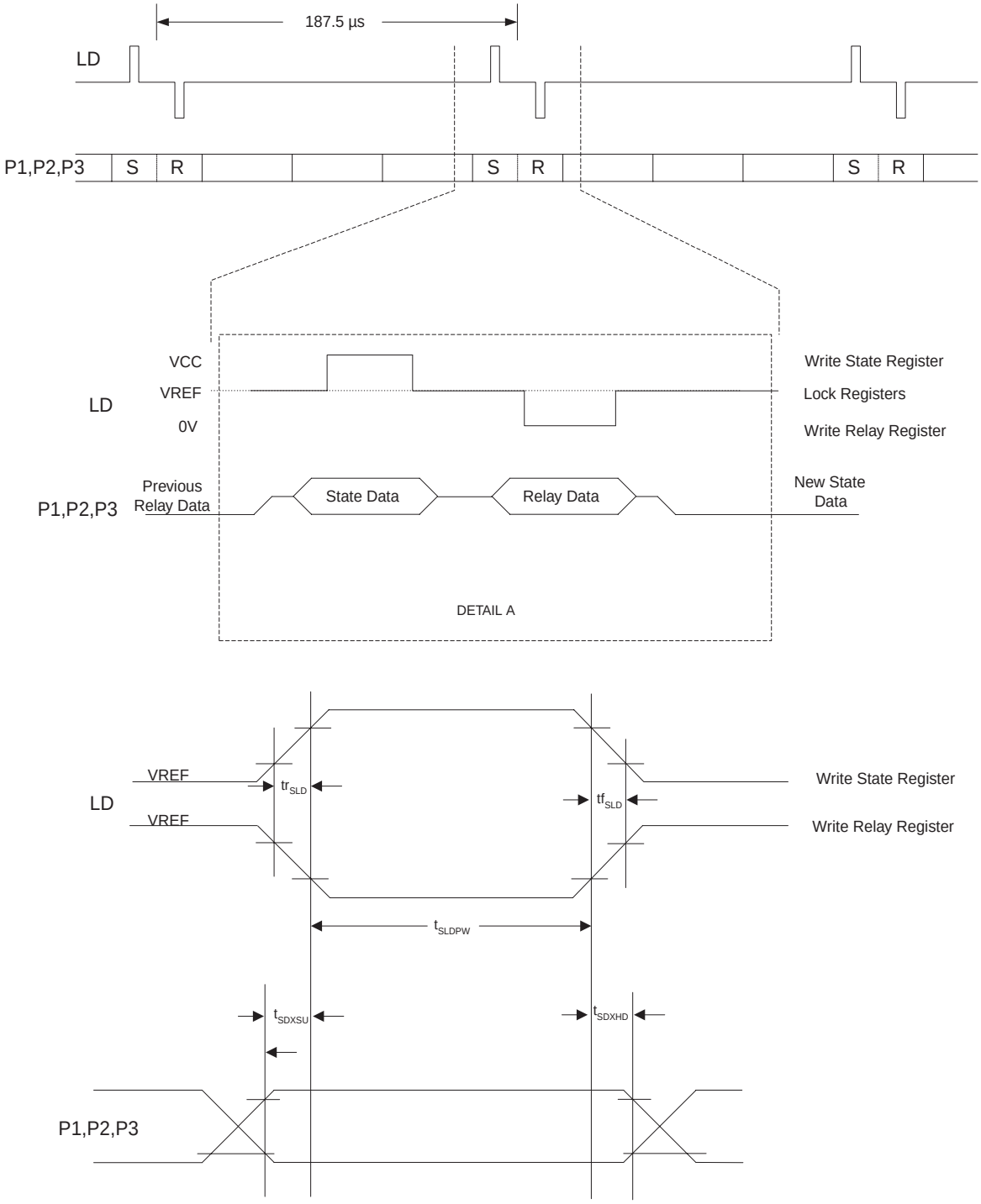
** Timing diagram valid for
F_{DCL} = 2048 or 4096 KHz

ISLIC DEVICE TIMING SPECIFICATIONS

(See Figure 18.)

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tr_{SLD}	LD	Rise time			2	µs
tf_{SLD}	LD	Fall time			2	
t_{SLDPW}	LD	LD minimum pulse width	3			
t_{SDXSU}	P1,P2,P3	P1–3 data Setup time	4.5			
t_{SDXHD}	P1,P2,P3	P1–3 data hold time	4.5			

Figure 18. ISLIC Device Bus Timing Waveform



APPLICATION CIRCUITS

Figure 19. Internal Ringing Line Schematic

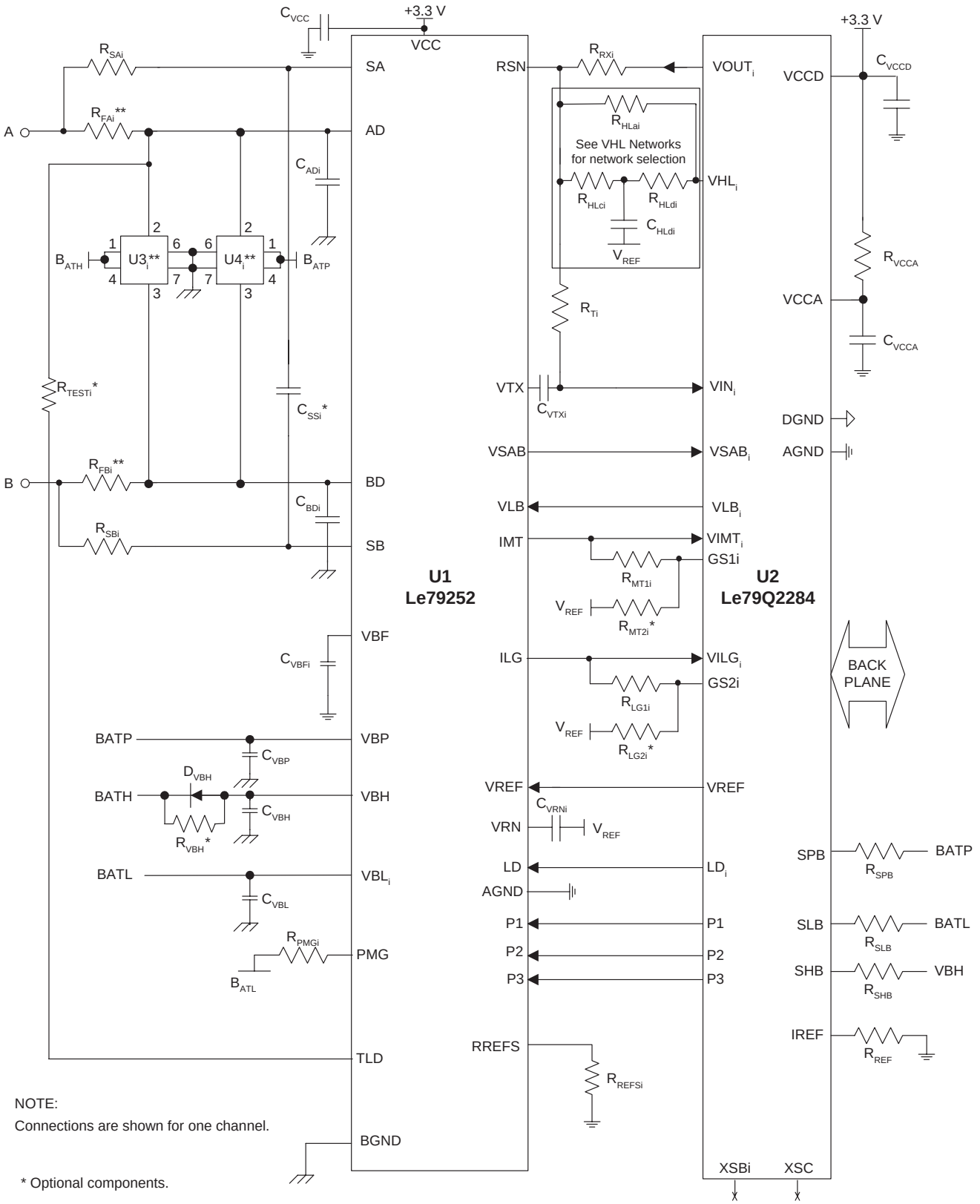
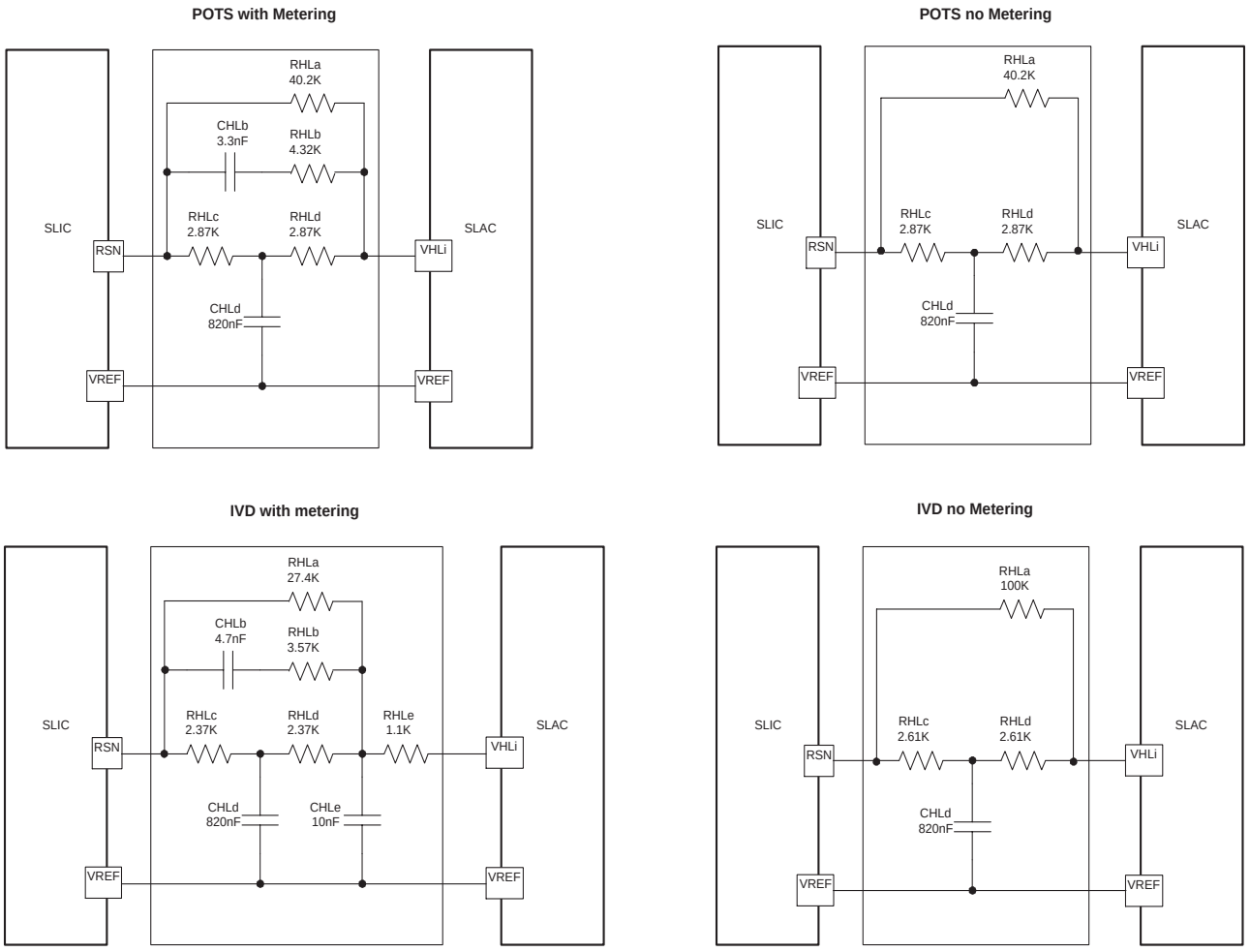


Figure 20. VHL networks for POTS and IVD Applications with and without Metering



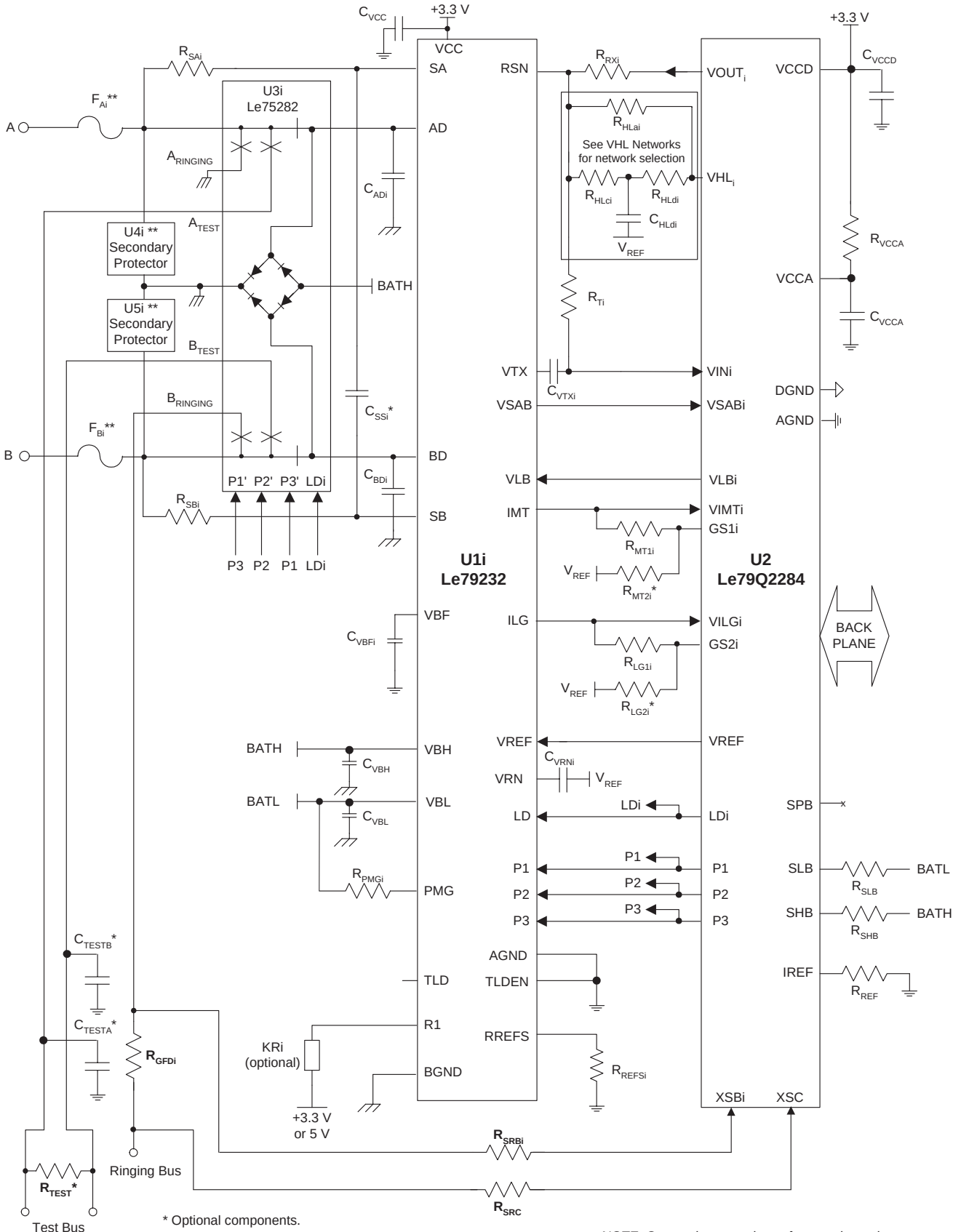
LINE CARD PARTS LIST- INTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2,3,4 or i = 1,2).

Item	Type	Value	Tol.	Rating	Comments	Optional Components
$U1_i$	Le79252 device				Dual ISLIC device	
U2	Le79228x				ISLAC device	
U3i	TISP8200M				Bourns® Negative Overvoltage Protector	
U4i	TISP8201M				Bourns® Positive Overvoltage Protector	
D_{VBH}	Diode	100 mA		100 V		
R_{VBH}	Resistor	1 kΩ	5%	1/16 W		Required if VoiceEdge Control Processor (VCP) is not used and R_{FAi}, R_{FBi} are PTC components and R_{SAi}, R_{SBi} sense resistors are wired as shown in Figure 3
R_{FAi}, R_{FBi}	Resistor	50 Ω	2%	2 W	Fusible resistors or PTC protection resistors	
R_{SAi}, R_{SBi}	Resistor	200 kΩ	1%	3/4 W	Sense resistors, pulse withstanding component	
R_{Ti}	Resistor	80.6 kΩ	1%	1/16 W	Impedance control resistor	
R_{RXi}	Resistor	90.9 kΩ	1%	1/16 W	Receive path gain resistor	
C_{VTXi}	Capacitor	100 nF	10%	50 V		
R_{REF}	Resistor	69.8 kΩ	1%	1/16 W	Current reference setting resistor	
R_{SHB}, R_{SLB}, R_{SPB}	Resistor	750 kΩ	1%	1/16 W	Battery sense resistors	
R_{HLai}	Resistor	40.2 kΩ	1%	1/16 W	Feed resistor, see VHL networks for IVD value	
R_{HLbi}	Resistor	4.32 kΩ	1%	1/16 W	Metering resistor	Required for metering
R_{HLci}, R_{HLdi}	Resistor	2.87 kΩ	1%	1/16 W	Feed resistors, see VHL networks for IVD values	
C_{HLbi}	Capacitor	3.3 nF	10%	10 V	Metering capacitor - Not Polarized	Required for metering
C_{HLdi}	Capacitor	0.82 µF	10%	10 V	Feed capacitor -Ceramic	
C_{SSi}	Capacitor	33 or 56 pF	5%	100 V	Metering capacitor -Ceramic, use 33 pF for 3.2 Vrms max. or 56 pF for 5.0 Vrms max. metering.	Only required for metering > 2.2 Vrms, otherwise omit
R_{MT1i}	Resistor	3.01 kΩ	1%	1/16 W	Metallic loop current gain resistor	
R_{MT2i}	Resistor	75 kΩ	1%	1/16 W	Metallic loop current resistor for high gain selection	Required for testing, tie RMT1i to VREF if not used
R_{LG1i}	Resistor	6.04 kΩ	1%	1/16 W	Longitudinal loop current gain resistor	
R_{LG2i}	Resistor	150 kΩ	1%	1/16 W	Longitudinal loop current resistor for high gain selection	Required for testing, tie RLG1i to VREF if not used
R_{REFSi}	Resistor	56.2 kΩ	1%	1/16 W		
R_{PMGi}	Resistor	510Ω	5%	1 W	Value should be adjusted to suit application	
R_{TESTi}	Resistor	2 kΩ	1%	1 W	Test load	Optional for testing
C_{ADi}, C_{BDi}	Capacitor	15 nF	10%	200 V	Ceramic, X7R dielectric	
C_{VBH}, C_{VBL}, C_{VBP}	Capacitor	100 nF	20%	100 V	Ceramic	
C_{VBFi}	Capacitor	1 nF	20%	100 V	Ceramic	
C_{VCC}	Capacitor	100 nF	20%	10 V		

C_{VCCD}	Capacitor	100 nF	20%	10 V		
C_{VCCA}	Capacitor	33 µF	20%	6.3 V	Tantalum	
R_{VCCA}	Resistor	3.3 Ω	1%	1/16 W		
C_{VRNi}	Capacitor	100 nF	20%	10 V		

Figure 21. External Ringing Line Schematic



* Optional components.

** Consult Legerity for an optimized protection recommendation.

NOTE: Connections are shown for one channel.

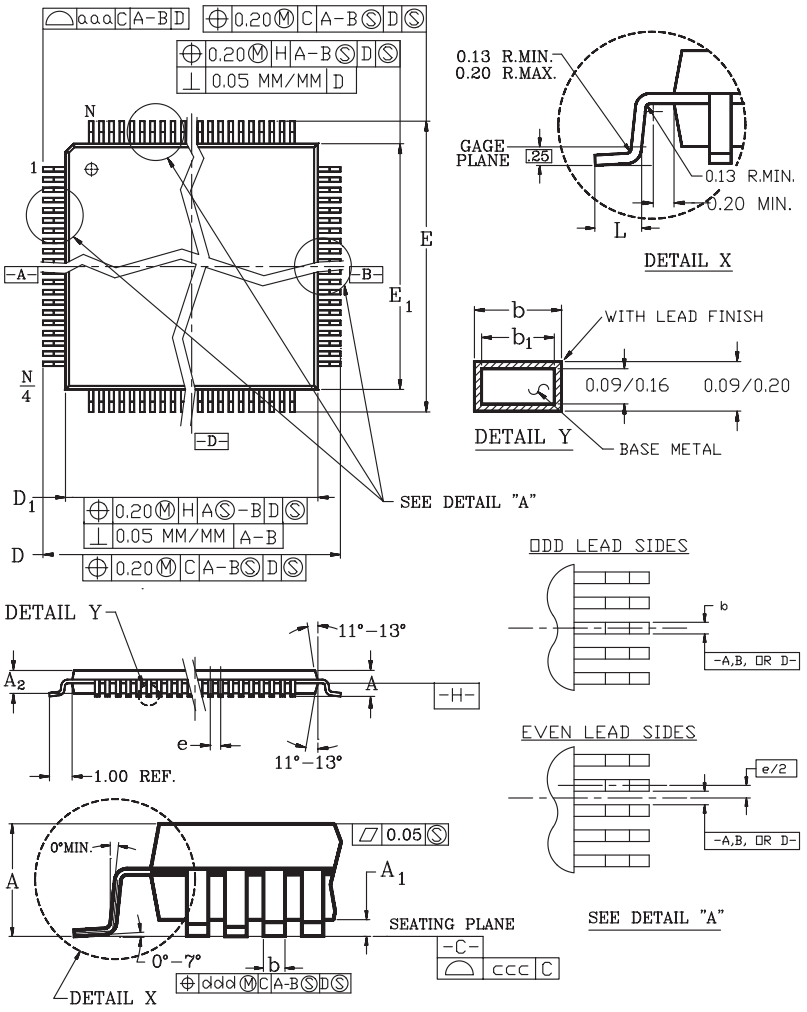
LINE CARD PARTS LIST - EXTERNAL RINGING

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2,3,4 or i = 1,2).

Item	Type	Value	Tol.	Rating	Comments	Optional Components
$U1_i$	Le79232 device				Dual ISLIC device	
U2	Le79228x				ISLAC device	
$U3_i$	Le75282				LCAS device	
$U4_i$	TISP4125H3	±125 V			Bourns® Overvoltage Protector or equivalent	
$U5_i$	TISP4A250H3	+125 V, -250 V			Bourns® Asymmetrical Overvoltage Protector or equivalent	
F_{Ai}, F_{Bi}	B1250T	1.25 A		600 V	Bourns® Fuse	
R_{SAi}, R_{SBi}	Resistor	200 kΩ	1%	1/2 W	Sense resistors, pulse withstanding component	
R_{Ti}	Resistor	80.6 kΩ	1%	1/16 W	Impedance control resistor	
R_{RXi}	Resistor	90.9 kΩ	1%	1/16 W	Receive path gain resistor	
C_{VTXi}	Capacitor	100 nF	10%	50 V		
R_{REF}	Resistor	69.8 kΩ	1%	1/16 W	Current reference setting resistor	
R_{SHB}, R_{SLB}	Resistor	750 kΩ	1%	1/16 W	Battery sense resistors	
R_{HLai}	Resistor	40.2 kΩ	1%	1/16 W	Feed resistor, see VHL networks for IVD value	
R_{HLbi}	Resistor	4.32 kΩ	1%	1/16 W	Metering resistor	Required for metering
R_{HLci}, R_{HLdi}	Resistor	2.87 kΩ	1%	1/16W	Feed resistors, see VHL networks for IVD values	
C_{HLbi}	Capacitor	3.3 nF	10%	10 V	Metering capacitor - Not Polarized	Required for metering
C_{HLdi}	Capacitor	0.82 µF	10%	10 V	Feed capacitor -Ceramic	
C_{SSi}	Capacitor	33 or 56 pF	5%	100 V	Metering capacitor -Ceramic, use 33 pF for 3.2 Vrms max. or 56 pF for 5.0 Vrms max. metering.	Only required for metering > 2.2 Vrms, otherwise omit
R_{MT1i}	Resistor	3.01 kΩ	1%	1/16 W	Metallic loop current gain resistor	
R_{MT2i}	Resistor	75 kΩ	1%	1/16 W	Metallic loop current resistor for high gain selection	Required for testing, tie RMT1i to VREF if not used
R_{LG1i}	Resistor	6.04 kΩ	1%	1/16 W	Longitudinal loop current gain resistor	
R_{LG2i}	Resistor	150 kΩ	1%	1/16 W	Longitudinal loop current resistor for high gain selection	Required for testing, tie RLG1i to VREF if not used
R_{REFSi}	Resistor	56.2 kΩ	1%	1/16 W		
R_{PMGi}	Resistor	510Ω	5%	1 W	Value should be adjusted to suit application	
$R_{TEST(i)}$	Resistor	2 kΩ	1%	1 W	Test load, power rating assumes intermittent operation per test algorithms	Optional for testing
C_{TESTA}, C_{TESTB}	Capacitor	1 nF	20%	100 V	Test bus capacitors	Refer to Le75282 data sheet for applicability
C_{ADi}, C_{BDi}	Capacitor	15 nF	10%	200 V	Ceramic, X7R dielectric	
C_{VBH}, C_{VBL}	Capacitor	100 nF	20%	100 V	Ceramic	
C_{VBFi}	Capacitor	1 nF	20%	100 V	Ceramic	
C_{VCC}	Capacitor	100 nF	20%	10 V		
C_{VCCD}	Capacitor	100 nF	20%	10 V		
C_{VCCA}	Capacitor	33 µF	20%	6.3 V	Tantalum	
R_{VCCA}	Resistor	3.3 Ω	1%	1/16 W		
C_{VRNi}	Capacitor	100 nF	20%	10 V		

R_{GFDi}	Resistor	511 Ω	2%	2 W	Ringing feed resistor, wirewound or surge rated	
R_{SRBi}, R_{SRC}	Resistor	750 kΩ	1%	1/4 W	Sense resistor, if EMR used for ringing, then use a pulse withstanding component	

PHYSICAL DIMENSIONS
64-Pin Thin Quad Flat Pack (TQFP)



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D	12 BSC		
D1	10 BSC		
E	12 BSC		
E1	10 BSC		
L	0.45	0.60	0.75
N	64		
e	0.50 BSC		
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
ccc	0.08		
ddd	0.08		
aaa	0.20		

JEDEC #: MS-026 (C) ACD

Notes:
1. All dimensions and toleerances conform to ANSI Y14.5-1982.
2. Datum plane -H- is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.
3. Dimensions “D1” and “E1” do not include mold protrusion. Allowable protrusion is 0.254mm per side. Dimensions “D1” and “E1” include mold mismatch and are determined at Datum plane -H- .
4. Dimension “B” does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the “b” dimension at maximum material condition. Dambar can not be located on the lower radius or the foot.
5. Controlling dimensions: Millimeter.
6. Dimensions “D” and “E” are measured from both innermost and outermost points.
7. Deviation from lead-tip true position shall be within ±0.076mm for pitch >0.5mm and within ±0.04 for pitch ≤0.5mm.
8. Lead coplanarity shall be within: (Refer to 06-500)
   1- 0.10mm for devices with lead pitch of 0.65-0.80mm.
   2- 0.076mm for devices with lead pitch of 0.50mm.
   Coplanarity is measured per specification 06-500.
9. Half span (center of package to lead tip) shall be 15.30 ± 0.165mm {.602”±.0065”}.
10. “N” is the total number of terminals.
11. The top of package is smaller than the bottom of the package by 0.15mm.
12. This outline conforms to Jedec publication 95 registration MS-026
13. The 160 lead is a compliant depopulation of the 176 lead MS-026 variation BGA.

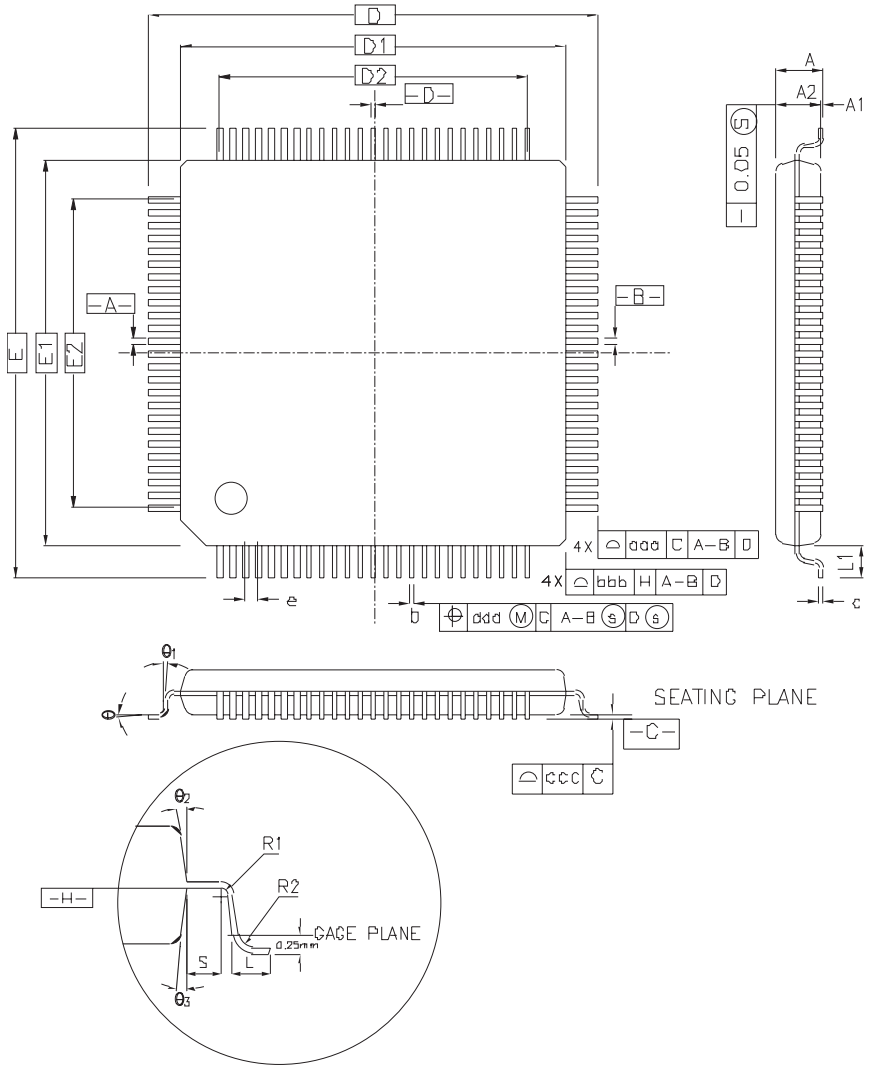
64-Pin TQFP

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

80-Pin Low-Profile Quad Flat Pack (LQFP)

80LD 12x12x1.4 mm LQFP
Package Outline Drawing



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

NOTE (OPTION):

SQUARE DOTTED LINE IS E-PAD OUTLINE.
SIZE IS DEPENDENT ON DIE ATTACH PAD.

	80L					
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.

2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.

   Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- Removed all references to 68-pin PLCC package.
- Added GS1x and GS2x pins to Le792283.
- Changed min/typ/max values in "Gain from VSAB to VHL" under DC Specifications from positive to negative.
- Combined gain/offset errors; made other minor formatting corrections.
- Updated Application Circuits and Parts Lists.
- Updated Related Literature.

Revision B1 to C1

- Changed Le79Q2283VC to Le79Q2284VC.
- Minor text and drawing changes.

Revision C1 to D1

- Changed OPN to reflect green package.
- Added *Package Assembly*, on page 11.
- In *Pin Descriptions*, on page 9, Pin Name I/O, removed TTL-compatible;Pin Name SHB, SLB, SPB, enhanced Description.
- In *Electrical Ranges*, on page 11, changed VCCA acceptable operating tolerance from -5% to -10%.
- In *DC Specifications*, 2, Input High Voltage Min tightened from 2.36 V to 2.46 V; 14, 21, 22, 26 Conditions added.
- In *Transmission Specifications*, 1, Conditions modified and Min and Max specifications tightened from ±0.34 dB to ±0.25 dB; 9, Min and Max requirements removed.
- *GCI Timing Specifications*, on page 25, t_{SD} Min time changed from t_{WH}+20 ns to 20 ns.
- Updated Application drawings and BOMs.

Revision D1 to E1

- Added "Packing" column and Note 2 to *Ordering Information*, on page 1; removed non-green package options
- Document updated from Preliminary Data Sheet to Final Data Sheet.
- Device Internal Block Diagram revised to 80-pin TQFP.
- Modified *Pin Descriptions*, on page 9 to identify pins that are package dependent.
- In *DC Specifications*, on page 12, No 1, added Digital input capacitance specification.
- In *Microprocessor Interface*, on page 21, No. 4,5 rise/fall times, changed max from 15 to 25 ns, No. 17, 19, 20 output parameters, changed max from 50 to 35 ns.
- Updated Application Circuits, VHL Networks, and Line Card Parts List.
- Minor text and table changes.

Revision E1 to F1

- Changed Le792284 OPN from Le79Q2284FVC to Le79Q2284MVC to reflect package change from TQFP to LQFP.
- Minor edit to schematics.
- Line Card Parts List - External Ringing, changed U4i from 95 V TISP4095H3 protector to 250 V TISP4250H3 protector.
- Physical Dimensions, replaced 80-pin TQFP with 80-pin LQFP.

Revision F1 to G1

- Page 21, PCM Interface, output loading added. DXA and DXB loading changed from 150 pF to 80 pF.
- Updated Figure 19, on page 28.
- Updated Figure 21, on page 32.
- Updated *Line card Parts List- INTERNAL RINGING*, on page 30.
- Updated *Line card Parts List - EXTERNAL RINGING*, on page 33.

Revision G1 to G2

- Enhanced format of package drawings in *Physical Dimensions*, on page 35
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at:

www.zarlink.com