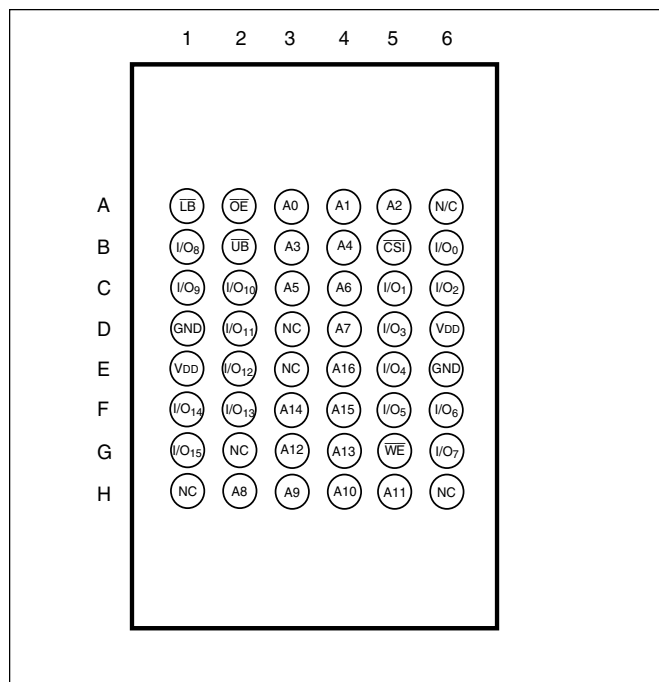
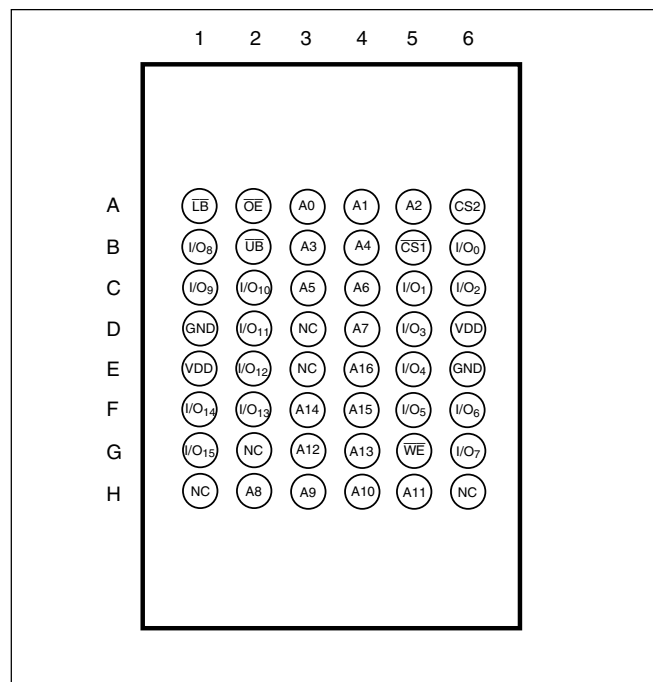
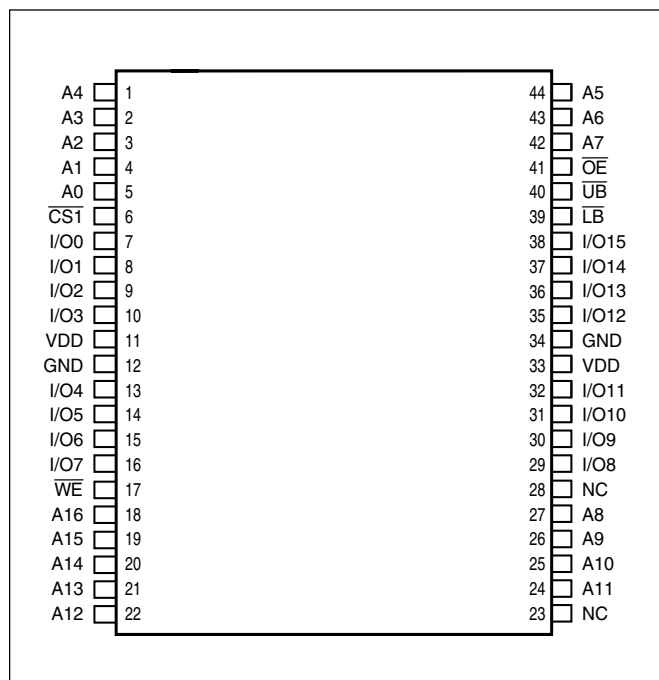


PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)
(Package Code B)48-Pin mini BGA (6mm x 8mm)
2 CS Option (Package Code B2)44-Pin mini TSOP (Type II)
(Package Code T)

PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V_{DD} Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	L	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	X	X	H	H	High-Z	High-Z	ISB1, ISB2
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I _{CC}
	H	L	H	H	X	L	High-Z	High-Z	I _{CC}
Read	H	L	H	L	L	H	DOUT	High-Z	I _{CC}
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	DIN	High-Z	I _{CC}
	L	L	H	X	H	L	High-Z	DIN	
	L	L	H	X	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.2 to V _{DD} +0.3	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS62WV12816ALL	IS62WV12816BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V _{DD}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I _{OH} = -1 mA	2.5-3.6V	2.2	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I _{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V _{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V _{DD} + 0.2	V
			2.5-3.6V	2.2	V _{DD} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}		-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled		-1	1	μA

Notes:

1. V_{IL} (min.) = -1.0V for pulse width less than 10 ns.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

IS62WV12816ALL, IS62WV12816BLL

IS62WV12816ALL, POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Max. 70	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} =Max., I _{OUT} =0 mA, f=f _{MAX} Com. Ind.	15 20	mA
I _{CC1}	Operating Supply Current	V _{DD} =Max., I _{OUT} =0 mA, f=0 Com. Ind.	3 3	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} CS1=V _{IH} , CS2=V _{IL} , f=1 MHz Com. Ind. OR	0.3 0.3	mA
	ULB Control	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} CS1=V _{IL} , f=0, $\overline{UB}$ =V _{IH} , $\overline{LB}$ =V _{IH}		
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} =Max., CS1 ≥ V _{DD} -0.2V, CS2 ≤ 0.2V, V _{IN} ≥ V _{DD} -0.2V, or V _{IN} ≤ 0.2V, f=0 Com. Ind. OR	5 10	μA
	ULB Control	V _{DD} = Max., $\overline{CS1}$ = V _{IL} , CS2=V _{IH} V _{IN} ≤ 0.2V, f=0; $\overline{UB}/\overline{LB}$ =V _{DD} -0.2V		

IS62WV12816BLL, POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Max. 45	Max. 55	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} =Max., I _{OUT} =0 mA, f=f _{MAX} Com. Ind. typ. ⁽²⁾	35 40 25	25 30 20	mA
I _{CC1}	Operating Supply Current	V _{DD} =Max., I _{OUT} =0 mA, f=0 Com. Ind.	3 3	3 3	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} CS1=V _{IH} , CS2=V _{IL} , f=1 MHz Com. Ind. OR	0.3 0.3	0.3 0.3	mA
	ULB Control	V _{DD} =Max., V _{IN} =V _{IH} or V _{IL} CS1=V _{IL} , f=0, $\overline{UB}$ =V _{IH} , $\overline{LB}$ =V _{IH}			
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} =Max., CS1 ≥ V _{DD} -0.2V, CS2 ≤ 0.2V, V _{IN} ≥ V _{DD} -0.2V, or V _{IN} ≤ 0.2V, f=0 Com. Ind. typ. ⁽²⁾ OR	10 10 3	10 10 3	μA
	ULB Control	V _{DD} = Max., $\overline{CS1}$ = V _{IL} , CS2=V _{IH} V _{IN} ≤ 0.2V, f=0; $\overline{UB}/\overline{LB}$ =V _{DD} -0.2V			

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

AC TEST CONDITIONS

Parameter	62WV12816ALL (Unit)	62WV12816BLL (Unit)
Input Pulse Level	0.4V to V _{DD} -0.2V	0.4V to V _{DD} -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V _{REF}	V _{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.65-2.2V	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V _{REF}	0.9V	1.5V
V _{TM}	1.8V	2.8V

AC TEST LOADS

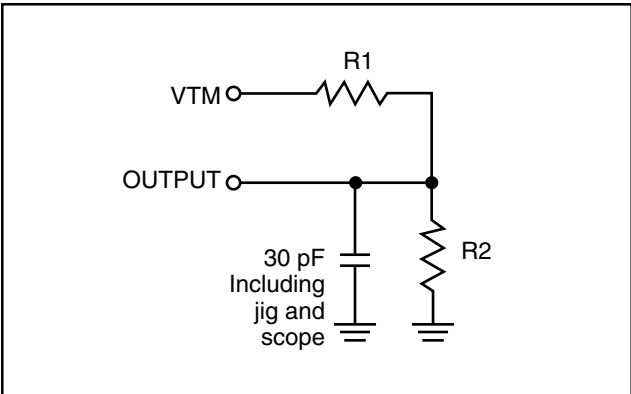


Figure 1

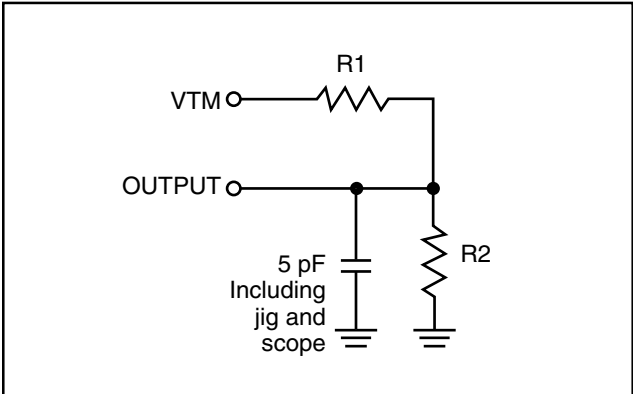


Figure 2

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

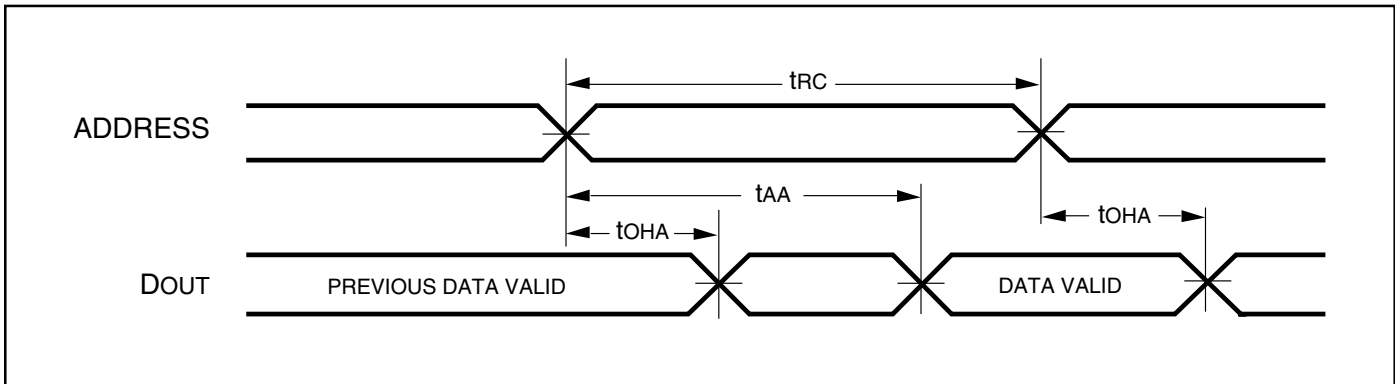
Symbol	Parameter	45 ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t _{AA}	Address Access Time	—	45	—	55	—	70	ns
t _{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t _{ACS1} /t _{ACS2}	$\overline{\text{CS1}}$ /CS2 Access Time	—	45	—	55	—	70	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	20	—	25	—	35	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	—	15	—	20	—	25	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	5	—	5	—	5	—	ns
t _{HZCS1} /t _{HZCS2} ⁽²⁾	$\overline{\text{CS1}}$ /CS2 to High-Z Output	0	15	0	20	0	25	ns
t _{LZCS1} /t _{LZCS2} ⁽²⁾	$\overline{\text{CS1}}$ /CS2 to Low-Z Output	10	—	10	—	10	—	ns
t _{BA}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Access Time	—	45	—	55	—	70	ns
t _{HZB}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to High-Z Output	0	15	0	20	0	25	ns
t _{LZB}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

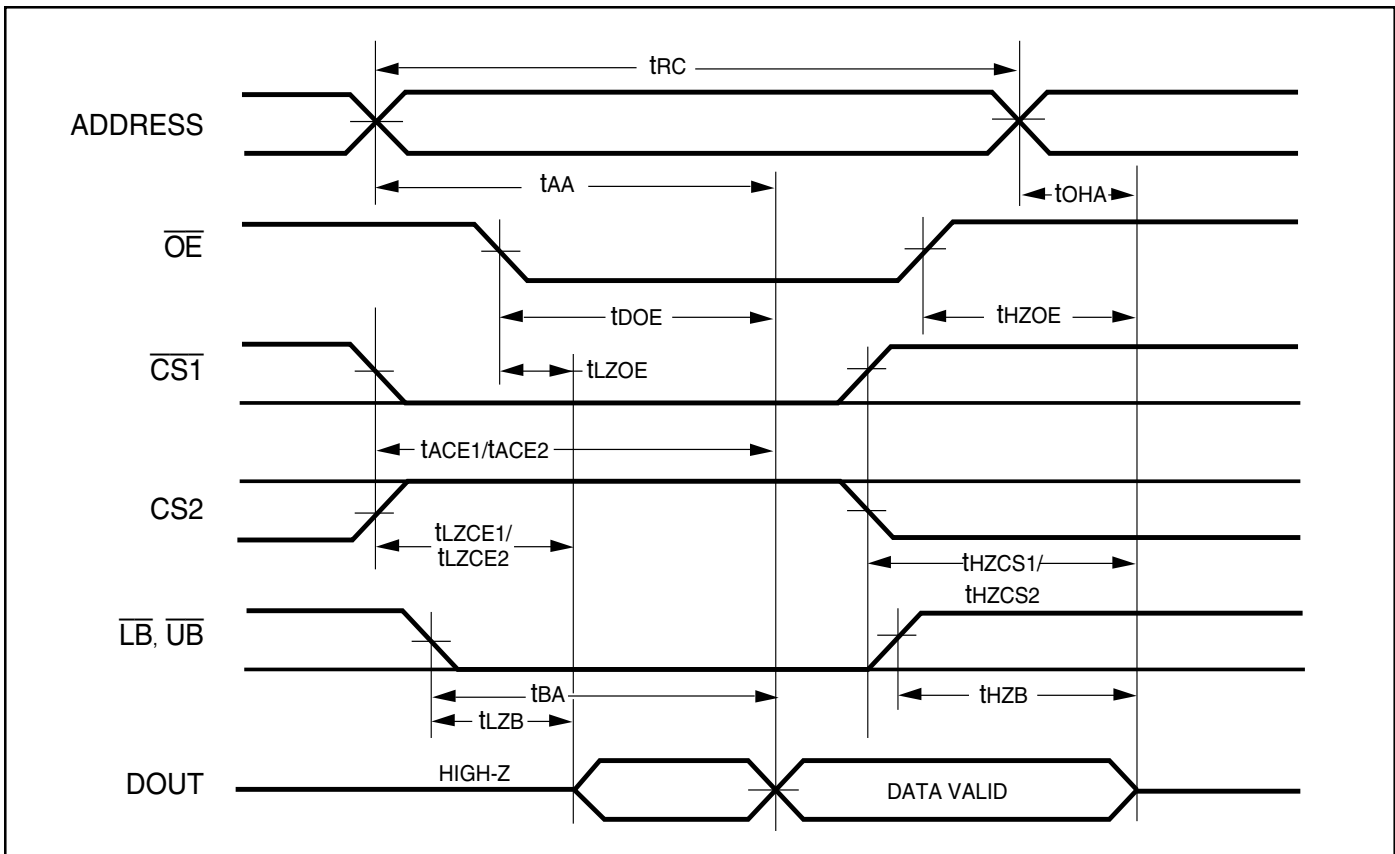
AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, $CS2$, $\overline{OE}$, AND $\overline{UB}/\overline{LB}$ Controlled)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$. $CS2 = \overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

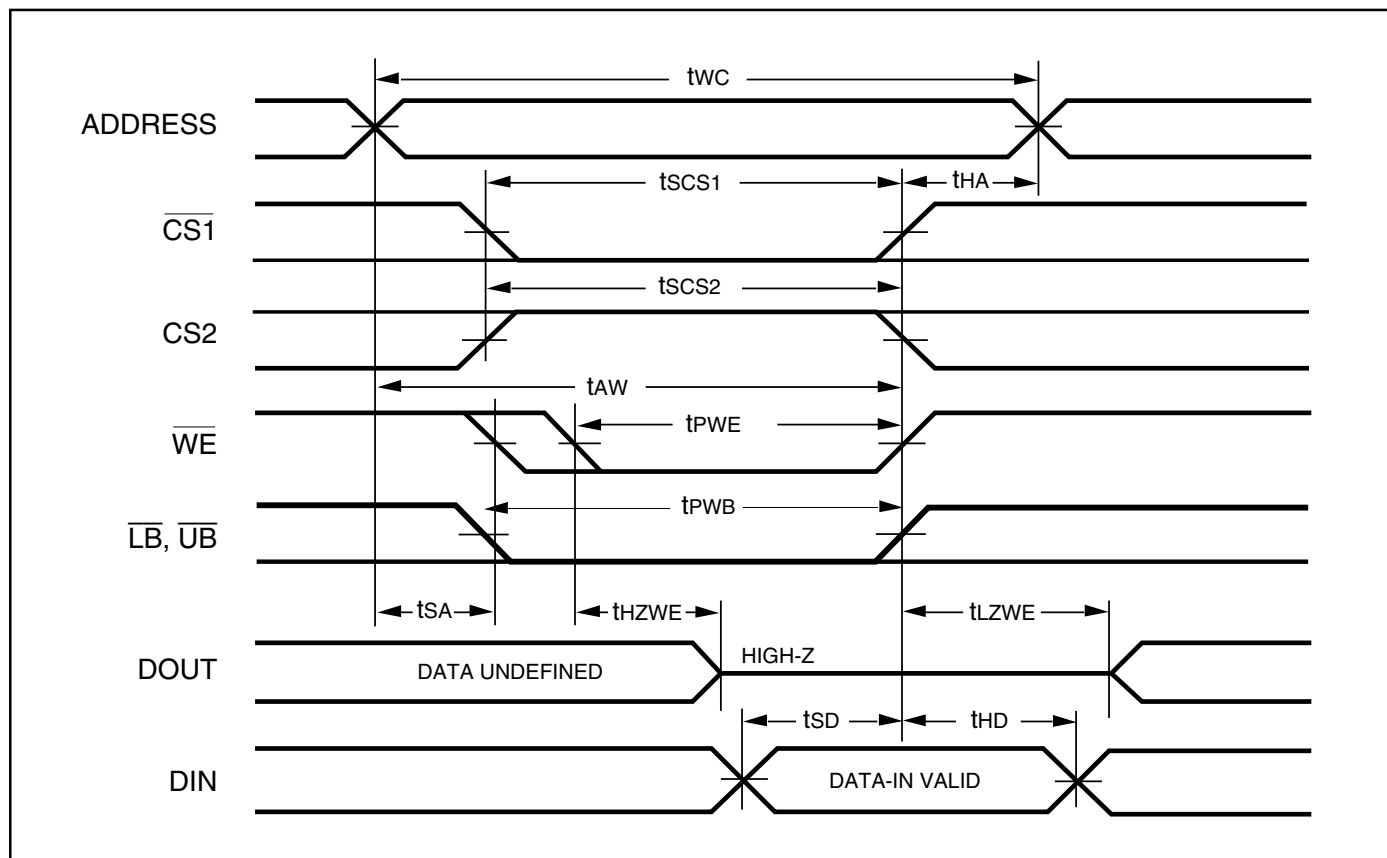
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

Symbol	Parameter	45ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t _{SCS1/tSCS2}	$\overline{CS1}/\overline{CS2}$ to Write End	35	—	45	—	60	—	ns
t _{AW}	Address Setup Time to Write End	35	—	45	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	35	—	45	—	60	—	ns
t _{PWE}	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
t _{SD}	Data Setup to Write End	20	—	25	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽³⁾	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t _{LZWE} ⁽³⁾	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

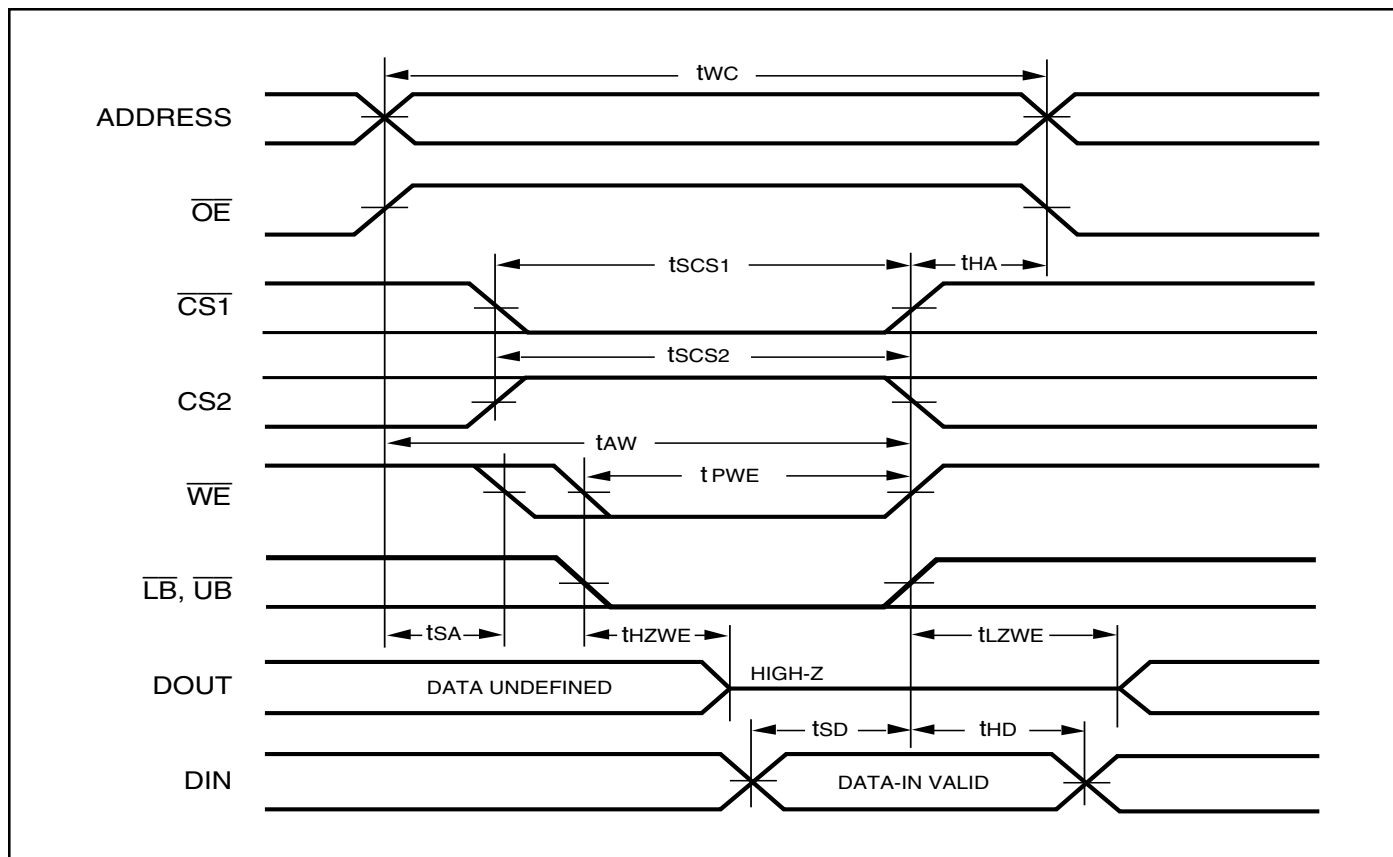
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)

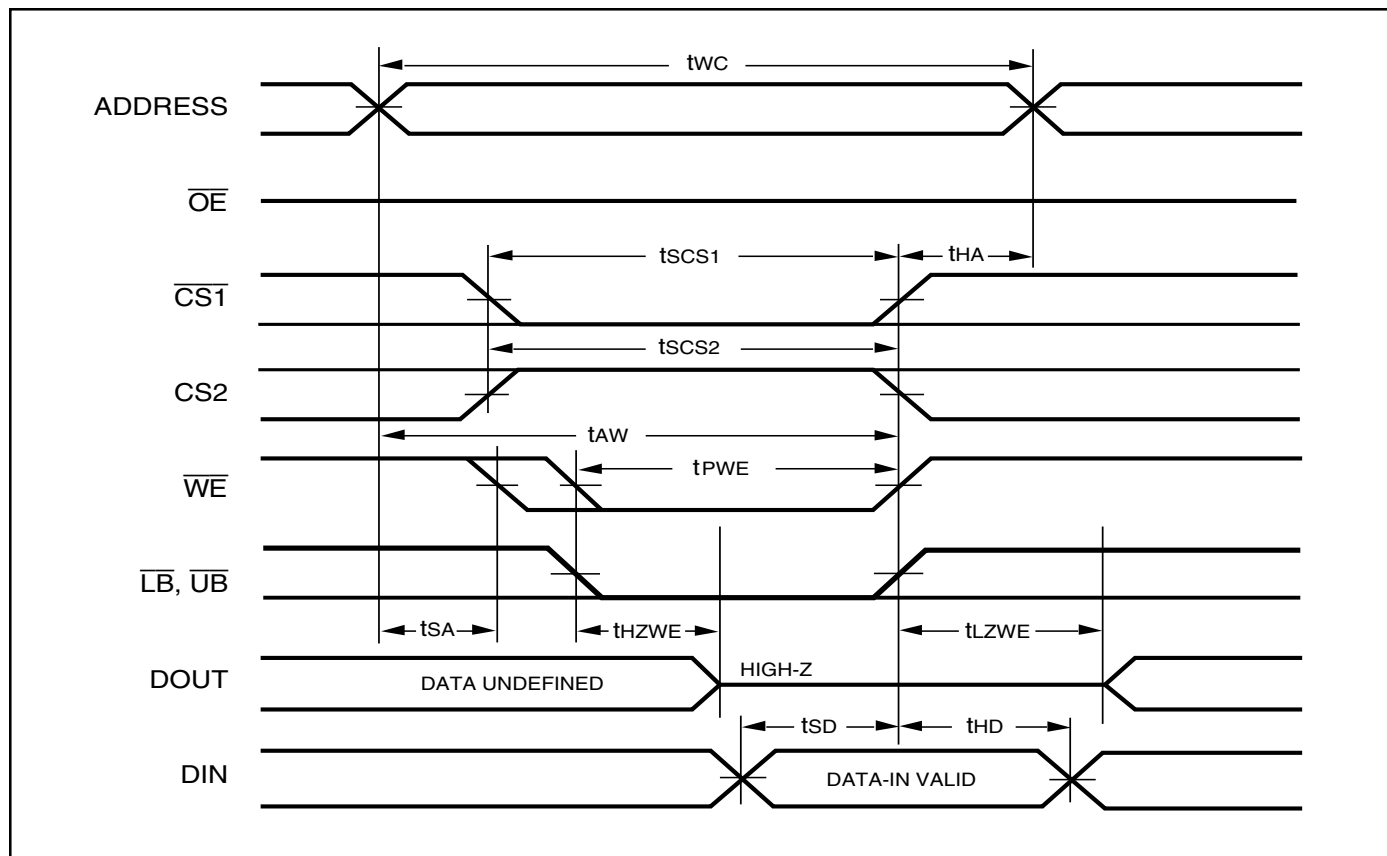
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, $\overline{CS2}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. $WRITE = (\overline{CS1}) [(\overline{LB}) = (\overline{UB})] (\overline{WE})$.

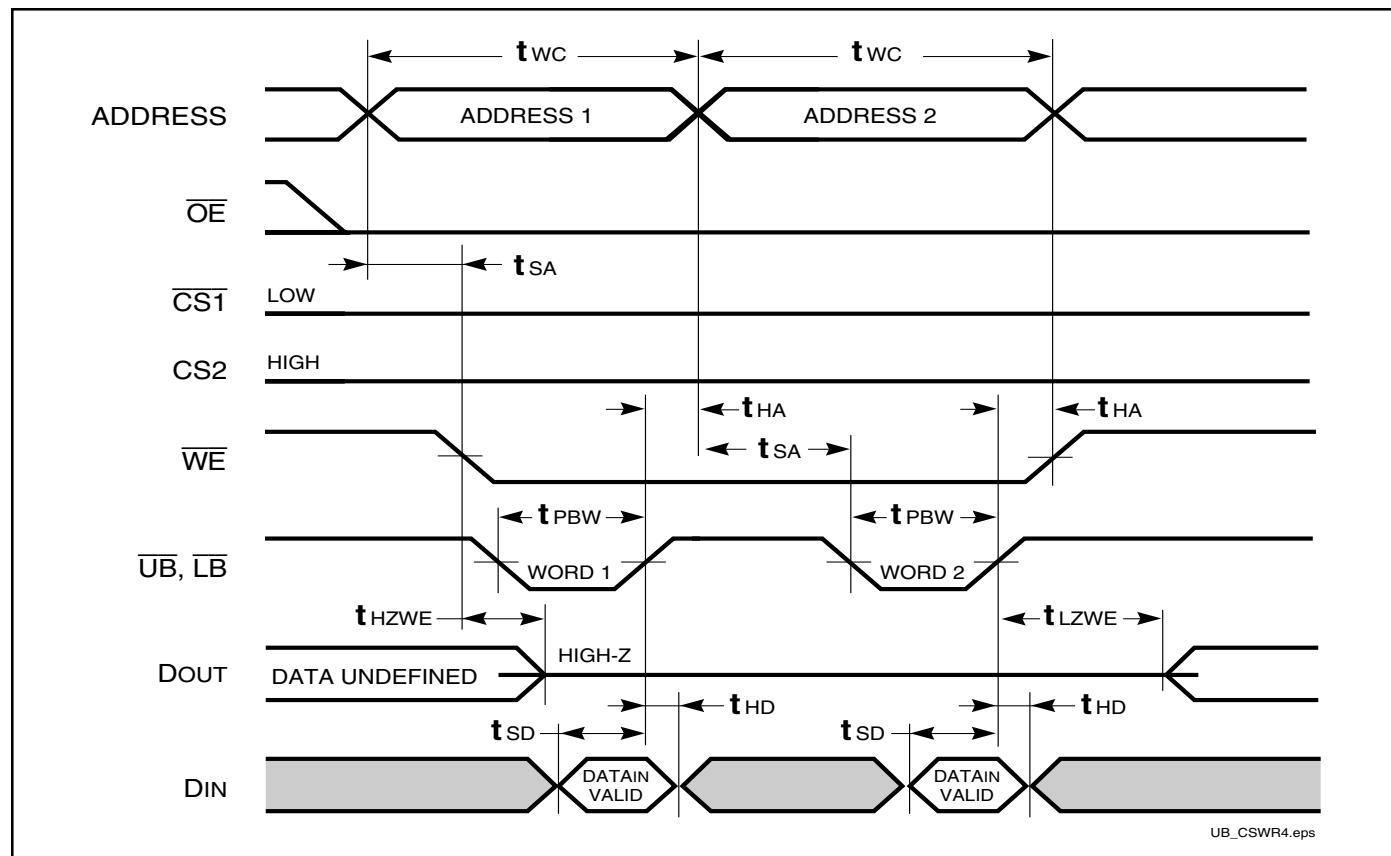
AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)

AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

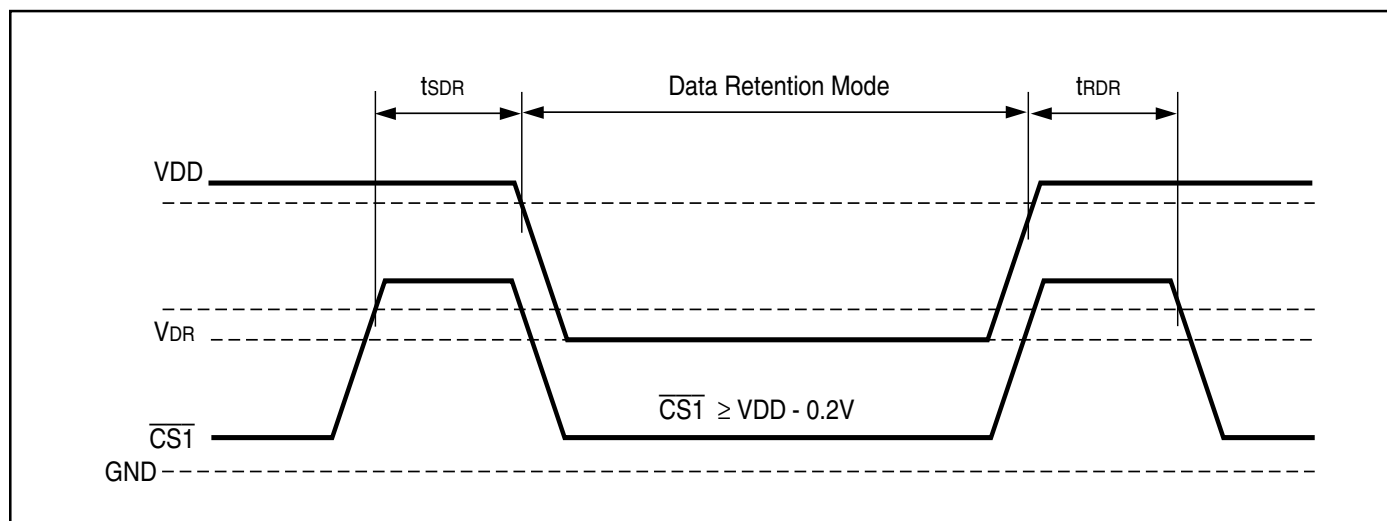
AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Controlled)

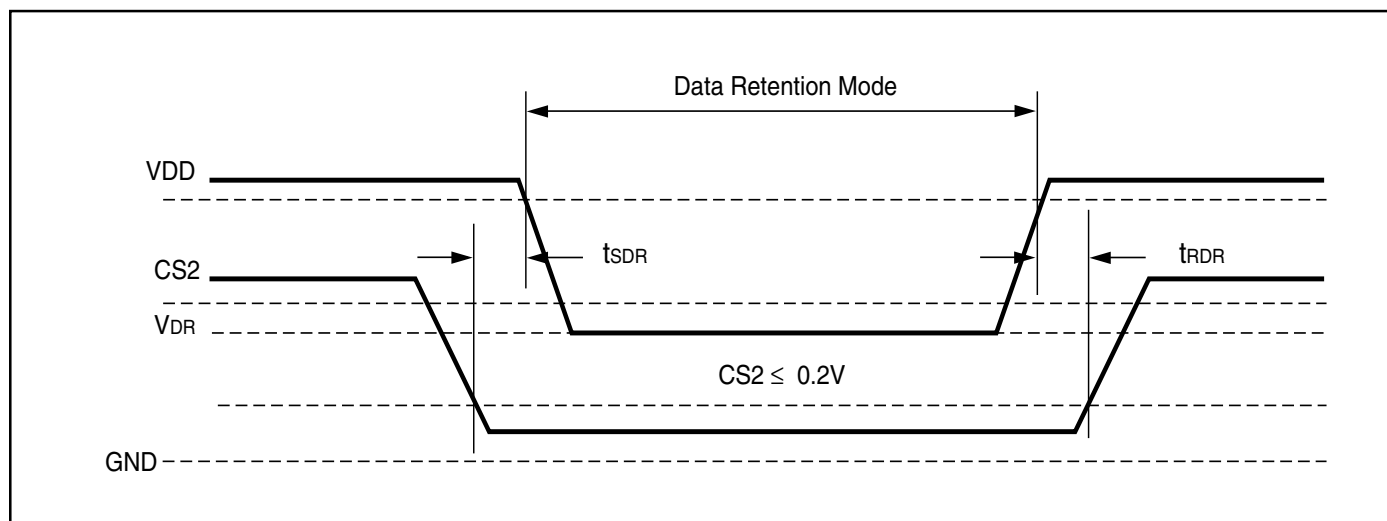
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.0	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.0V$, $\overline{CS1} \geq V_{DD} - 0.2V$	—	10	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM ($CS2$ Controlled)



IS62WV12816ALL, IS62WV12816BLL

ORDERING INFORMATION: IS62WV12816ALL (1.65V - 2.2V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS62WV12816ALL-70T	TSOP (Type II)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62WV12816ALL-70TI	TSOP (Type II)
70	IS62WV12816ALL-70BI	mini BGA (6mm x 8mm)
70	IS62WV12816ALL-70BLI	mini BGA (6mm x 8mm), Lead-free
70	IS62WV12816ALL-70B2I	mini BGA (6mm x 8mm), 2 CS Option

ORDERING INFORMATION: IS62WV12816BLL (2.5V - 3.6V)

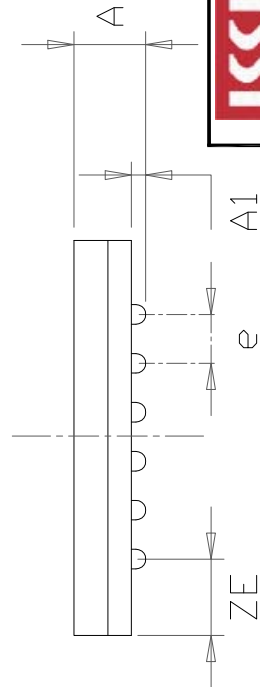
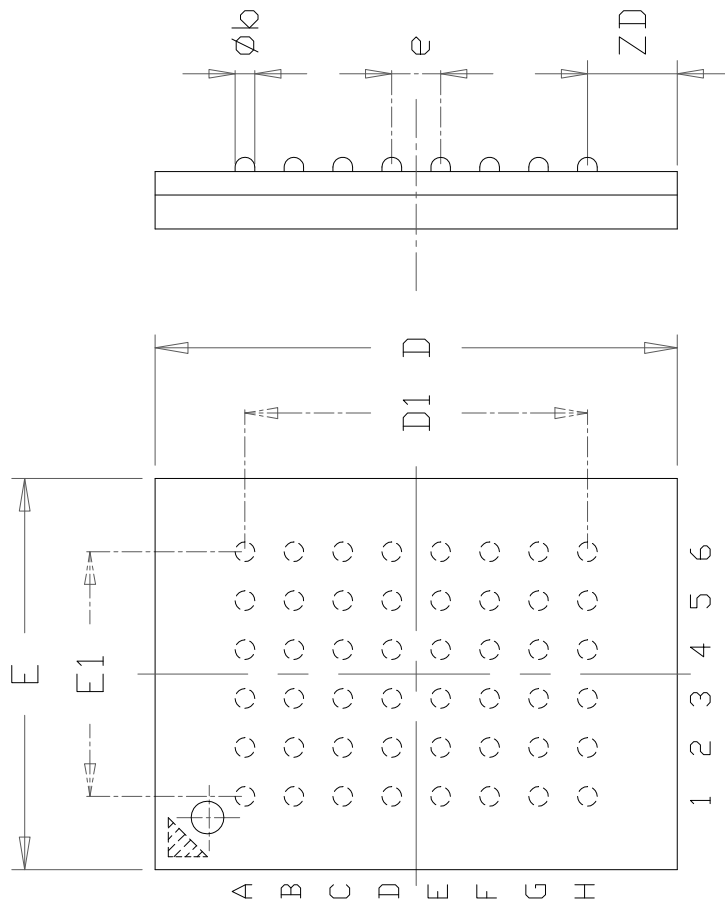
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62WV12816BLL-45B	mini BGA (6mm x 8mm)
45	IS62WV12816BLL-45B2	mini BGA (6mm x 8mm), 2 CS Option
55	IS62WV12816BLL-55T	TSOP (Type II)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV12816BLL-45TLI	TSOP (Type II), Lead-free
55	IS62WV12816BLL-55TI	TSOP (Type II)
55	IS62WV12816BLL-55TLI	TSOP (Type II), Lead-free
55	IS62WV12816BLL-55BI	mini BGA (6mm x 8mm)
55	IS62WV12816BLL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV12816BLL-55B2I	mini BGA (6mm x 8mm), 2 CS Option
55	IS62WV12816BLL-55B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
ϕb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25	BSC		0.207	BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75	BSC		0.148	BSC	
e	0.75	BSC.		0.030	BSC.	
ZD	1.375	REF.		0.054	REF.	
ZE	1.125	REF.		0.044	REF.	

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



TITLE

48L 6x8mm TF-BGA
Package Outline

REV.

C

DATE

08/12/2008

