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Previous Version: 2.10

Page	Subjects (major changes since last revision)
4, 22, 24	revised typo

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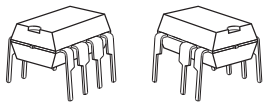
Off-Line SMPS Current Mode Controller with integrated 650V/800V CoolMOS™

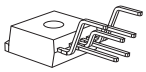
Product Highlights

- **Best in class in DIP8, DIP7, TO220 and DSO16/12 packages**
- **No heat-sink required for DIP8, DIP7 and DSO16/12**
- **Increased creepage distance for TO220, DIP7 and DSO16/12**
- **Isolated drain for TO220 packages**
- **Lowest standby power dissipation**
- **Enhanced protection functions with Auto Restart Mode**
- **Pb-free plating, halogen free mold compound**

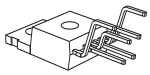


PG-DIP-7-1

PG-DIP-8



PG-TO220-6-46



PG-TO220-6-47

PG-DSO-16/12

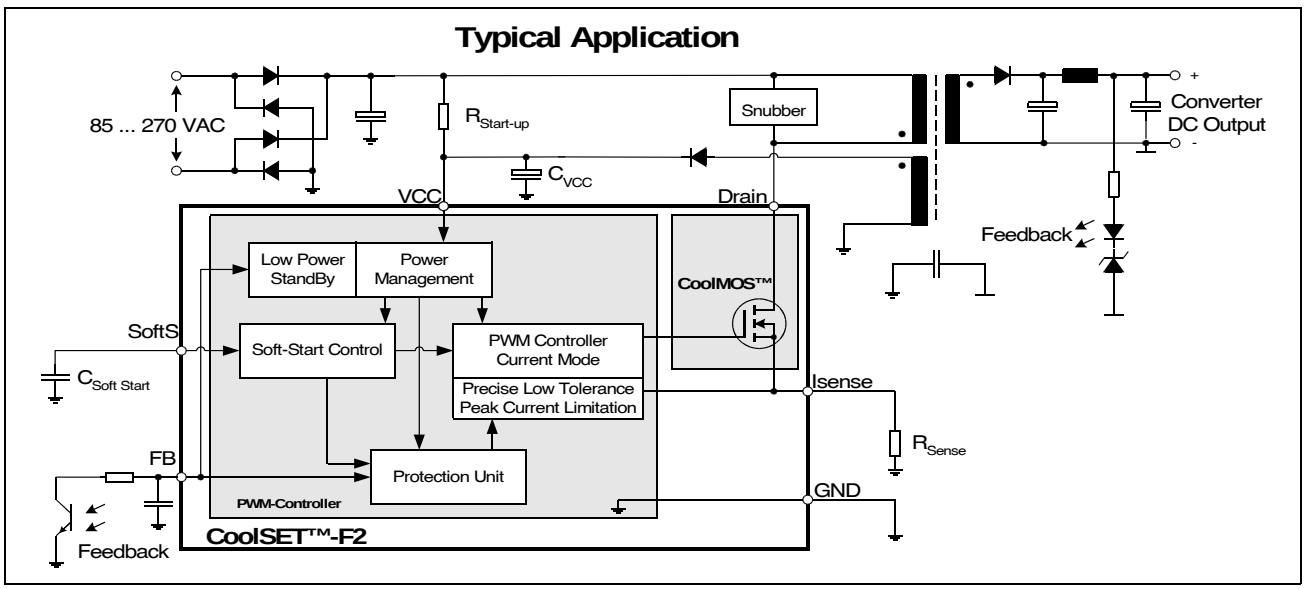
Features

- 650V/800V avalanche rugged CoolMOS™
- Only few external components required
- Input Vcc Undervoltage Lockout
- 67kHz/100kHz switching frequency
- Max duty cycle 72%
- Low Power Standby Mode to meet European Commission Requirements
- Thermal Shut Down with Auto Restart
- Overload and Open Loop Protection
- Overvoltage Protection during Auto Restart
- Adjustable Peak Current Limitation via external resistor
- Overall tolerance of Current Limiting < ±5%
- Internal Leading Edge Blanking
- User defined Soft Start
- Soft driving for low EMI

Description

The second generation CoolSET™-F2 provides several special enhancements to satisfy the needs for low power standby and protection features. In standby mode frequency reduction is used to lower the power consumption and support a stable output voltage in this mode. The frequency reduction is limited to 20kHz/21.5 kHz to avoid audible noise. In case of failure modes like open loop, overvoltage or overload due to short circuit the device switches in Auto Restart Mode which is controlled by the internal protection unit. By means of the internal precise peak current limitation, the dimension of the transformer and the secondary diode can be sized lower which leads to more cost effective for the overall system.

Typical Application



Overview

Type	Package	V_{DS}	F_{OSC}	R_{DSon} [1]	230VAC ±15% [2]	85-265 VAC [2]
ICE2A0565	PG-DIP-8	650V	100kHz	4.7Ω	23W	13W
ICE2A165	PG-DIP-8	650V	100kHz	3.0Ω	31W	18W
ICE2A265	PG-DIP-8	650V	100kHz	0.9Ω	52W	32W
ICE2A365	PG-DIP-8	650V	100kHz	0.45Ω	67W	45W
ICE2B0565	PG-DIP-8	650V	67kHz	4.7Ω	23W	13W
ICE2B165	PG-DIP-8	650V	67kHz	3.0Ω	31W	18W
ICE2B265	PG-DIP-8	650V	67kHz	0.9Ω	52W	32W
ICE2B365	PG-DIP-8	650V	67kHz	0.45Ω	67W	45W
ICE2A0565Z	PG-DIP-7-1	650V	100kHz	4.7Ω	23W	13W
ICE2A180Z	PG-DIP-7-1	800V	100kHz	3.0Ω	29W	17W
ICE2A280Z	PG-DIP-7-1	800V	100KHz	0.8Ω	50W	31W

1) typ @ T=25°C

2) Maximum power rating at T_a=75°C, T_j=125°C and with copper area on PCB = 6cm^2

Type	Package	V_{DS}	F_{OSC}	R_{DSon} [1]	230VAC ±15% [2]	85-265 VAC [2]
ICE2A0565G	PG-DSO-16/12	650V	100kHz	4.7Ω	23W	13W

1) typ @ T=25°C

2) Maximum power rating at T_a=75°C, T_j=125°C and with copper area on PCB = 6cm²

Type	Package	V_{DS}	F_{OSC}	R_{DSon} [1]	230VAC ±15% [2]	85-265 VAC [2]
ICE2A765I	PG-TO-220-6-46	650V	100kHz	0.45Ω	240W	130W
ICE2B765I	PG-TO-220-6-46	650V	67kHz	0.45Ω	240W	130W
ICE2A765P2	PG-TO-220-6-47	650V	100kHz	0.45Ω	240W	130W
ICE2B765P2	PG-TO-220-6-47	650V	67kHz	0.45Ω	240W	130W
ICE2A380P2	PG-TO-220-6-47	800V	100kHz	1.89Ω	111W	60W

1) typ @ T=25°C

2) Maximum practical continuous power in an open frame design at T_a=75°C, T_j=125°C and R_{thCA}=2.7K/W

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1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DIP-8

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	Drain	650V[1]/800V[2] CoolMOS™ Drain
5	Drain	650V[1]/800V[2] CoolMOS™ Drain
6	N.C	Not connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

[1] at T_j = 110°C

[2] at T_j = 25°C

1.2 Pin Configuration with PG-DIP-7-1

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	N.C.	Not connected
5	Drain	650V[1]/800V[2] CoolMOS™ Drain
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

[1] at T_j = 110°C

[2] at T_j = 25°C

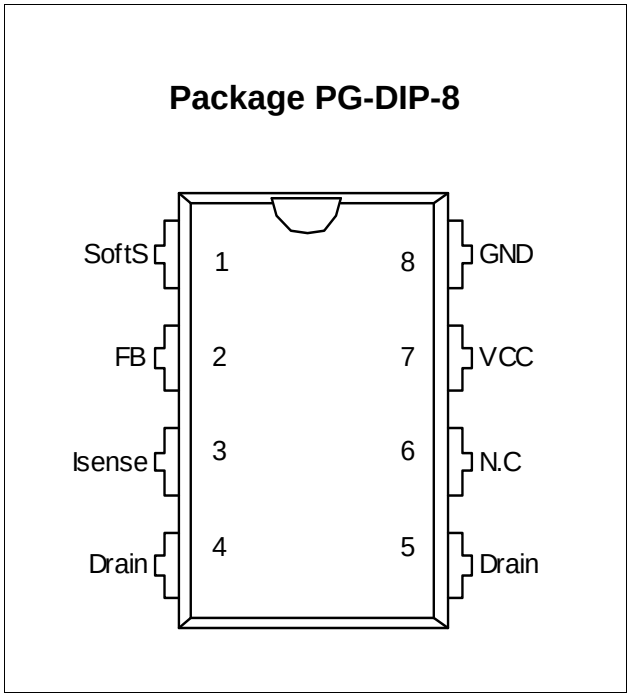

Figure 1 Pin Configuration PG-DIP-8 (top view)

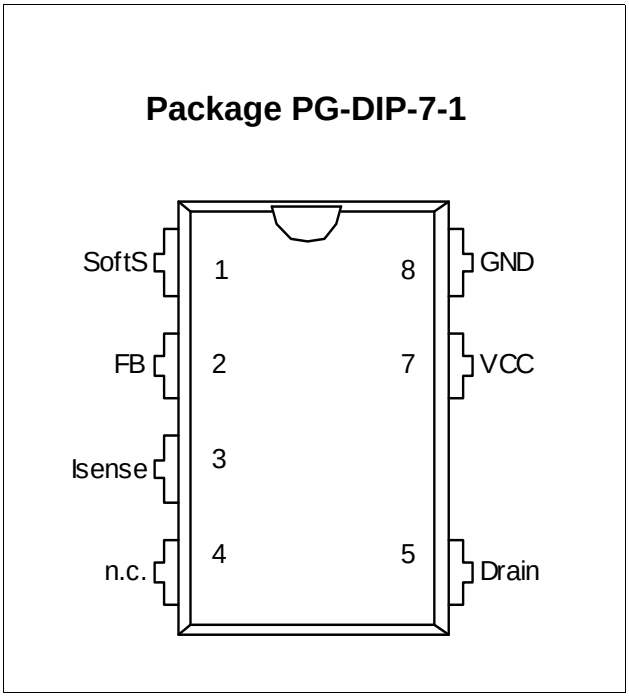

Figure 2 Pin Configuration PG-DIP-7-1 (top view)

1.3 Pin Configuration with PG-TO220-6-46/7

Pin	Symbol	Function
1	Drain	650V[1] CoolMOS™ Drain
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	GND	Controller Ground
5	VCC	Controller Supply Voltage
6	SoftS	Soft-Start
7	FB	Feedback

[1] at T_j = 110°C

Package PG-TO220-6-46/47

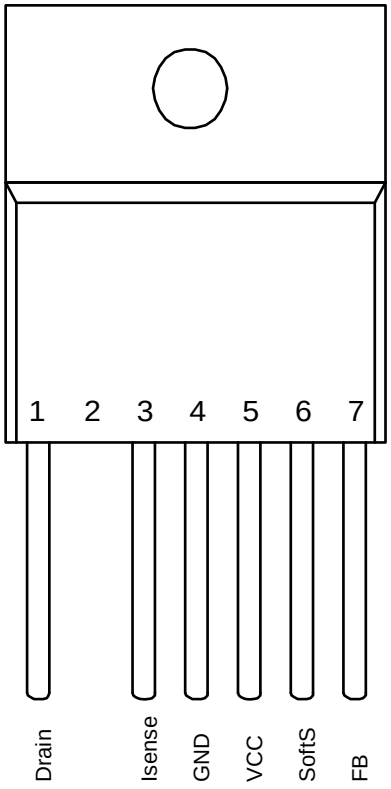

Figure 3 Pin Configuration PG-TO220-6-46/47 (top view)

1.4 Pin Configuration with PG-DSO-16/12

Pin	Symbol	Function
1	N.C.	Not Connected
2	SoftS	Soft-Start
3	FB	Feedback
4	Isense	Controller Current Sense Input, CoolMOS™ Source Output
5	Drain	650V[1] CoolMOS™ Drain
6	Drain	650V[1] CoolMOS™ Drain
7	Drain	650V[1] CoolMOS™ Drain
8	Drain	650V[1] CoolMOS™ Drain
9	N.C.	Not Connected
10	N.C.	Not Connected
11	VCC	Controller Supply Voltage
12	GND	Controller Ground

[1] at T_j = 110°C

Package PG-DSO-16/12

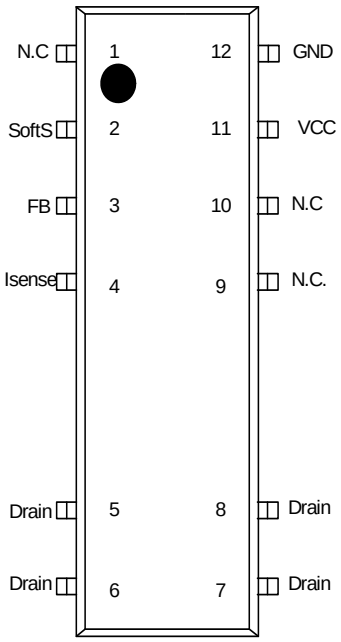

Figure 4 Pin Configuration PG-DSO-16/12 (top view)

1.5 Pin Functionality

SoftS (Soft Start & Auto Restart Control)

This pin combines the function of Soft Start in case of Start Up and Auto Restart Mode and the controlling of the Auto Restart Mode in case of an error detection.

FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle.

Isense (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the integrated CoolMOS™. When Isense reaches the internal threshold of the Current Limit Comparator, the Driver output is disabled. By this means the Over Current Detection is realized.

Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

Drain (Drain of integrated CoolMOS™)

Pin Drain is the connection to the Drain of the internal CoolMOS™.

VCC (Power supply)

This pin is the positive supply of the IC. The operating range is between 8.5V and 21V.

To provide overvoltage protection the driver gets disabled when the voltage becomes higher than 16.5V during Start Up Phase.

GND (Ground)

This pin is the ground of the primary side of the SMPS.

2 Representative Blockdiagram

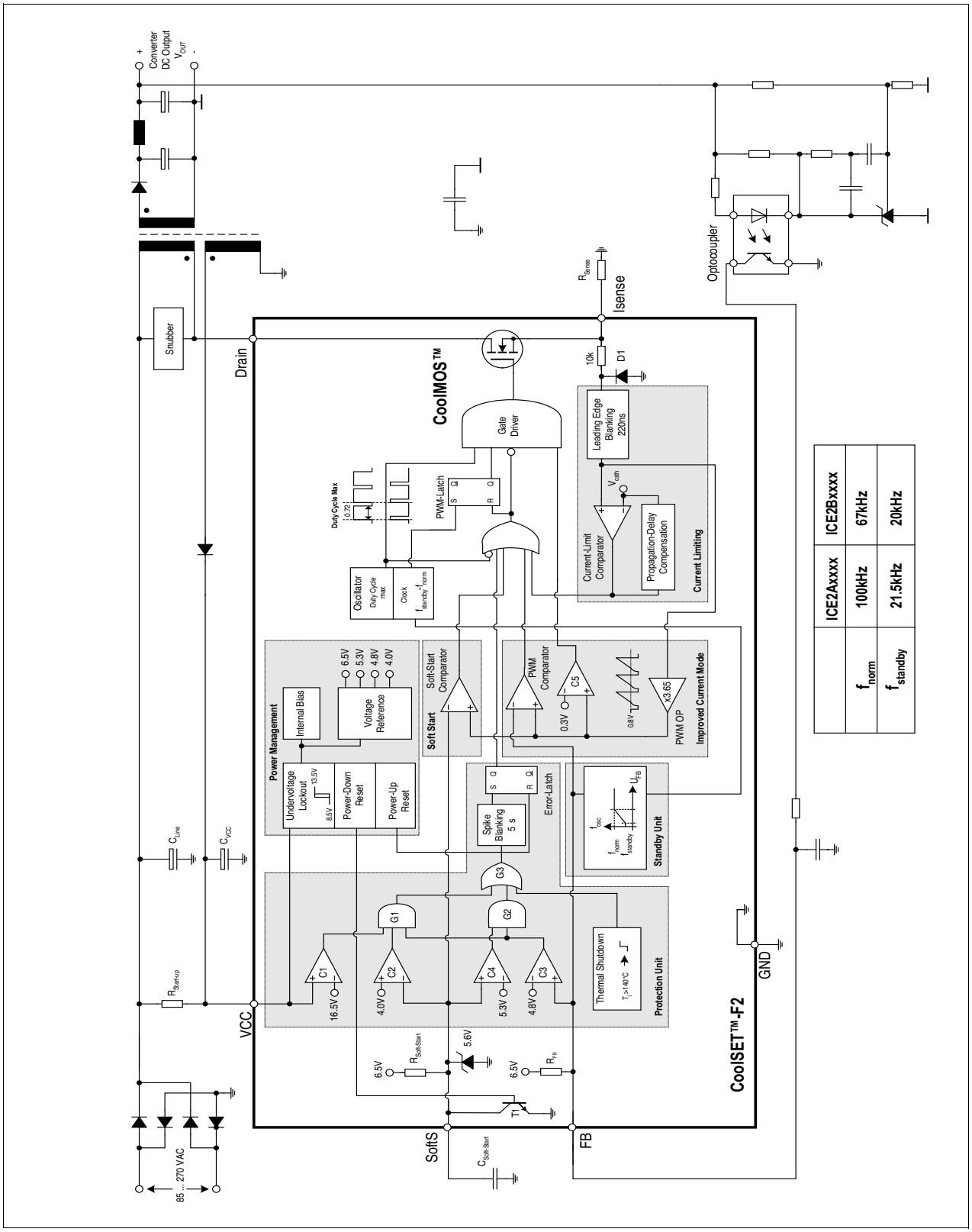

Figure 5 Representative Blockdiagram

3 Functional Description

3.1 Power Management

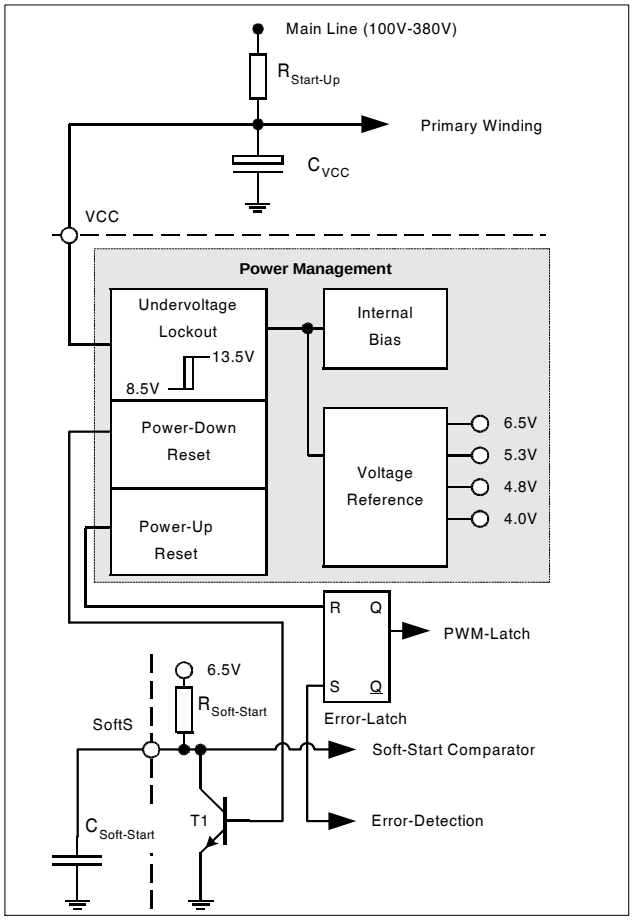

Figure 6 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC}. In case the IC is inactive the current consumption is max. 55µA. When the SMPS is plugged to the main line the current through $R_{Start-up}$ charges the external Capacitor C_{VCC}. When V_{VCC} exceeds the on-threshold V_{CCon}=13.5V the internal bias circuit and the voltage reference are switched on. After that the internal bandgap generates a reference voltage V_{REF}=6.5V to supply the internal circuits. To avoid uncontrolled ringing at switch-on a hysteresis is implemented which means that switch-off is only after active mode when Vcc falls below 8.5V.

In case of switch-on a Power Up Reset is done by resetting the internal error-latch in the protection unit.

When V_{VCC} falls below the off-threshold V_{CCoff}=8.5V the internal reference is switched off and the Power Down reset let T1 discharging the soft-start capacitor $C_{Soft-Start}$ at pin SoftS. Thus it is ensured that at every switch-on the voltage ramp at pin SoftS starts at zero.

3.2 Improved Current Mode

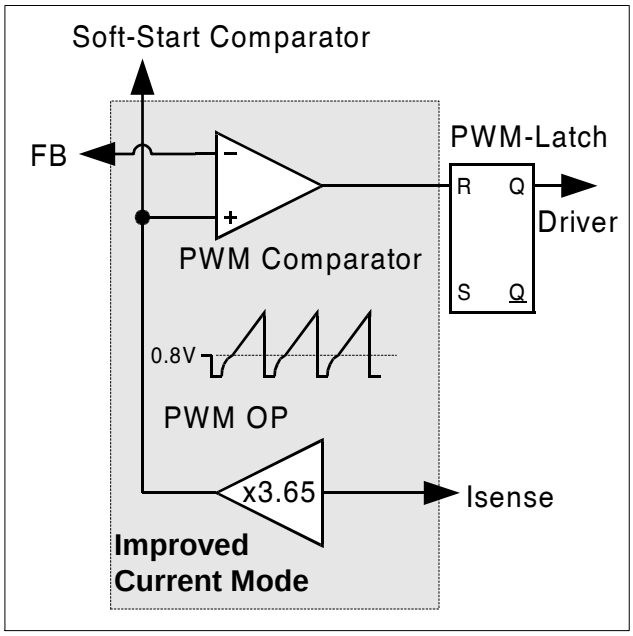

Figure 7 Current Mode

Current Mode means that the duty cycle is controlled by the slope of the primary current. This is done by comparison the FB signal with the amplified current sense signal.

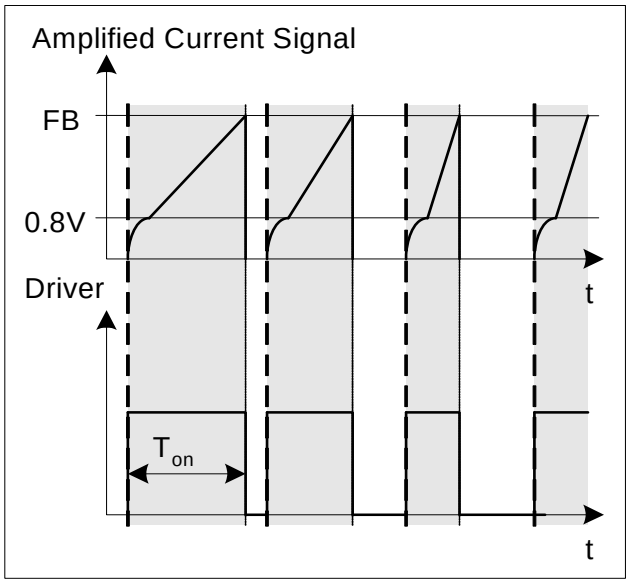

Figure 8 Pulse Width Modulation

In case the amplified current sense signal exceeds the FB signal the on-time T_{on} of the driver is finished by resetting the PWM-Latch (see Figure 8).

The primary current is sensed by the external series resistor R_{Sense} inserted in the source of the integrated CoolMOS™. By means of Current Mode regulation, the

secondary output voltage is insensitive on line variations. Line variation changes the current waveform slope which controls the duty cycle.

The external R_{Sense} allows an individual adjustment of the maximum source current of the integrated CoolMOS™.

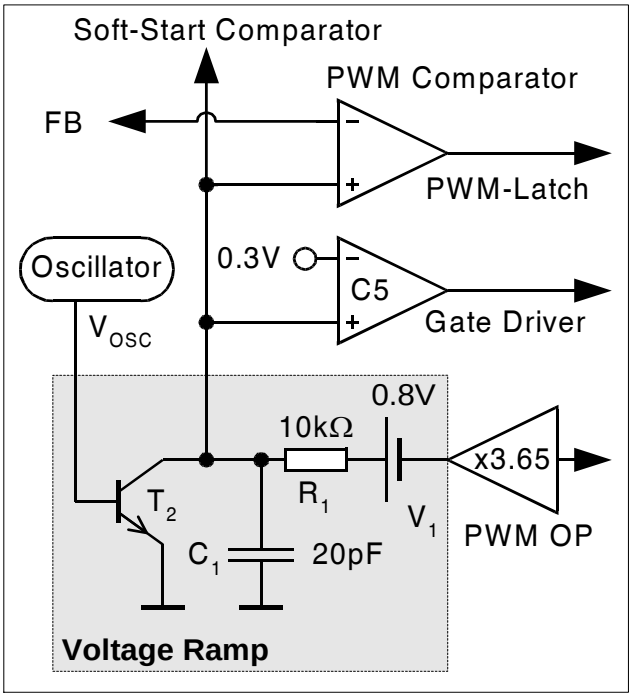

Figure 9 Improved Current Mode

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T_2, the voltage source V_1 and the 1st order low pass filter composed of R_1 and C_1(see Figure 9, Figure 10). Every time the oscillator shuts down for max. duty cycle limitation the switch T2 is closed by V_{OSC}. When the oscillator triggers the Gate Driver T2 is opened so that the voltage ramp can start.

In case of light load the amplified current ramp is to small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the Comparator C5, the Gate Driver is switched-off until the voltage ramp exceeds 0.3V. It allows the duty cycle to be reduced continuously till 0% by decreasing V_{FB} below that threshold.

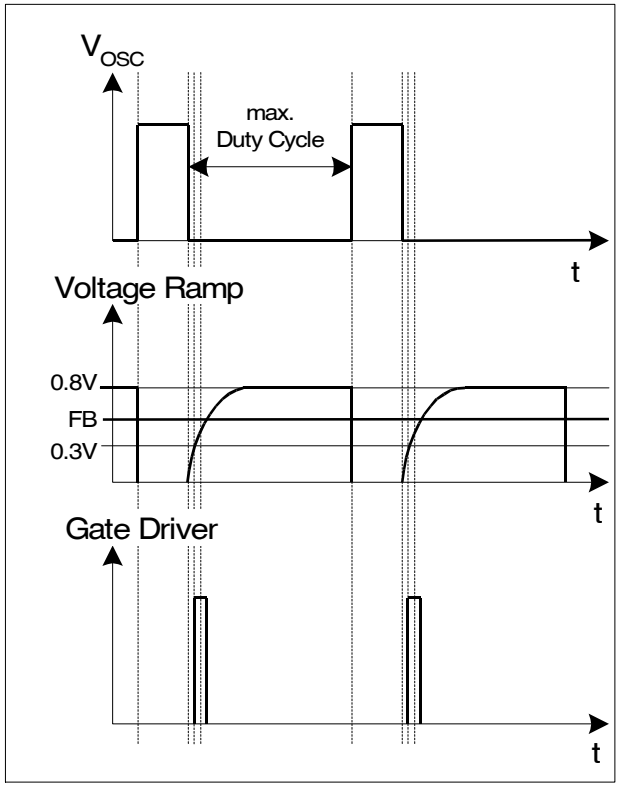

Figure 10 Light Load Conditions

3.2.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor R_{Sense} connected to pin Isense. R_{Sense} converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.65 by PWM OP. The output of the PWM-OP is connected to the voltage source V1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator, C5 and the Soft-Start-Comparator.

3.2.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the integrated CoolMOS™ with the feedback signal V_{FB} (see Figure 11). V_{FB} is created by an external optocoupler or external transistor in combination with the internal pull-up resistor R_{FB} and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS™ exceeds the signal V_{FB} the PWM-Comparator switches off the Gate Driver.

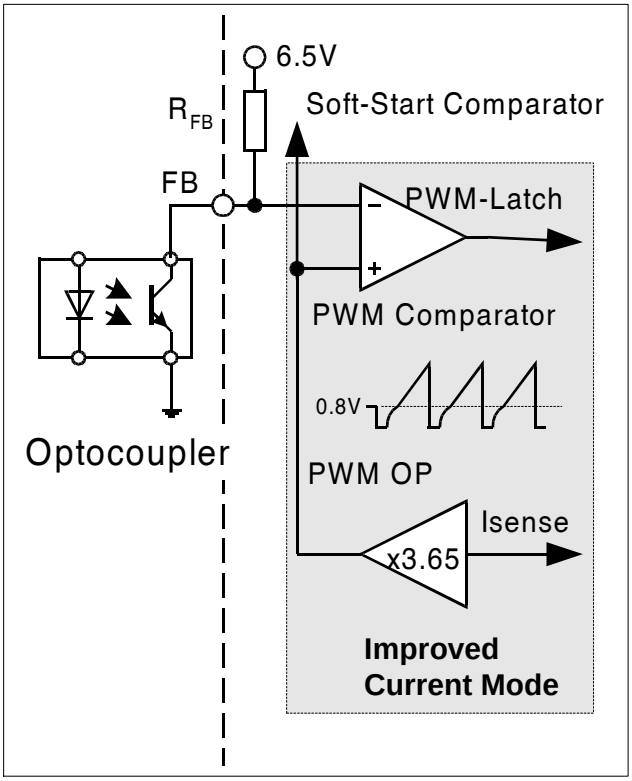

Figure 11 PWM Controlling

3.3 Soft-Start

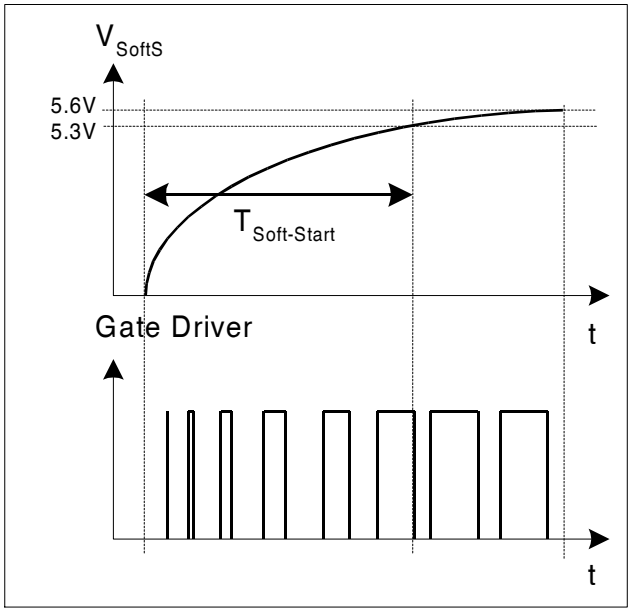

Figure 12 Soft-Start Phase

The Soft-Start is realized by the internal pull-up resistor $R_{Soft-Start}$ and the external Capacitor $C_{Soft-Start}$ (see Figure 5). The Soft-Start voltage V_{SoftS} is generated by charging the external capacitor $C_{Soft-Start}$ by the internal pull-up resistor $R_{Soft-Start}$. The Soft-Start-Comparator compares the voltage at pin SoftS at the negative input with the ramp signal of the PWM-OP at the positive input. When Soft-Start voltage V_{SoftS} is less than Feedback voltage V_{FB} the Soft-Start-Comparator limits the pulse width by resetting the PWM-Latch (see Figure 12). In addition to Start-Up, Soft-Start is also activated at each restart attempt during Auto Restart. By means of the above mentioned $C_{Soft-Start}$ the Soft-Start can be defined by the user. The Soft-Start is finished when V_{SoftS} exceeds 5.3V. At that time the Protection Unit is activated by Comparator C4 and senses the FB by Comparator C3 wether the voltage is below 4.8V which means that the voltage on the secondary side of the SMPS is settled. The internal Zener Diode at SoftS has a clamp voltage of 5.6V to prevent the internal circuit from saturation (see Figure 13).

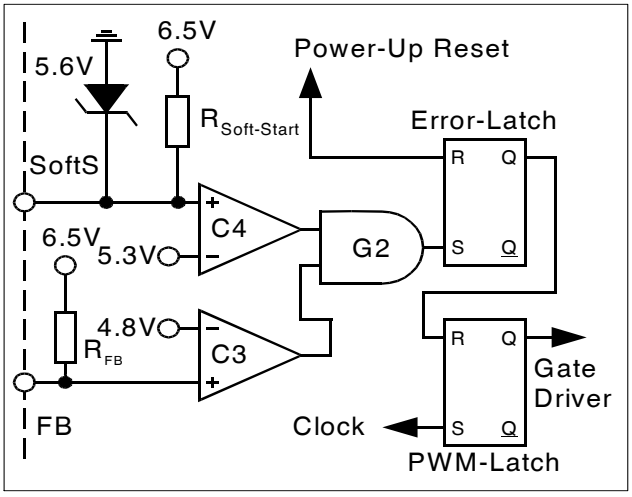

Figure 13 Activation of Protection Unit

The Start-Up time $T_{Start-Up}$ within the converter output voltage V_{OUT} is settled must be shorter than the Soft-Start Phase $T_{Soft-Start}$ (see Figure 14).

$$C_{Soft-Start} = \frac{T_{Soft-Start}}{R_{Soft-Start} \times 1.69}$$

By means of Soft-Start there is an effective minimization of current and voltage stresses on the integrated CoolMOS™, the clamp circuit and the output

overshoot and prevents saturation of the transformer during Start-Up.

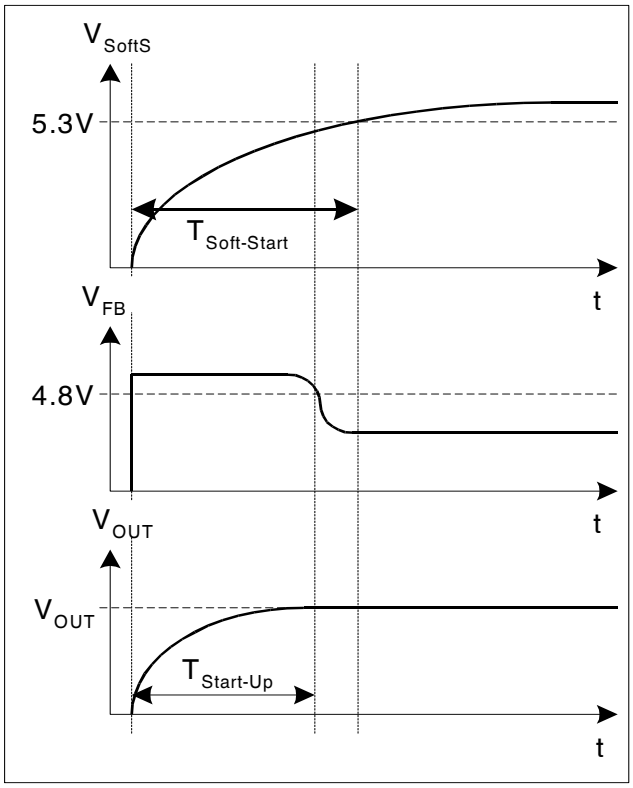

Figure 14 Start Up Phase

3.4 Oscillator and Frequency Reduction

3.4.1 Oscillator

The oscillator generates a frequency f_{switch} = 67kHz/ 100kHz. A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a max. duty cycle limitation of D_{max}=0.72.

3.4.2 Frequency Reduction

The frequency of the oscillator is depending on the voltage at pin FB. The dependence is shown in Figure 15. This feature allows a power supply to operate at lower frequency at light loads thus lowering the switching losses while maintaining good cross regulation performance and low output ripple. In case of low power the power consumption of the whole SMPS can now be reduced very effective. The minimal reachable frequency is limited to 20kHz/21.5 kHz to avoid audible noise in any case.

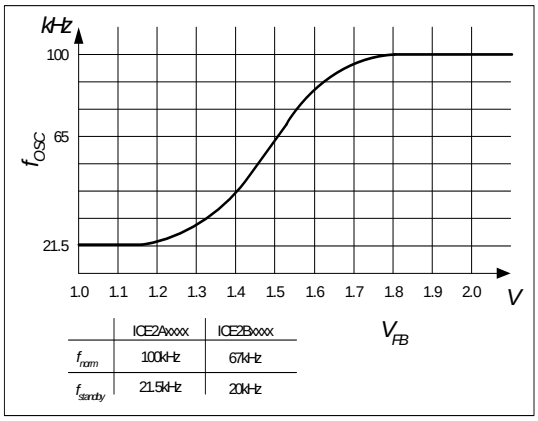

Figure 15 Frequency Dependence

3.5 Current Limiting

There is a cycle by cycle current limiting realized by the Current-Limit Comparator to provide an overcurrent detection. The source current of the integrated CoolMOS™ is sensed via an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense}. When the voltage V_{Sense} exceeds the internal threshold voltage V_{csth} the Current-Limit-Comparator immediately turns off the gate drive. To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated at the Current Sense. Furthermore a Propagation Delay Compensation is added to support the immediate shut down of the CoolMOS™ in case of overcurrent.

3.5.1 Leading Edge Blanking

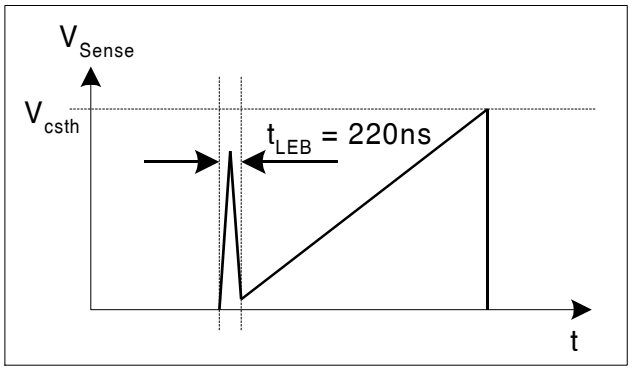

Figure 16 Leading Edge Blanking

Each time when CoolMOS™ is switched on a leading spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. To avoid a premature termination of the

switching pulse this spike is blanked out with a time constant of t_{LEB} = 220ns. During that time the output of the Current-Limit Comparator cannot switch off the gate drive.

3.5.2 Propagation Delay Compensation

In case of overcurrent detection by I_{Limit} the shut down of CoolMOS™ is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current I_{peak} which depends on the ratio of dI/dt of the peak current (see Figure 17).

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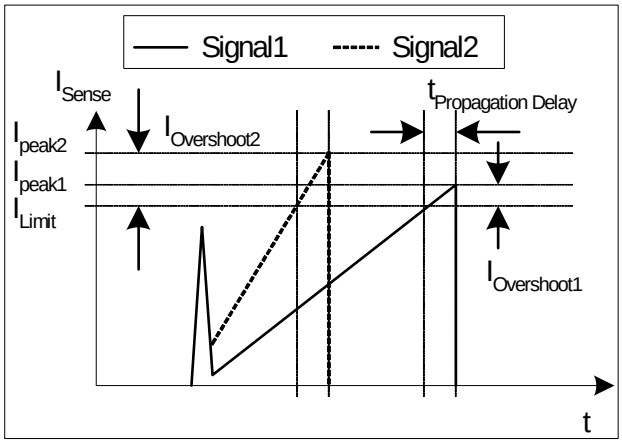


Figure 17 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform.

A propagation delay compensation is integrated to bound the overshoot dependent on dI/dt of the rising primary current. That means the propagation delay time between exceeding the current sense threshold V_{csth} and the switch off of CoolMOS™ is compensated over temperature within a range of at least.

$$0 \leq R_{Sense} \times \frac{dI_{peak}}{dt} \leq \frac{dV_{Sense}}{dt}$$

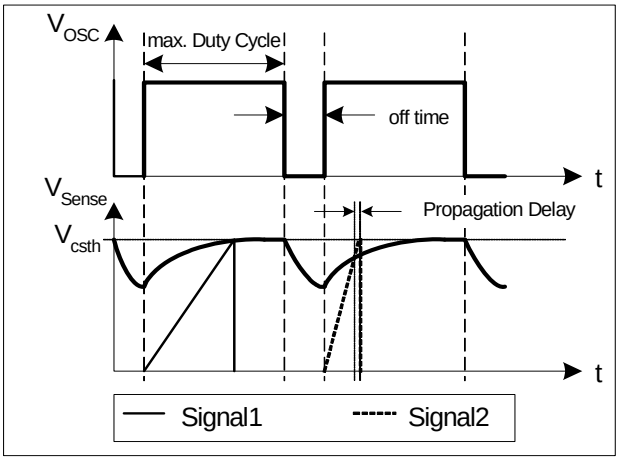


Figure 18 Dynamic Voltage Threshold V_{csth}

The propagation delay compensation is done by means of a dynamic threshold voltage V_{csth} (see Figure 18). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

E.g. I_{peak} = 0.5A with R_{Sense} = 2. Without propagation delay compensation the current sense threshold is set to a static voltage level V_{csth}=1V. A current ramp of dI/dt = 0.4A/µs, that means dV_{Sense}/dt = 0.8V/µs, and a propagation delay time of i.e. $t_{Propagation\ Delay}$ =180ns leads then to a I_{peak} overshoot of 14.4%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 19).

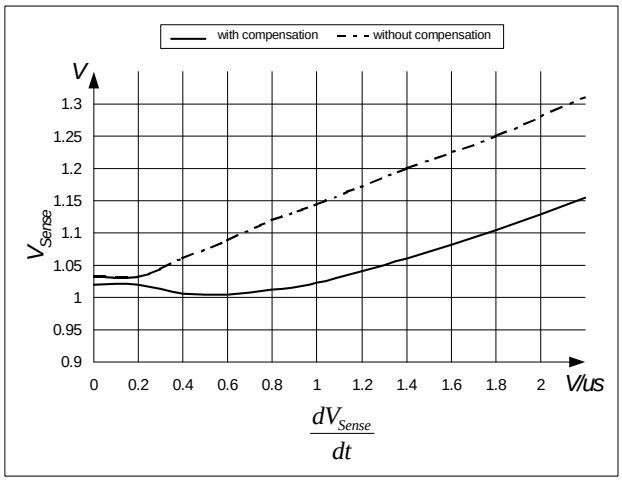


Figure 19 Overcurrent Shutdown

3.6 PWM-Latch

The oscillator clock output applies a set pulse to the PWM-Latch when initiating CoolMOS™ conduction. After setting the PWM-Latch can be reset by the PWM-OP, the Soft-Start-Comparator, the Current-Limit-Comparator, Comparator C3 or the Error-Latch of the Protection Unit. In case of resetting the driver is shut down immediately.

3.7 Driver

The driver-stage drives the gate of the CoolMOS™ and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 20) to the CoolMOS™ gate.

Thus the leading switch on spike is minimized. When CoolMOS™ is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage. At voltages below the undervoltage lockout threshold V_{VCCoff} the gate drive is active low.

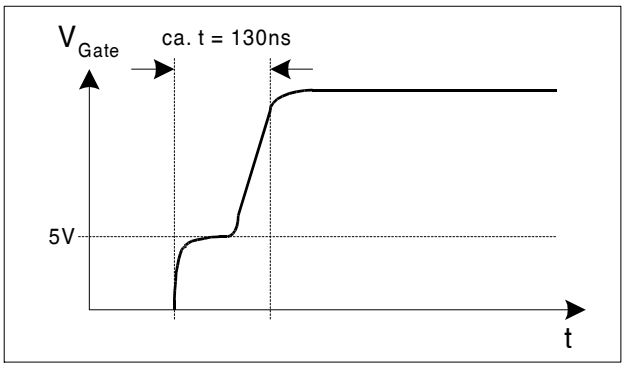


Figure 20 Internal Gate Rising Slope

3.8 Protection Unit (Auto Restart Mode)

An overload, open loop and overvoltage detection is integrated within the Protection Unit. These three failure modes are latched by an Error-Latch. Additional thermal shutdown is latched by the Error-Latch. In case of those failure modes the Error-Latch is set after a blanking time of 5µs and the CoolMOS™ is shut down. That blanking prevents the Error-Latch from distortions caused by spikes during operation mode.

3.8.1 Overload / Open Loop with Normal Load

Figure 21 shows the Auto Restart Mode in case of overload or open loop with normal load. The detection of open loop or overload is provided by the Comparator C3, C4 and the AND-gate G2 (see Figure 22). The detection is activated by C4 when the voltage at pin SoftS exceeds 5.3V. Till this time the IC operates in the Soft-Start Phase. After this phase the comparator C3 can set the Error-Latch in case of open loop or overload which leads the feedback voltage V_{FB} to exceed the threshold of 4.8V. After latching VCC decreases till 8.5V and inactivates the IC. At this time the external Soft-Start capacitor is discharged by the internal transistor T1 due to Power Down Reset. When the IC is inactive V_{VCC} increases till V_{CCon} = 13.5V by charging the Capacitor C_{VCC} by means of the Start-Up Resistor $R_{Start-Up}$. Then the Error-Latch is reset by Power Up Reset and the external Soft-Start capacitor $C_{Soft-Start}$ is charged by the internal pull-up resistor $R_{Soft-Start}$. During the Soft-Start Phase which ends when the voltage at pin SoftS exceeds 5.3V the detection of overload and open loop by C3 and G2 is inactive. In this way the Start Up Phase is not detected as an overload.

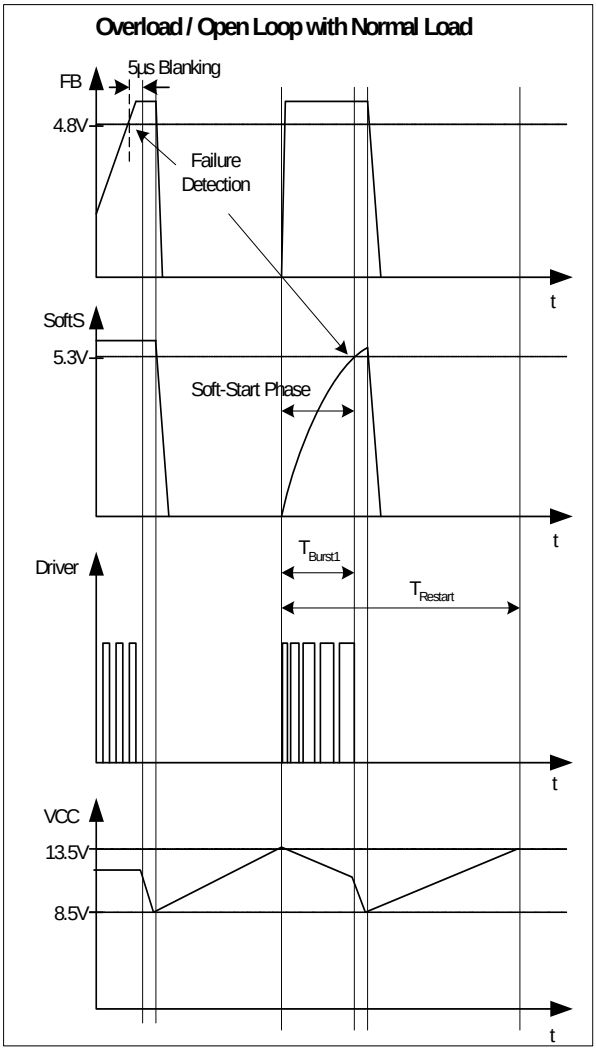


Figure 21 Auto Restart Mode

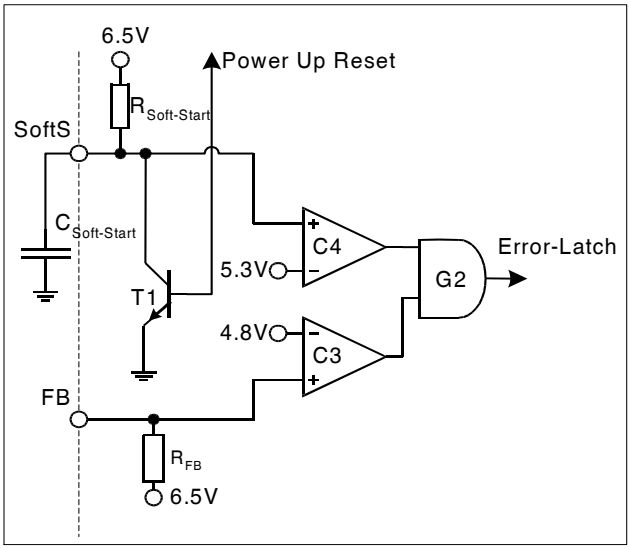


Figure 22 FB-Detection

But the Soft-Start Phase must be finished within the Start Up Phase to force the voltage at pin FB below the failure detection threshold of 4.8V.

3.8.2 Overvoltage due to Open Loop with No Load

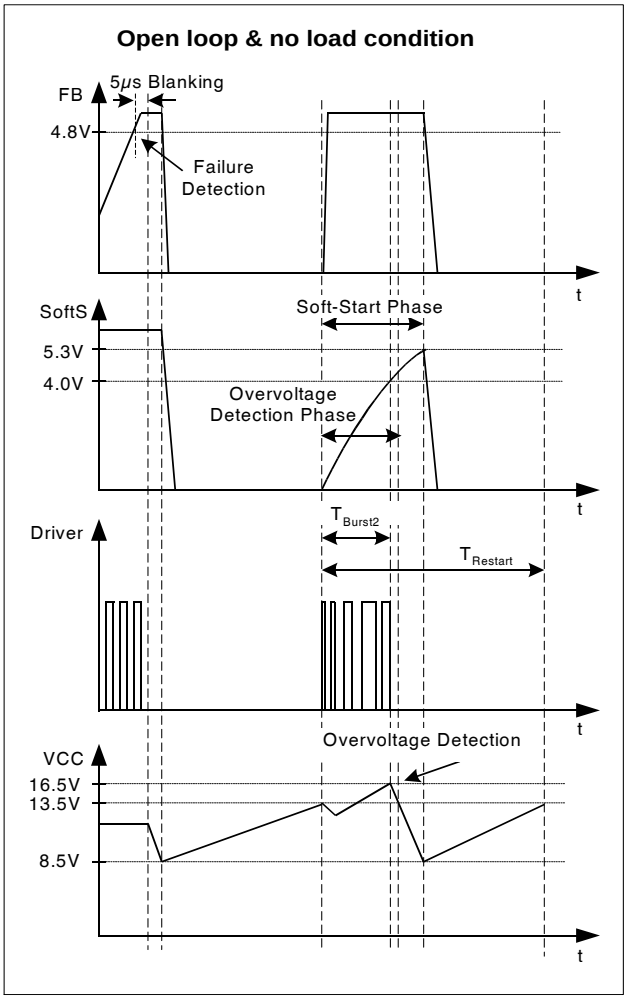


Figure 23 Auto Restart Mode

Figure 23 shows the Auto Restart Mode for open loop and no load condition. In case of this failure mode the converter output voltage increases and also VCC. An additional protection by the comparators C1, C2 and the AND-gate G1 is implemented to consider this failure mode (see Figure 24).The overvoltage detection is provided by Comparator C1 only in the first time during the Soft-Start Phase till the Soft-Start voltage exceeds the threshold of the Comparator C2 at 4.0V and the voltage at pin FB is above 4.8V. When VCC exceeds 16.5V during the overvoltage detection phase C1 can set the Error-Latch and the Burst Phase during Auto Restart Mode is finished earlier. In that case T_{Burst2} is shorter than $T_{Soft\text{-}Start}$. By means of C2 the normal operation mode is prevented from overvoltage detection due to varying of VCC concerning the regulation of the converter output. When the voltage V_{SoftS} is above 4.0V the overvoltage detection by C1 is deactivated.

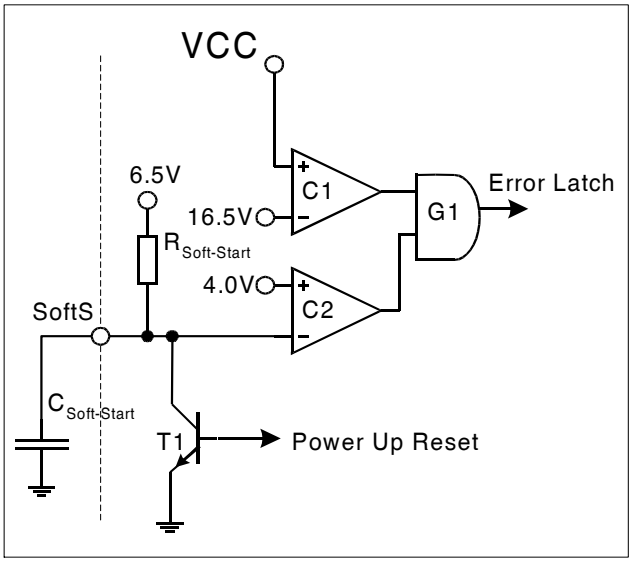


Figure 24 Overvoltage Detection

3.8.3 Thermal Shut Down

Thermal Shut Down is latched by the Error-Latch when junction temperature T_j of the pwm controller is exceeding an internal threshold of 140°C. In that case the IC switches in Auto Restart Mode.

Note: All the values which are mentioned in the functional description are typical. Please refer to Electrical Characteristics for min/max limit values.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 6 (VCC) is discharged before assembling the application circuit.

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Drain Source Voltage ICE2A0565/165/265/365/765I/765P2 ICE2B0565/165/265/365/765I/765P2 ICE2A0565G ICE2A0565Z		V_{DS}	-	650	V	T_j = 110°C
Drain Source Voltage ICE2A180Z/280Z/380P2		V_{DS}	-	800	V	T_j = 25°C
Pulsed drain current, t_p limited by T_{jmax}	ICE2A0565/ ICE2B056/ ICE2A0565G/ ICE2A0565Z	I_{D_Puls1}		2.0	A	
	ICE2A165/ ICE2B165	I_{D_Puls2}		3.8	A	
	ICE2A265/ ICE2B265	I_{D_Puls3}		9.8	A	
	ICE2A365/ ICE2B365	I_{D_Puls4}		23.3	A	
	ICE2A180Z	I_{D_Puls5}		4.1	A	
	ICE2A280Z	I_{D_Puls6}		14.8	A	
	ICE2A765P2/ ICE2B765P2/ ICE2A765I/ ICE2B765I	I_{D_Puls7}		19.0	A	
	ICE2A380P2	I_{D_Puls8}		5.7	A	

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Avalanche energy, repetitive t_{AR} limited by max. T_j=150°C[1)]	ICE2A0565	E_{AR1}	-	0.01	mJ	
	ICE2A165	E_{AR2}	-	0.07	mJ	
	ICE2A265	E_{AR3}	-	0.40	mJ	
	ICE2A365	E_{AR4}	-	0.50	mJ	
	ICE2B0565	E_{AR5}	-	0.01	mJ	
	ICE2B165	E_{AR6}	-	0.07	mJ	
	ICE2B265	E_{AR7}	-	0.40	mJ	
	ICE2B365	E_{AR8}	-	0.50	mJ	
	ICE2A0565G	E_{AR9}	-	0.01	mJ	
	ICE2A0565Z	E_{AR10}	-	0.01	mJ	
	ICE2A180Z	E_{AR11}	-	0.07	mJ	
	ICE2A280Z	E_{AR12}	-	0.40	mJ	
	ICE2A765I	E_{AR13}	-	0.50	mJ	
	ICE2B765I	E_{AR14}	-	0.50	mJ	
	ICE2A765P2	E_{AR15}	-	0.50	mJ	
	ICE2B765P2	E_{AR16}	-	0.50	mJ	
	ICE2A380P2	E_{AR17}	-	0.06	mJ	

[1)] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}* f$

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Avalanche current, repetitive tAR limited by max. T_j=150°C	ICE2A0565	I_{AR1}	-	0.5	A	
	ICE2A165	I_{AR2}	-	1	A	
	ICE2A265	I_{AR3}	-	2	A	
	ICE2A365	I_{AR4}	-	3	A	
	ICE2B0565	I_{AR5}	-	0.5	A	
	ICE2B165	I_{AR6}	-	1	A	
	ICE2B265	I_{AR7}	-	2	A	
	ICE2B365	I_{AR8}	-	3	A	
	ICE2A0565G	I_{AR9}	-	0.5	A	
	ICE2A0565Z	I_{AR10}	-	0.5	A	
	ICE2A180Z	I_{AR11}	-	1	A	
	ICE2A280Z	I_{AR12}	-	2	A	
	ICE2A765I	I_{AR13}	-	7	A	
	ICE2B765I	I_{AR14}	-	7	A	
	ICE2A765P2	I_{AR15}	-	7	A	
	ICE2B765P2	I_{AR16}	-	7	A	
	ICE2A380P2	I_{AR17}	-	2.4	A	
V_{CC} Supply Voltage		V_{CC}	-0.3	22	V	
FB Voltage		V_{FB}	-0.3	6.5	V	
SoftS Voltage		V_{SoftS}	-0.3	6.5	V	
I_{Sense}		I_{Sense}	-0.3	3	V	
Junction Temperature		T_j	-40	150	°C	Controller & CoolMOS™
Storage Temperature		T_S	-50	150	°C	
Thermal Resistance Junction-Ambient		R_{thJA1}	-	90	K/W	PG-DIP-8
		R_{thJA2}	-	96	K/W	PG-DIP-7-1
		R_{thJA3}	-	110	K/W	P-DSO-16/12
ESD Robustness[1)]		V_{ESD}	-	2[2)]	kV	Human Body Model

1) Equivalent to discharging a 100pF capacitor through a 1.5 kW series resistor

2) 1kV at pin drain of ICE2x0565, ICE2A0565Z and ICE2A0565G

4.2 Thermal Impedance (ICE2X765I and ICE2X765P2)

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Thermal Resistance Junction-Ambient	ICE2A765I ICE2B765I ICE2A765P2 ICE2B765P2	R_{thJA4}	-	74	K/W	Free standing with no heat-sink
	ICE2A380P2	R_{thJA5}	-	82	K/W	
Junction-Case	ICE2A765I ICE2B765I ICE2A765P2 ICE2B765P2	R_{thJC1}	-	2.5	K/W	
	ICE2A380P2	R_{thJC2}	-	2.86	K/W	

4.3 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	V_{CCoff}	21	V	
Junction Temperature of Controller	T_{JCon}	-25	130	°C	Limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	$T_{JCoolMOS}$	-25	150	°C	

4.4 Characteristics

Note: The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from – 25 °C to 125 °C.Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

4.4.1 Supply Section

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Start Up Current		I_{VCC1}	-	27	55	µA	V_{CC}=V_{CCon} -0.1V
Supply Current with Inactive Gate		I_{VCC2}	-	5.0	6.6	mA	V_{SoftS} = 0 I_{FB} = 0
Supply Current with Active Gate	ICE2A0565	I_{VCC3}	-	5.3	6.7	mA	V_{SoftS} = 5V I_{FB} = 0
	ICE2A165	I_{VCC4}	-	6.5	7.8	mA	
	ICE2A265	I_{VCC5}	-	6.7	8.0	mA	
	ICE2A365	I_{VCC6}	-	8.5	9.8	mA	
	ICE2B0565	I_{VCC7}	-	5.2	6.7	mA	
	ICE2B165	I_{VCC8}	-	5.5	7.0	mA	
	ICE2B265	I_{VCC9}	-	6.1	7.3	mA	
	ICE2B365	I_{VCC10}	-	7.1	8.3	mA	
	ICE2A0565G	I_{VCC11}	-	5.3	6.7	mA	
	ICE2A0565Z	I_{VCC12}	-	5.3	6.7	mA	
	ICE2A180Z	I_{VCC13}	-	6.5	7.8	mA	
	ICE2A280Z	I_{VCC14}	-	7.7	9.0	mA	
Supply Current with Active Gate	ICE2A765I	I_{VCC15}	-	8.5	9.8	mA	V_{SoftS} = 5V I_{FB} = 0
	ICE2B765I	I_{VCC16}	-	7.1	8.3	mA	
	ICE2A765P2	I_{VCC17}	-	8.5	9.8	mA	
	ICE2B765P2	I_{VCC18}	-	7.1	8.3	mA	
	ICE2A380P2	I_{VCC19}	-	6.7	8.0	mA	
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis		V_{CCon} V_{CCoff} V_{CCHY}	13 - 4.5	13.5 8.5 5	14 - 5.5	V V V	

4.4.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V_{REF}	6.37	6.50	6.63	V	measured at pin FB

4.4.3 Control Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator Frequency ICE2A0565/165/265/365/765I/765P2 ICE2A0565G/0565Z/180Z/280Z/380P2	f_{OSC1}	93	100	107	kHz	V_{FB} = 4V
Oscillator Frequency ICE2B0565/165/265/365/765I/765P2	f_{OSC3}	62	67	72	kHz	V_{FB} = 4V
Reduced Osc. Frequency ICE2A0565/165/265/365/765I/765P2 ICE2A0565G/0565Z/180Z/280Z/380P2	f_{OSC2}	-	21.5	-	kHz	V_{FB} = 1V
Reduced Osc. Frequency ICE2B0565/165/265/365/765I/765P2	f_{OSC4}	-	20	-	kHz	V_{FB} = 1V
Frequency Ratio f_{osc1}/f_{osc2} ICE2A0565/165/265/365/765I/765P2 ICE2A0565G/0565Z/180Z/280Z/380P2		4.5	4.65	4.9		
Frequency Ratio f_{osc3}/f_{osc4} ICE2B0565/165/265/365/765I/765P2		3.18	3.35	3.53		
Max Duty Cycle	D_{max}	0.67	0.72	0.77		
Min Duty Cycle	D_{min}	0	-	-		V_{FB} < 0.3V
PWM-OP Gain	A_V	3.45	3.65	3.85		
V_{FB} Operating Range Min Level	V_{FBmin}	0.3	-	-	V	
V_{FB} Operating Range Max level	V_{FBmax}	-	-	4.6	V	
Feedback Resistance	R_{FB}	3.0	3.7	4.9	kΩ	
Soft-Start Resistance	$R_{Soft-Start}$	42	50	62	kΩ	

4.4.4 Protection Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over Load & Open Loop Detection Limit	V_{FB2}	4.65	4.8	4.95	V	V_{SoftS} > 5.5V
Activation Limit of Overload & Open Loop Detection	V_{SoftS1}	5.15	5.3	5.46	V	V_{FB} > 5V
Deactivation Limit of Overvoltage Detection	V_{SoftS2}	3.88	4.0	4.12	V	V_{FB} > 5V V_{CC} > 17.5V
Overvoltage Detection Limit	V_{VCC1}	16	16.5	17.2	V	V_{SoftS} < 3.8V V_{FB} > 5V
Latched Thermal Shutdown	T_{jSD}	130	140	150	°C	1)
Spike Blanking	t_{Spike}	-	5	-	µs	

1) The parameter is not subject to production test - verified by design/characterization

4.4.5 Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay Time)	V_{csth}	0.95	1.0	1.05	V	dV_{sense} / dt = 0.6V/ms
Leading Edge Blanking	t_{LEB}	-	220	-	ns	

4.4.6 CoolMOS™ Section

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Drain Source Breakdown Voltage ICE2A0565/165/265/365/765I/765P2 ICE2B0565/165/265/365/765I/765P2 ICE2A0565G/0565Z		$V_{(BR)DSS}$	600 650	- -	- -	V V	T_j=25°C T_j=110°C
Drain Source Breakdown Voltage ICE2A180Z/280Z/380P2		$V_{(BR)DSS}$	800 870	- -	- -	V V	T_j=25°C T_j=110°C
Drain Source On-Resistance	ICE2A0565	R_{DSon1}	- -	4.7 10.0	5.5 12.5	Ω Ω	T_j=25°C T_j=125°C
	ICE2A165	R_{DSon2}	- -	3 6.6	3.3 7.3	Ω Ω	T_j=25°C T_j=125°C
	ICE2A265	R_{DSon3}	- -	0.9 1.9	1.08 2.28	Ω Ω	T_j=25°C T_j=125°C
	ICE2A365	R_{DSon4}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2B0565	R_{DSon5}	- -	4.7 10.0	5.5 12.5	Ω Ω	T_j=25°C T_j=125°C
	ICE2B165	R_{DSon6}	- -	3 6.6	3.3 7.3	Ω Ω	T_j=25°C T_j=125°C
	ICE2B265	R_{DSon7}	- -	0.9 1.9	1.08 2.28	Ω Ω	T_j=25°C T_j=125°C
	ICE2B365	R_{DSon8}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2A0565G	R_{DSon9}	- -	4.7 10.0	5.5 12.5	Ω Ω	T_j=25°C T_j=125°C
	ICE2A0565Z	R_{DSon10}	- -	4.7 10.0	5.5 12.5	Ω Ω	T_j=25°C T_j=125°C
	ICE2A180Z	R_{DSon11}	- -	3 6.6	3.3 7.3	Ω Ω	T_j=25°C T_j=125°C
	ICE2A280Z	R_{DSon12}	- -	0.8 1.7	1.06 2.04	Ω Ω	T_j=25°C T_j=125°C
	ICE2A765I	R_{DSon13}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2B765I	R_{DSon14}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2A765P2	R_{DSon15}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2B765P2	R_{DSon16}	- -	0.45 0.95	0.54 1.14	Ω Ω	T_j=25°C T_j=125°C
	ICE2A380P2	R_{DSon17}	- -	1.89 4.15	2.27 4.98	Ω Ω	T_j=25°C T_j=125°C

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Effective output capacitance, energy related	ICE2A0565	$C_{o(er)1}$	-	4.751	-	pF	V_{DS} =0V to 480V
	ICE2A165	$C_{o(er)2}$	-	7	-	pF	
	ICE2A265	$C_{o(er)3}$	-	21	-	pF	
	ICE2A365	$C_{o(er)4}$	-	30	-	pF	
	ICE2B0565	$C_{o(er)5}$	-	4.751	-	pF	
	ICE2B165	$C_{o(er)6}$	-	7	-	pF	
	ICE2B265	$C_{o(er)7}$	-	21	-	pF	
	ICE2B365	$C_{o(er)8}$	-	30	-	pF	
	ICE2A0565G	$C_{o(er)9}$	-	4.751	-	pF	
	ICE2A0565Z	$C_{o(er)10}$	-	4.751	-	pF	
	ICE2A180Z	$C_{o(er)11}$	-	7	-	pF	
	ICE2A280Z	$C_{o(er)12}$	-	22	-	pF	
	ICE2A765I	$C_{o(er)13}$	-	30	-	pF	
	ICE2B765I	$C_{o(er)14}$	-	30	-	pF	
	ICE2A765P2	$C_{o(er)15}$	-	30	-	pF	
	ICE2B765P2	$C_{o(er)16}$	-	30	-	pF	
	ICE2A380P2	$C_{o(er)17}$	-	16.8	-	pF	
Zero Gate Voltage Drain Current		I_{DSS}	-	0.5	-	µA	V_{VCC}=0V
Rise Time		t_{rise}	-	30[1)]	-	ns	
Fall Time		t_{fall}	-	30[1)]	-	ns	

1) Measured in a Typical Flyback Converter Application

5 Typical Performance Characteristics

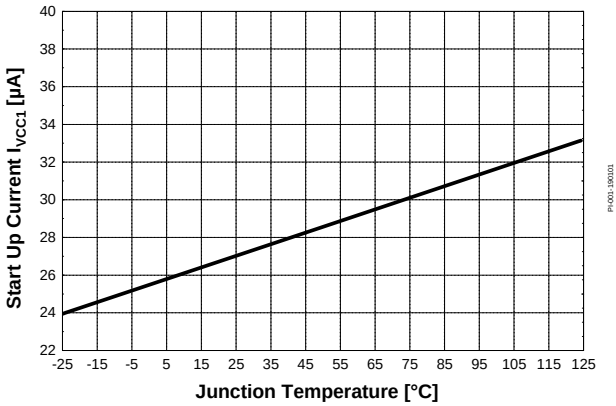


Figure 25 Start Up Current I_{VCC1} vs. T_j

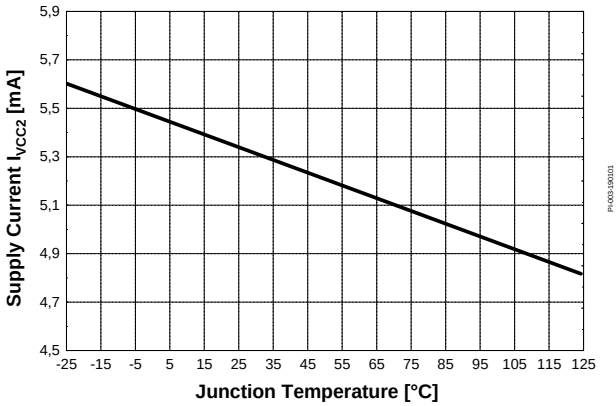


Figure 26 Static Supply Current I_{VCC2} vs. T_j

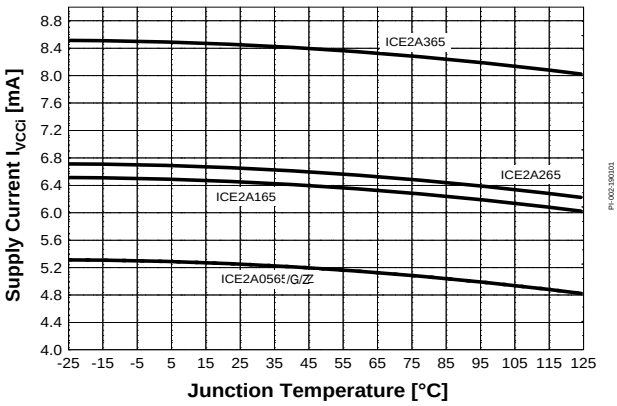


Figure 27 Supply Current I_{VCCI} vs. T_j

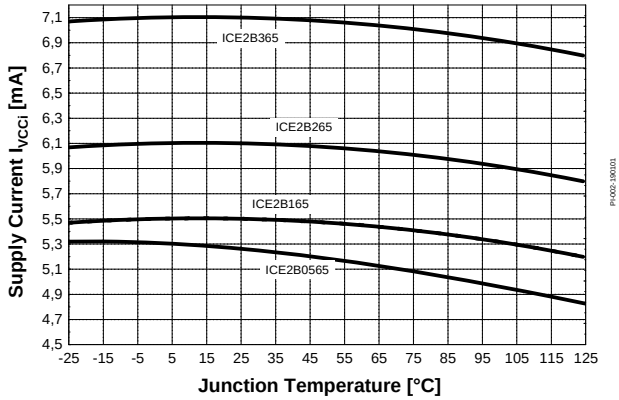


Figure 28 Supply Current I_{VCCI} vs. T_j

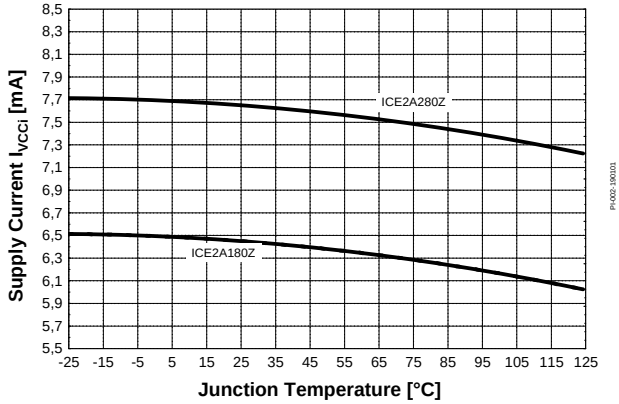


Figure 29 Supply Current I_{VCCI} vs. T_j

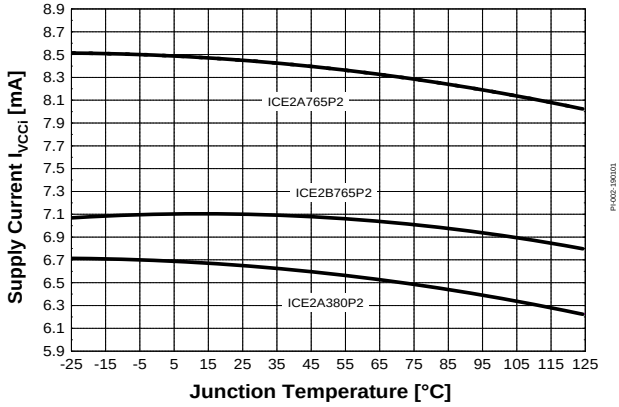


Figure 30 Supply Current I_{VCCI} vs. T_j

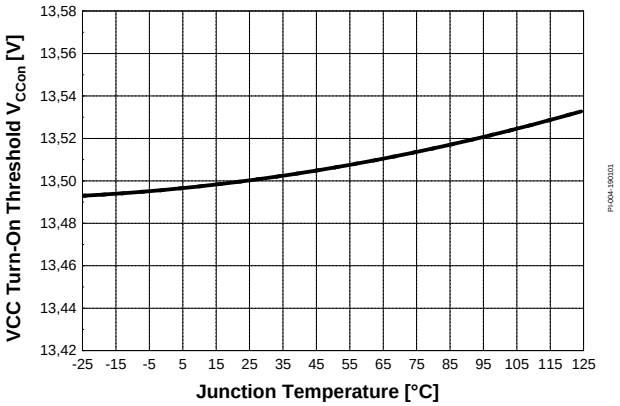


Figure 31 VCC Turn-On Threshold V_{CCon} vs. T_j

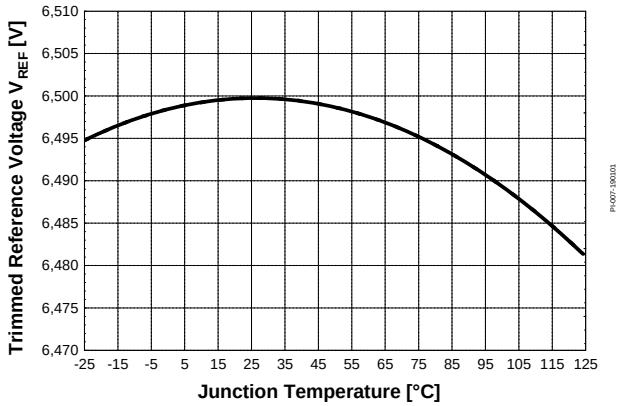


Figure 34 Trimmed Reference V_{REF} vs. T_j

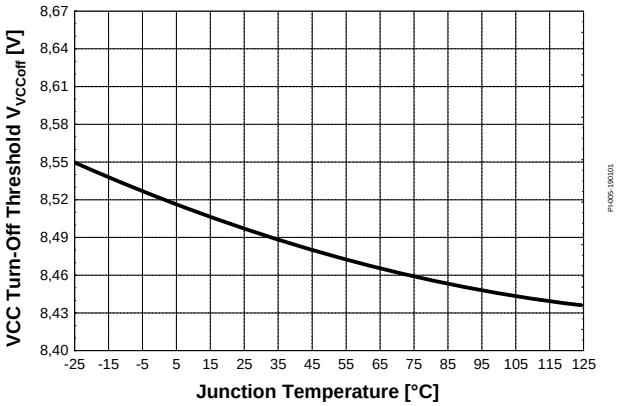


Figure 32 VCC Turn-Off Threshold V_{VCCoff} vs. T_j

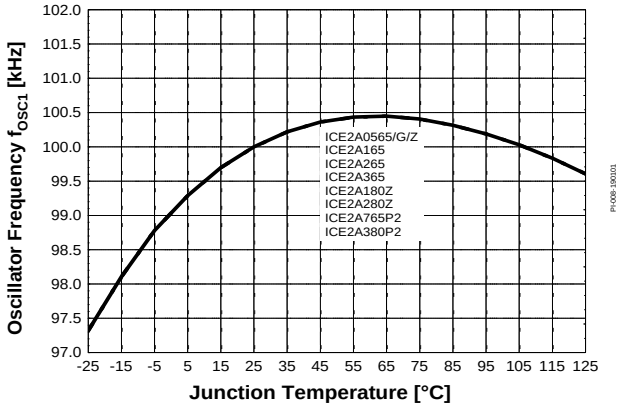


Figure 35 Oscillator Frequency f_{OSC1} vs. T_j

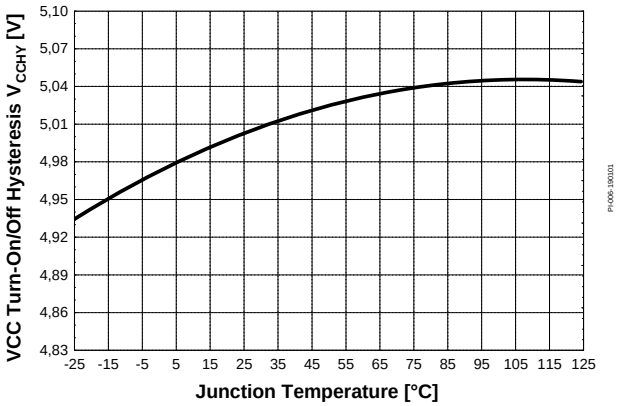


Figure 33 VCC Turn-On/Off Hysteresis V_{VCCHY} vs. T_j

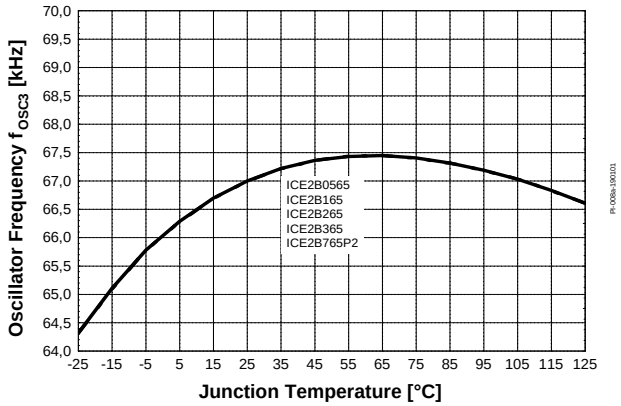


Figure 36 Oscillator Frequency f_{OSC3} vs. T_j

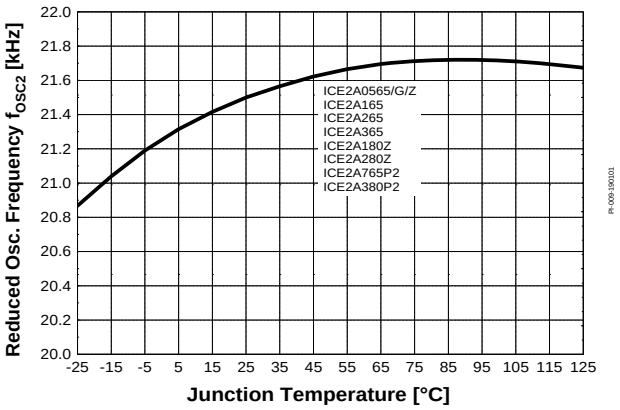


Figure 37 Reduced Osc. Frequency f_{OSC2} vs. T_j

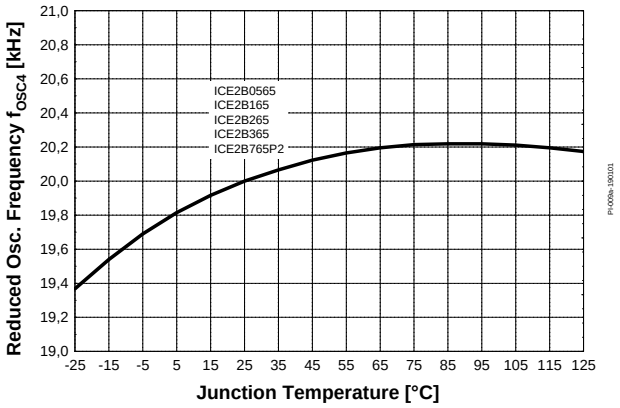


Figure 38 Reduced Osc. Frequency f_{OSC4} vs. T_j

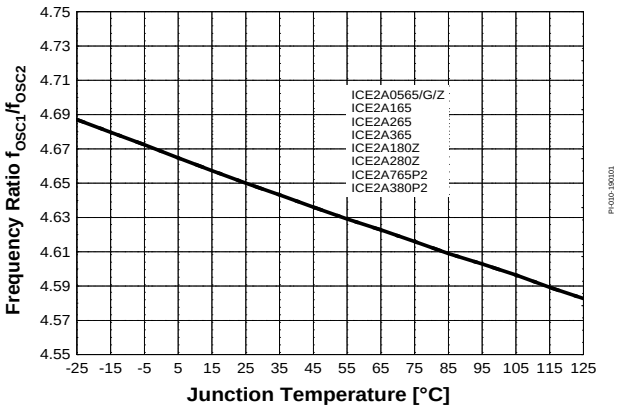


Figure 39 Frequency Ratio f_{OSC1} / f_{OSC2} vs. T_j

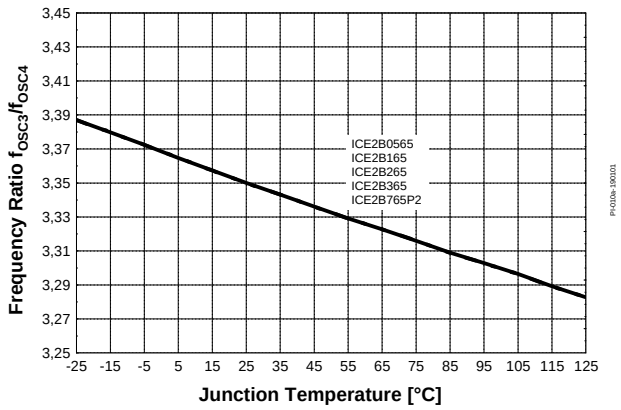


Figure 40 Frequency Ratio f_{OSC3} / f_{OSC4} vs. T_j

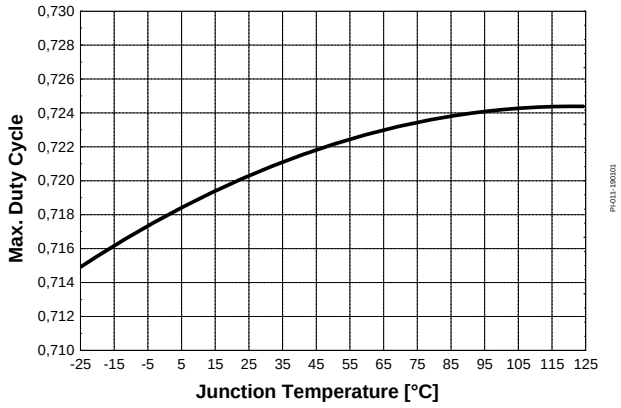


Figure 41 Max. Duty Cycle vs. T_j

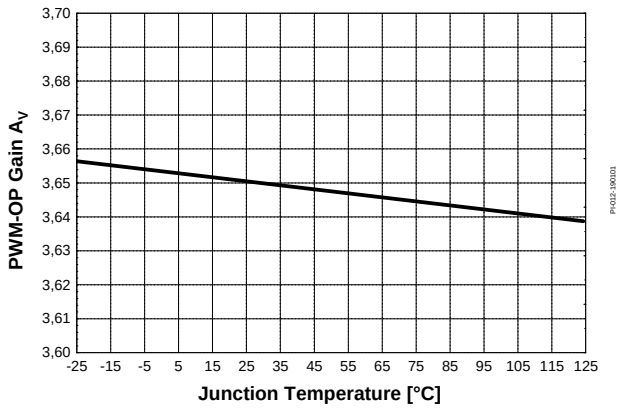


Figure 42 PWM-OP Gain A_V vs. T_j

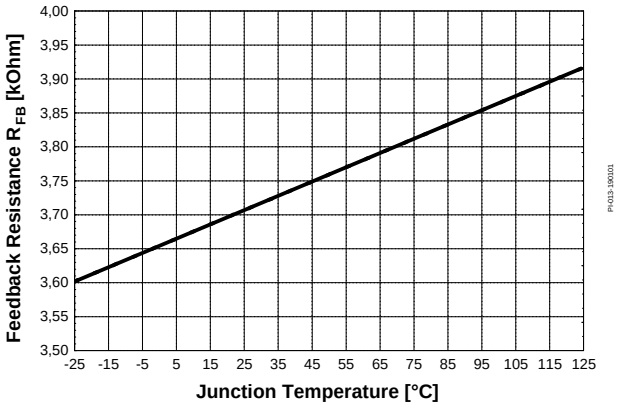


Figure 43 Feedback Resistance R_{FB} vs. T_j

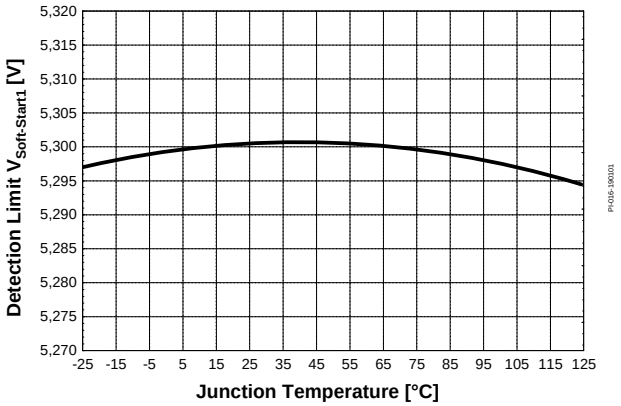


Figure 46 Detection Limit $V_{Soft-Start1}$ vs. T_j

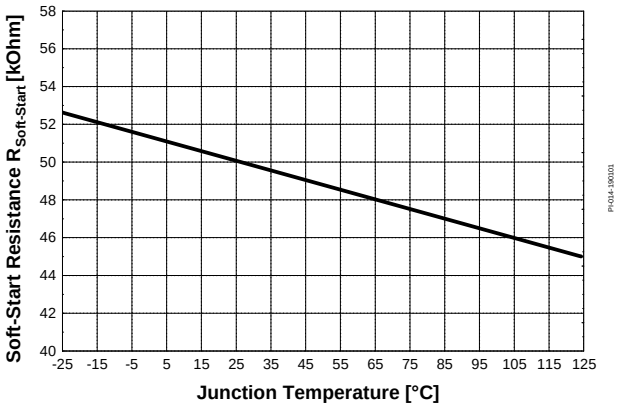


Figure 44 Soft-Start Resistance $R_{Soft-Start}$ vs. T_j

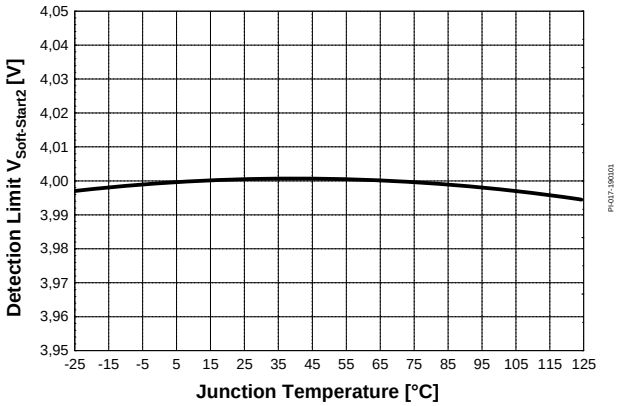


Figure 47 Detection Limit $V_{Soft-Start2}$ vs. T_j

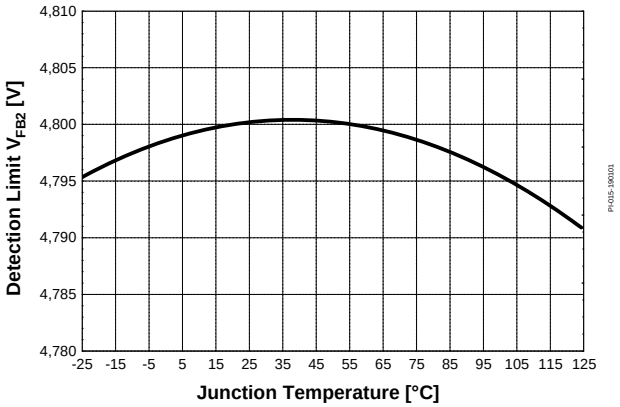


Figure 45 Detection Limit V_{FB2} vs. T_j

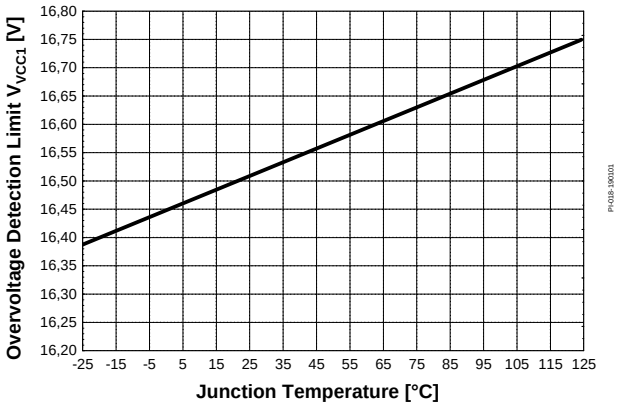


Figure 48 Overvoltage Detection Limit V_{VCC1} vs. T_j

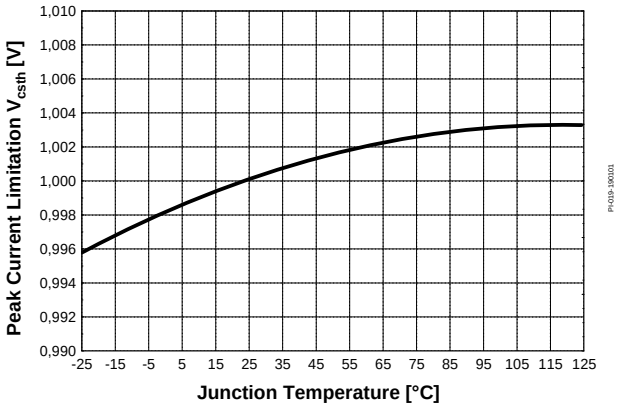


Figure 49 Peak Current Limitation V_{csth} vs. T_j

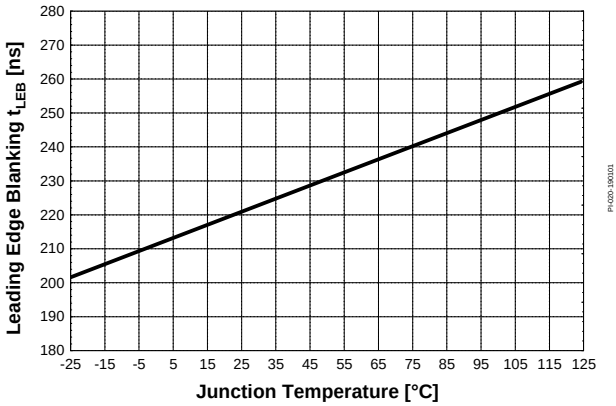


Figure 50 Leading Edge Blanking V_{VCC1} vs. T_j

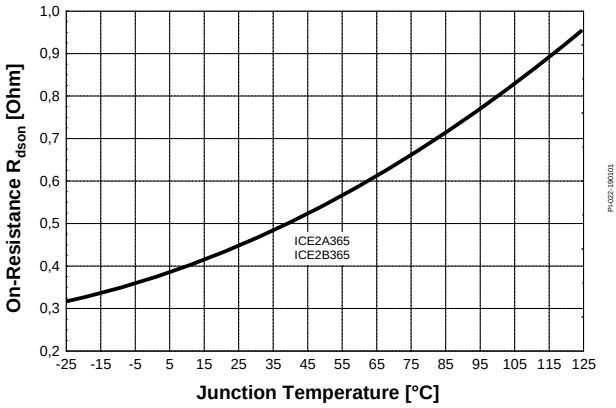


Figure 51 Drain Source On-Resistance R_{DSon} vs. T_j

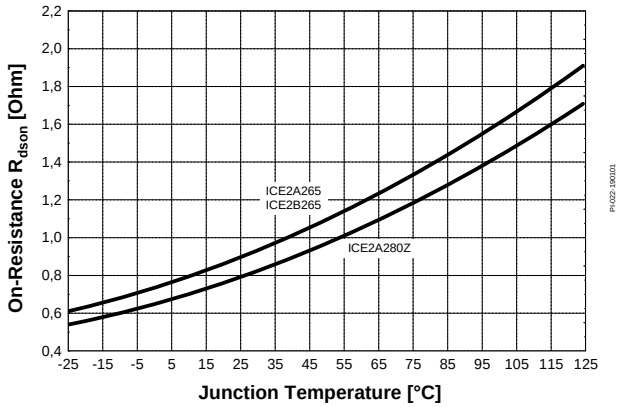


Figure 52 Drain Source On-Resistance R_{DSon} vs. T_j

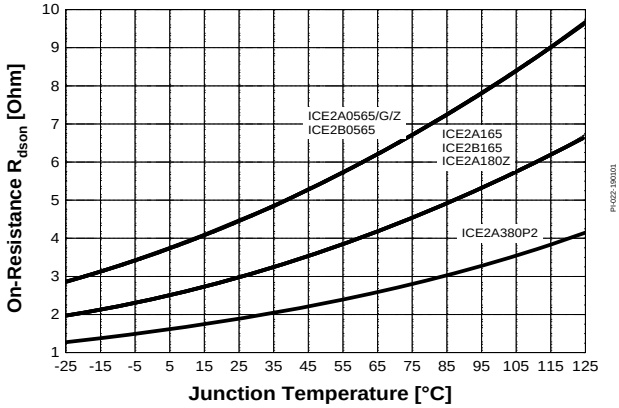


Figure 53 Drain Source On-Resistance R_{DSon} vs. T_j

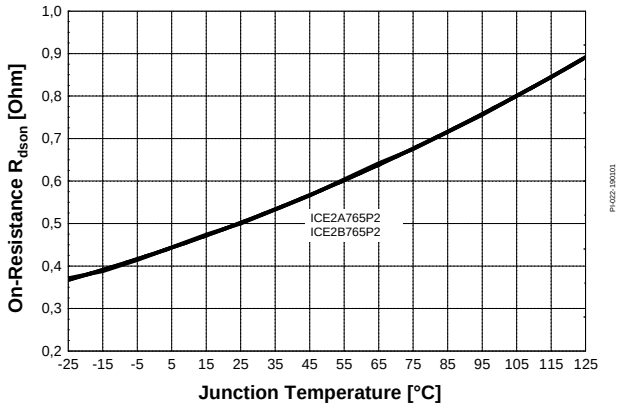


Figure 54 Drain Source On-Resistance R_{DSon} vs. T_j

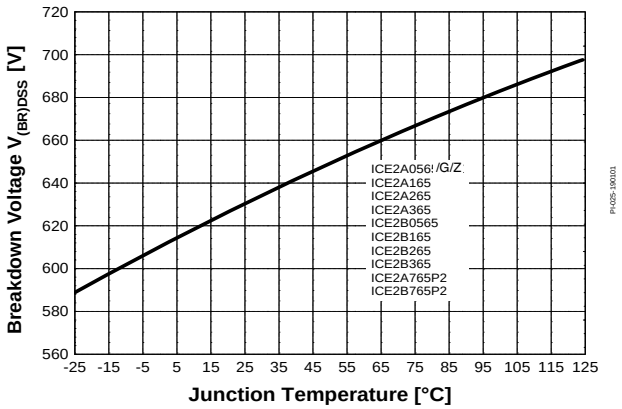


Figure 55 Breakdown Voltage $V_{BR(DSS)}$ vs. T_j

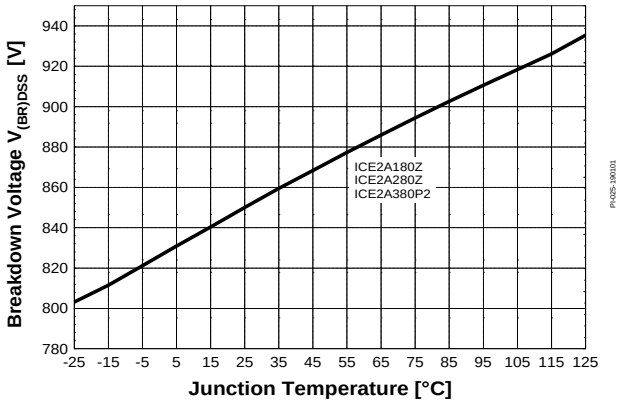


Figure 56 Breakdown Voltage $V_{BR(DSS)}$ vs. T_j

6 Layout Recommendation for C_{18}

Note: Only for ICE2A765I/P2 and ICE2B765I/P2

Soft Start Capacitor Layout Recommendation in Detail

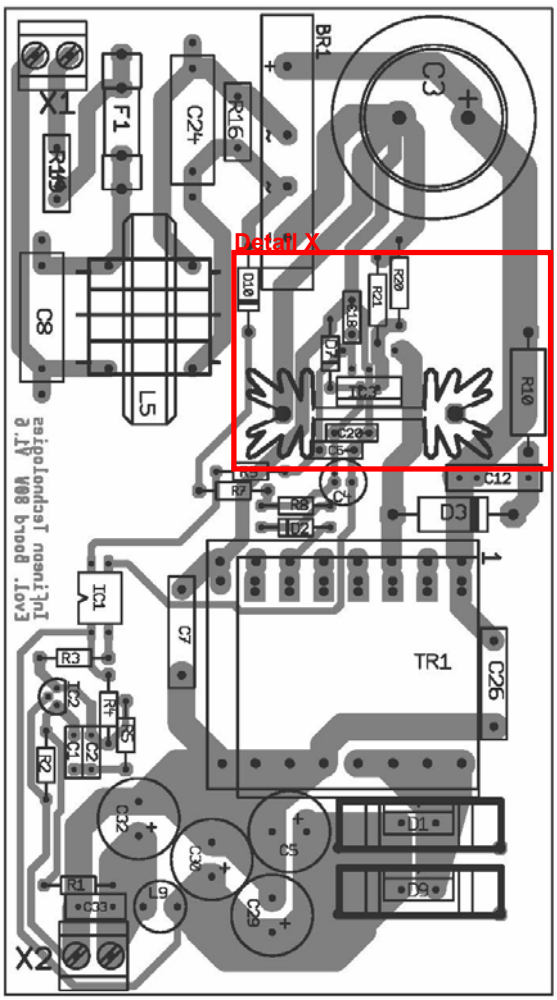


Figure 57A Layout of Board EVALSF2_ICE2B765P2

To improve the startup behavior of the IC during startup or auto restart mode, place the soft start capacitor C_{18} (red section Detail X in Figure 57A) as close as possible to the soft start PIN 6 and GND PIN 4. More details see Detail X in Figure 57B.

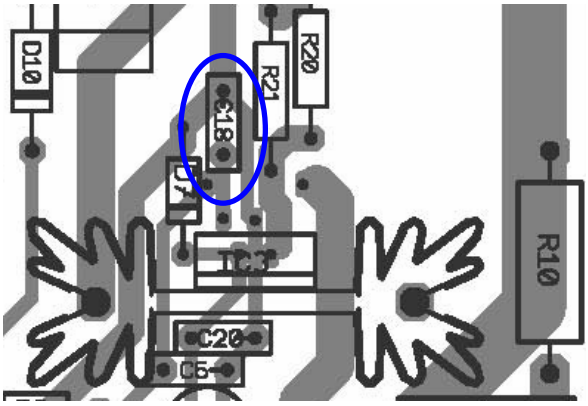


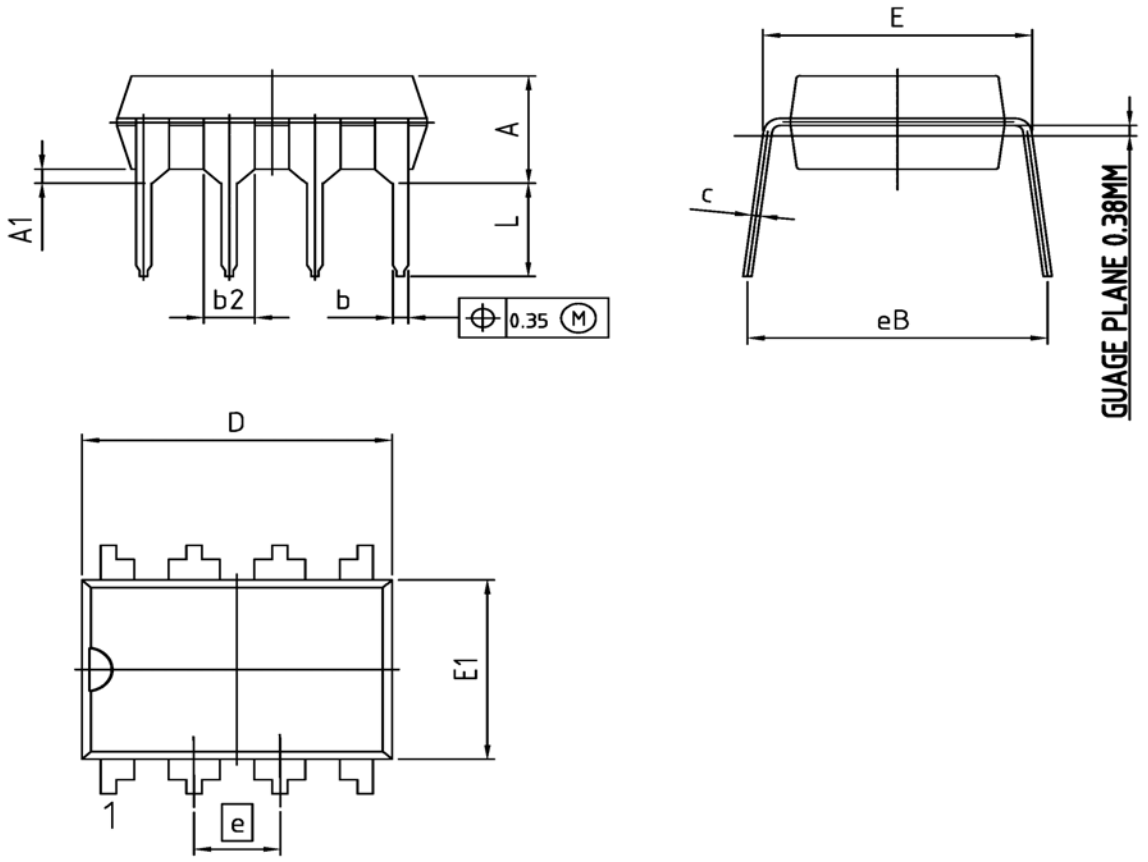
Figure 57B Detail X, Soft Start Capacitor C_{18} Layout Recommendation

Place Soft Start capacitor C_{18} in the same way as shown in Detail X (blue mark).

Figure 57 Layout Recommendation for ICE2A765I/P2 and ICE2B765I/P2

7 Outline Dimension

PG-DIP-8



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.80	-	0.189
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.70	-	0.067
c	0.15	0.36	0.006	0.014
D	9.10	9.77	0.358	0.385
E	7.49	8.26	0.295	0.325
E1	6.10	6.60	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	8		8	
eB	7.90	9.90	0.311	0.390
L	3.00	-	0.118	-

DOCUMENT NO.
Z8B00155363

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
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REVISION
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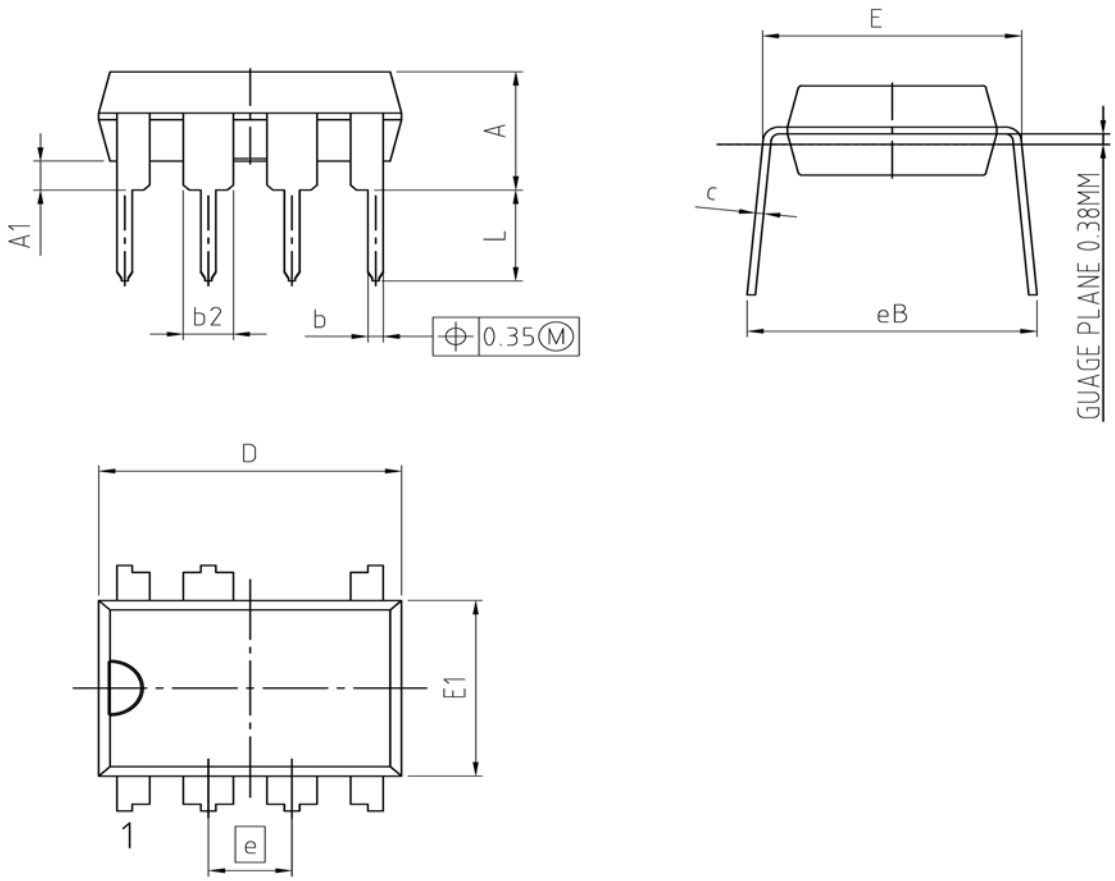
Figure 58 PG-DIP-8 (Plastic Dual In-line Package)

PG-DIP-7-1
(Plastic Dual In-Line Package)



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.57	-	0.180
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.70	-	0.067
c	0.20	0.36	0.008	0.014
D	9.10	9.77	0.358	0.385
E	7.49	8.26	0.295	0.325
E1	6.10	6.60	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	7		7	
eB	7.90	10.90	0.311	0.429
L	2.92	-	0.115	-

DOCUMENT NO.
Z8B00155542

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
22.07.2011

REVISION
02

Figure 59 PG-DIP-7-1(Plastic Dual In-line Package)

PG-TO220-6-46
Isodrain Package

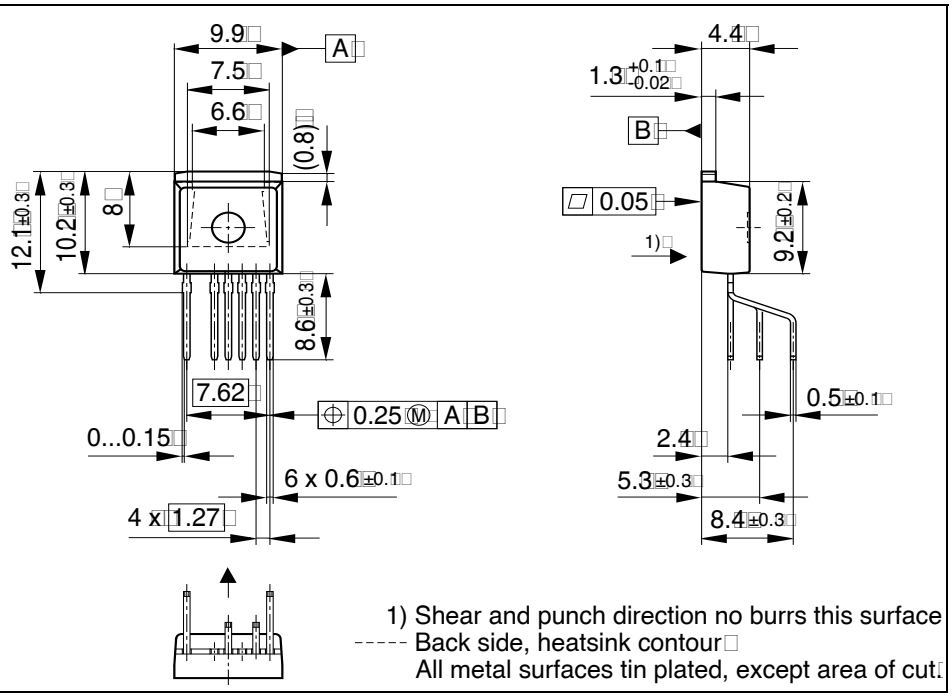


Figure 60 PG-TO220-6-46 (Isodrain Package)

PG-TO220-6-47
Isodrain Package

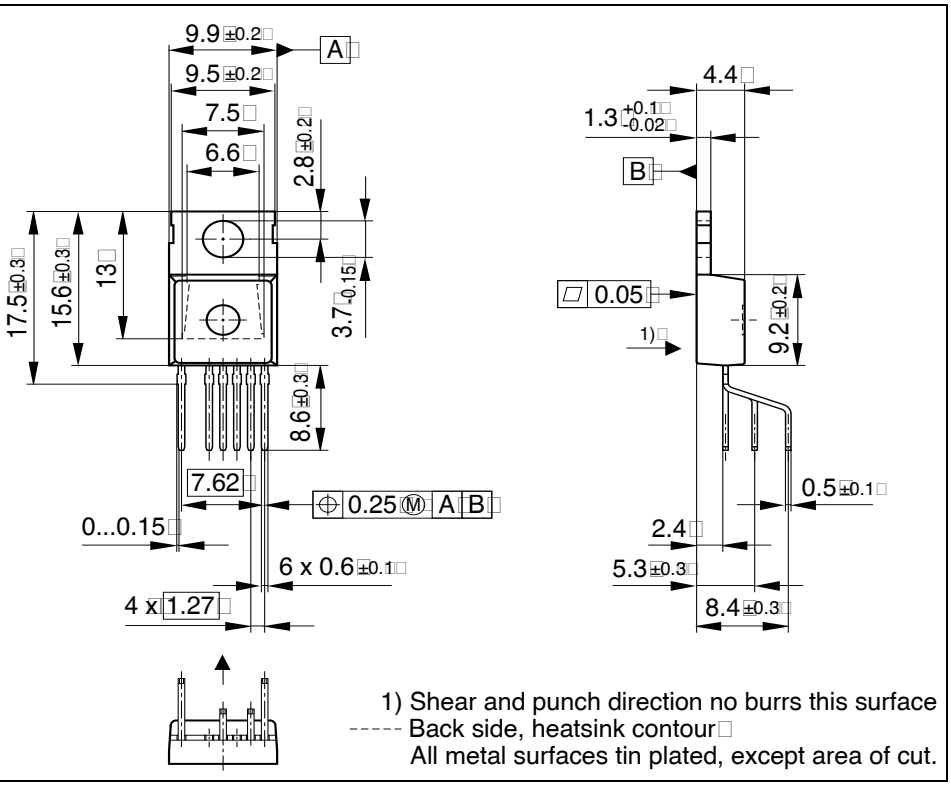
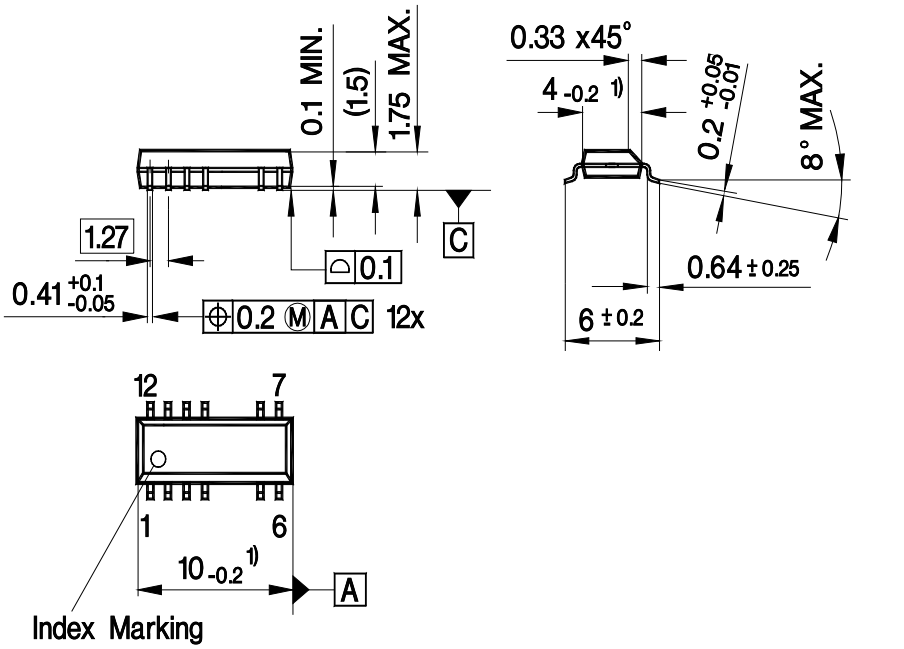


Figure 61 PG-TO220-6-47 (Isodrain Package)

Dimensions in mm

PG-DSO-16/12
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 62 PG-DSO-16/12 (Plastic Dual Small Outline Package)

Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

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Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

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