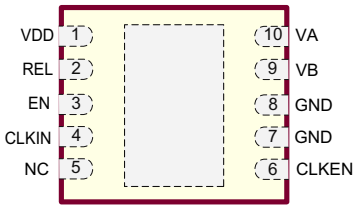
Ordering Information

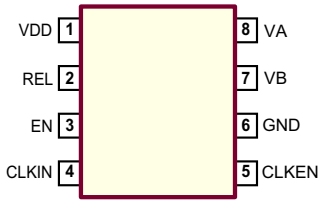
DEVICE	Package Options	
	10-Lead DFN *3.00x3.00mm body* *0.80mm height (max)* *0.50mm pitch*	8-Lead MSOP *3.00x3.00mm body* *1.10mm height (max)* *0.65mm pitch*
HV853	HV853K7-G	HV853MG-G

-G indicates package is RoHS compliant ('Green')

Pin Configurations



10-Lead DFN (K7)
(top View)



8-Lead MSOP (MG)
(top view)

Note: *Pads are at the bottom of the package. Center heat slug should be connected to GND or left floating.*

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

10-Lead DFN (K7)

Top Marking

Bottom Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
____ = "Green" Packaging

8-Lead MSOP(MG)

Absolute Maximum Ratings

Parameter	Value
V_{DD}, supply voltage	-0.5V to 6.5V
Storage temperature	-65°C to +150°C
Power dissipation (10-Lead DFN)	1.6W
Power dissipation (8-Lead MSOP)	300mW

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Input voltage	3.2	-	5.0	V	---
f_{EL}	EL lamp frequency	50	-	500	Hz	---
C_{load}	EL lamp capacitance	0	-	5.3	nF	---
T_A	Operating temperature	-25	-	+85	^{O}C	---

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified, T_A = 25ºC)

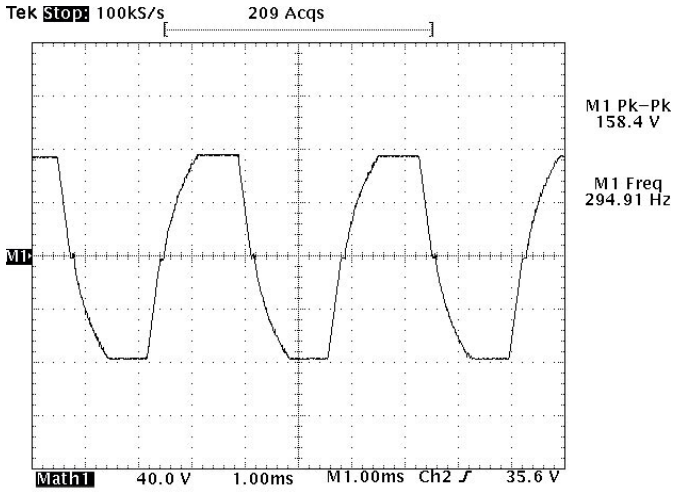
Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{DDQ}	Quiescent current	-	-	150	nA	EN = 0V
V_A or V_B	Peak output voltage	68	80	92	V	No load
V_A-V_B	Peak to peak output voltage	136	160	184	V	
I_{DD}	Operating current	-	15	30	mA	See Figure 1 V_{DD} = 3.5V R_{EL} = 1.5MΩ Load = 3.3nF + 1.0kΩ
V_A or V_B	Peak output voltage	68	80	92	V	
V_A-V_B	Peak to peak output voltage	136	160	184	V	
f_{EL}	EL lamp frequency	240	280	320	Hz	

Electrical Characteristics *(cont.)*

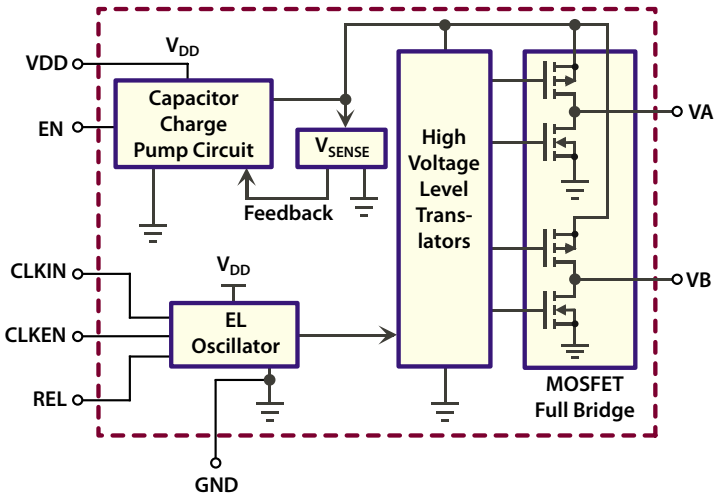
(Over recommended operating conditions unless otherwise specified, T_A = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{rout}	Output voltage rise time	-	450	-	µs	1.0in² lamp 0V to 90% of final value
t_{fout}	Output voltage fall time	150	-	-	µs	90% to 10% of final value
Logic Inputs						
V_{IL}	Input logic low voltage	0	-	0.5	V	---
V_{IH}	Input logic high voltage	2.0	-	V_{DD}	V	---
I_{IL}	Input logic low current	-	-	1.0	µA	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
EN_{rise}	Enable input rise time (for delay turn off)	0.01	-	10	ms	Using external R-C circuit, see Figure 2
EN_{fall}	Enable input fall time (for delay turn off)	10µ	-	5.0	s	
C_{in}	Logic input capacitance	-	-	10	pF	---

Typical Output Waveform



Functional Block Diagram



Typical Performance

(The following was the observed performance when driving a 1.0in² green lamp)

Load	R_{EL} (MΩ)	V_{DD} (V)	I_{DD} (mA)	V_A-V_B (V)	f_{EL} (Hz)
3.3nF + 1.0kΩ	1.5	3.2	13.1	158	294
		3.5	12.9	158	
		3.8	12.7	158	
		4.2	12.5	158	
		5.0	12.3	158	

Figure 1: Typical Application

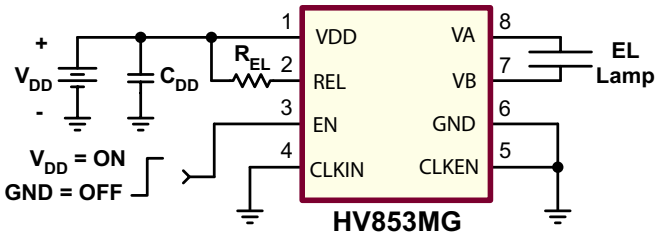


Figure 2: Push Button Turn on with Delay Turn off

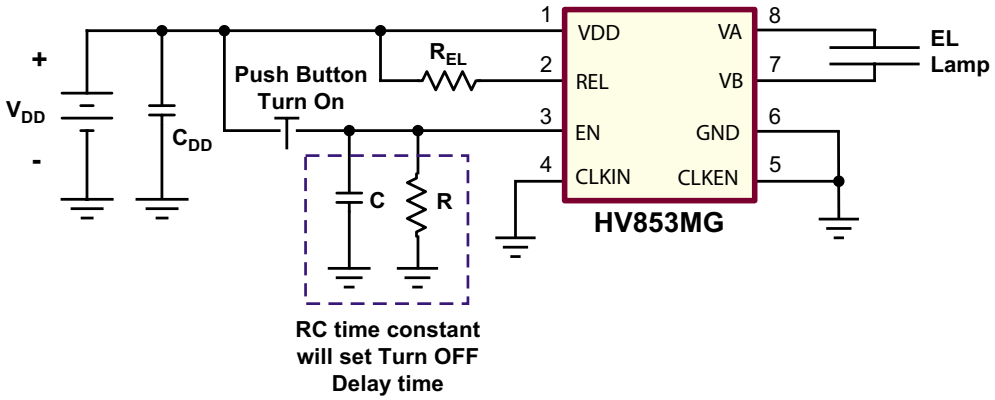
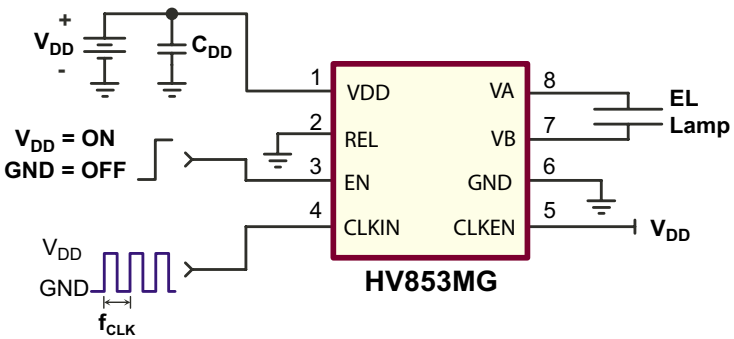


Figure 3: Independent Programmable Output Frequency (f_{EL})

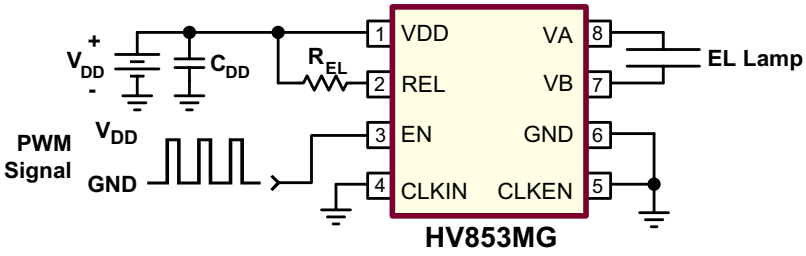


Note: $f_{EL} = f_{CLK}/128$

EL Lamp Dimming Using PWM

EL lamp dimming can be achieved by applying a PWM signal to the ENABLE pin. This is done by pulse skipping the output pulses. The PWM frequency should be kept below the EL frequency but above 50Hz to avoid flickering.

Figure 4: PWM Dimming Circuit

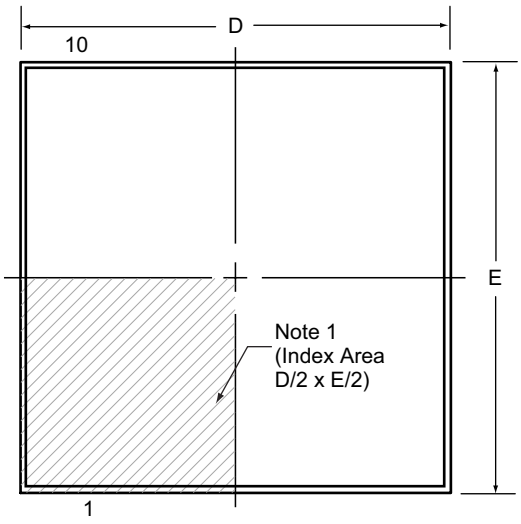


Pin Descriptions: 10-Lead DFN (K7) / 8-Lead MSOP (MG)

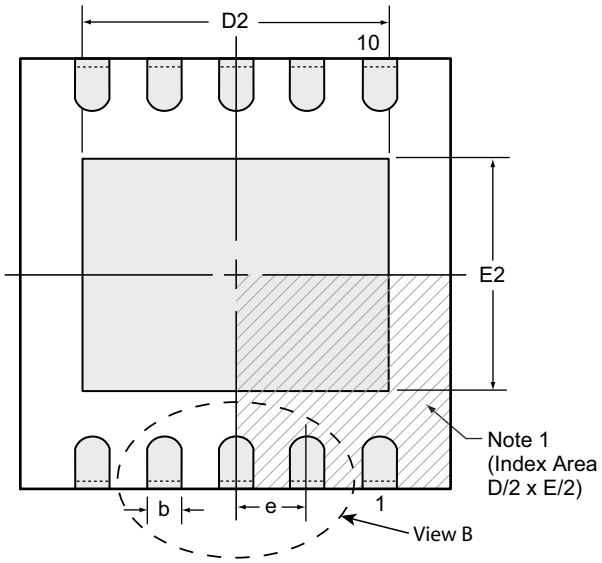
K7 Pin #	MG Pin #	Pin Name	Description
1	1	VDD	Input supply voltage pin.
2	2	REL	An external resistor to VDD will set the EL lamp frequency. The EL frequency is inversely proportional to the R_{EL} resistor value. A 1.5MΩ resistor would provide a nominal lamp frequency of 280Hz $f_{EL} = (1.5M\Omega)(280Hz) / (R_{EL})$ When using an external clock to set the EL lamp frequency, the REL pin should be connected to ground.
3	3	EN	Enable input pin. Logic high will turn the device on. An external R-C circuit can be added for a delayed turn off.
4	4	CLKIN	Logic input pin. An external logic clock applied to this pin can be used to set the EL lamp frequency (see Figure 3). The EL lamp frequency is the external clock frequency divided by 128. This is useful for applications requiring the EL lamp to be synchronized to a system clock. Connect to ground when not in use.
5	-	NC	No connect.
6	5	CLKEN	Logic input pin. Logic high will cause the EL lamp frequency to be set by the CLKIN input. Logic low will cause the EL lamp frequency to be set by the external R_{EL} resistor.
7,8	6	GND	IC ground pin.
9	7	VB	EL lamp driver output pin. The EL lamp is connected across VA and VB terminals.
10	8	VA	EL lamp driver output pin. The EL lamp is connected across VA and VB terminals.

10-Lead DFN Package Outline (K7)

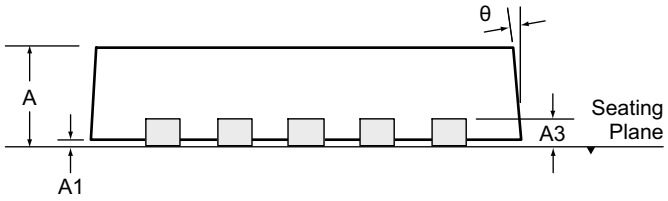
3.00x3.00mm body, 0.80mm height (max), 0.50mm pitch



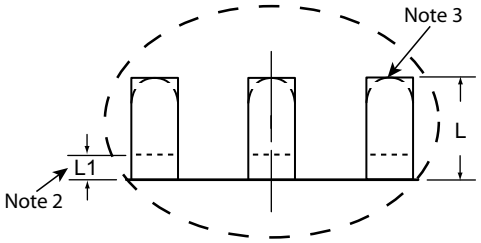
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

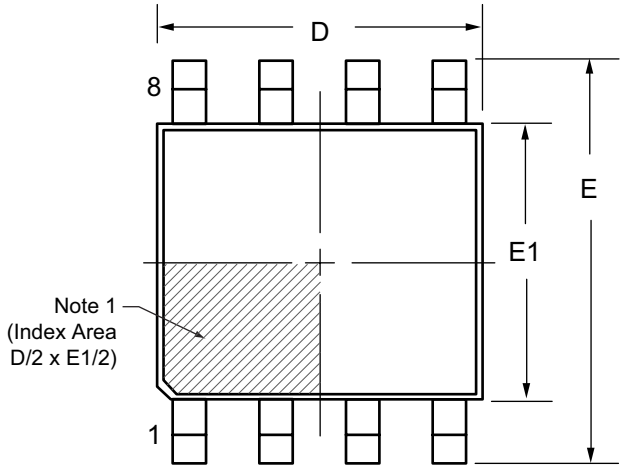
Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85*	2.20	2.85*	1.40	0.50 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15*	2.70	3.15*	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEED-5, Issue C, Aug. 2003.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

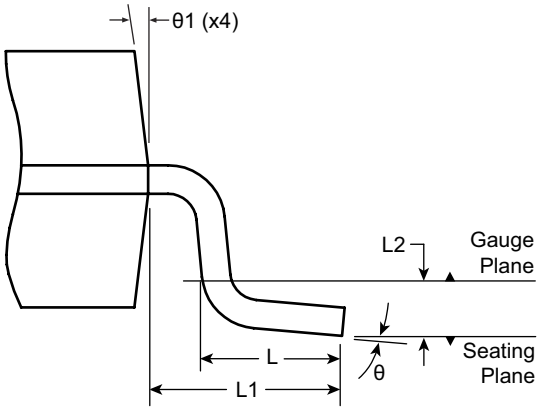
Drawings not to scale.
Supertex Doc.#: *DSPD-10DFNK73X3P050, Version C101008.*

8-Lead MSOP Package Outline (MG)

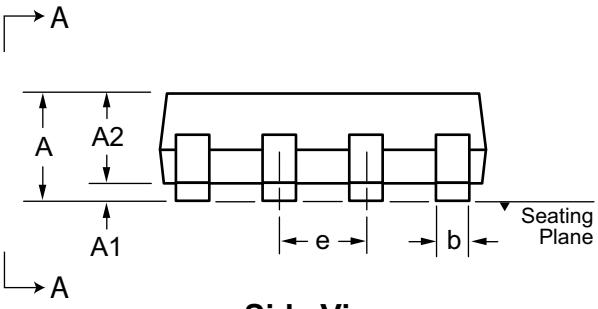
3.00x3.00mm body, 1.10mm height (max), 0.65mm pitch



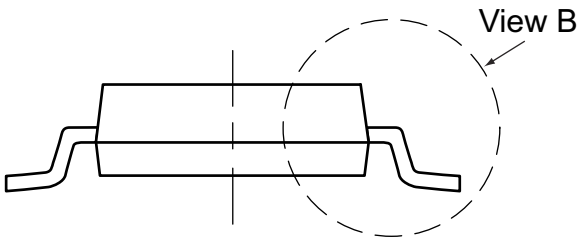
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.22	2.80*	4.65*	2.80*	0.65 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.38	3.20*	5.15*	3.20*		0.80			8°	15°

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-8MSOPMG, Version G101008.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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