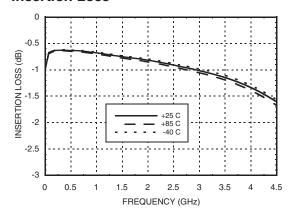




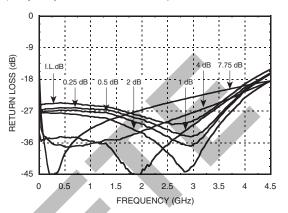
# 0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

#### Insertion Loss



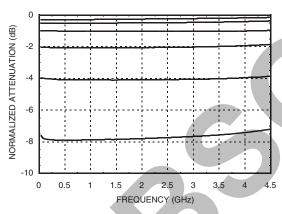
# Return Loss RF1, RF2

(Only Major States are Shown)

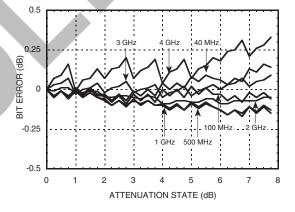


## **Normalized Attenuation**

(Only Major States are Shown)

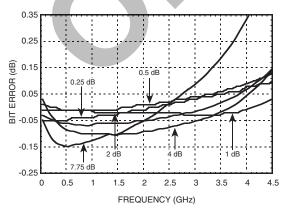


#### Bit Error vs. Attenuation State



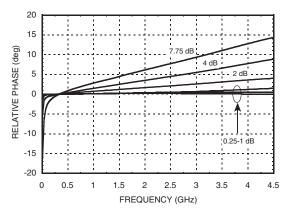
# Bit Error vs. Frequency

(Only Major States are Shown)



# Relative Phase vs. Frequency

(Only Major States are Shown)



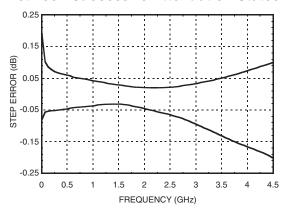


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# 0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

### Worst Case Step Error Between Successive Attenuation States



# Bias Voltage & Current

Vdd = +5.0 Vdc ± 10%			
Vdd (VDC)	Idd (Typ.) (mA)		
+4.5	3.3		
+5.0	3.5		
+5.5	3.7		

# **Control Voltage**

State	Bias Condition
Low	0 to +0.8V @ -5 uA Typ.
High	+2.0 to + 5.0 Vdc @ 30 uA Typ.
Note: Vdd = +5V	

#### **Truth Table**

Control Voltage Input				Attenuation	
V1 4 dB	V2 2 dB	V3 1 dB	V4 0.5 dB	V5 0.25 dB	State RF1 - RF2
High	High	High	High	High	Reference I.L.
High	High	High	High	Low	0.25 dB
High	High	High	Low	High	0.5 dB
High	High	Low	High	High	1 dB
High	Low	High	High	High	2 dB
Low	High	High	High	High	4 dB
Low	Low	Low	Low	Low	7.75 dB

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.





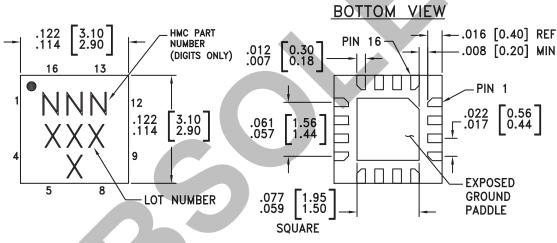
# 0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

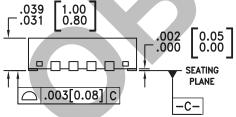
### **Absolute Maximum Ratings**

RF Input Power (DC - 4 GHz)	+29 dBm (T = +85 °C)
Control Voltage Range (V1 to V5)	-1V to Vdd +1V
Bias Voltage (Vdd)	+7.0 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 12.0 mW/°C above 85 °C)	0.781 W
Thermal Resistance	83 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A



### **Outline Drawing**





#### NOTES:

- 1. LEADFRAME MATERIAL: COPPER ALLOY
- 2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
- 3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- 4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- 5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- 6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

#### Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC539LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	539 XXXX
HMC539LP3E RoHS-compliant Low Stress Injection Molded Plastic		100% matte Sn	MSL1 [2]	<u>539</u> XXXX

- [1] Max peak reflow temperature of 235  $^{\circ}\text{C}$
- [2] Max peak reflow temperature of 260 °C
- [3] 4-Digit lot number XXXX



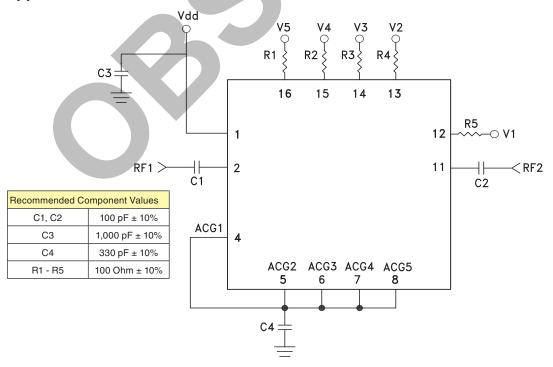


# 0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

### **Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 11	RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation.	RF1 RF2
3, 9, 10	N/C	These pins should be connected to PCB RF ground to maximize performance.	
4 - 8	ACG1 - ACG5	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
12 - 16	V1 - V5	See truth table and control voltage table.	500 142K (V1-V5) =
	GND	Package bottom has an exposed metal paddle that must be connected to RF Ground.	GND =

# **Application Circuit**

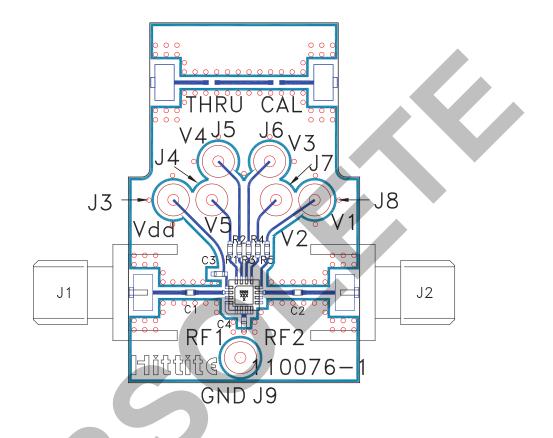




RoHS (E)

# 0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

#### **Evaluation PCB**



### List of Materials for Evaluation PCB 110078 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3 - J9	DC Pin
C1, C2	100 pF Capacitor, 0402 Pkg.
C3	1000 pF Capacitor, 0402 Pkg.
C4	330 pF Capacitor, 0402 Pkg.
R1 - R5	100 Ohm Resistor 0402
U1	HMC539LP3 / HMC539LP3E Digital Attenuator
PCB [2]	110076 Evaluation PCB

<sup>[1]</sup> Reference this number when ordering complete evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

<sup>[2]</sup> Circuit Board Material: Rogers 4350