

Contents

1 **Pin information** 3

2 **Functional description** 4

3 **Electrical characteristics** 7

4 **Package information** 13

 4.1 PDIP-16 package information 13

 4.2 SO-16 package information 14

5 **Ordering information** 16

6 **Revision history** 16



1 Pin information

Figure 1. Pin connections (top view)

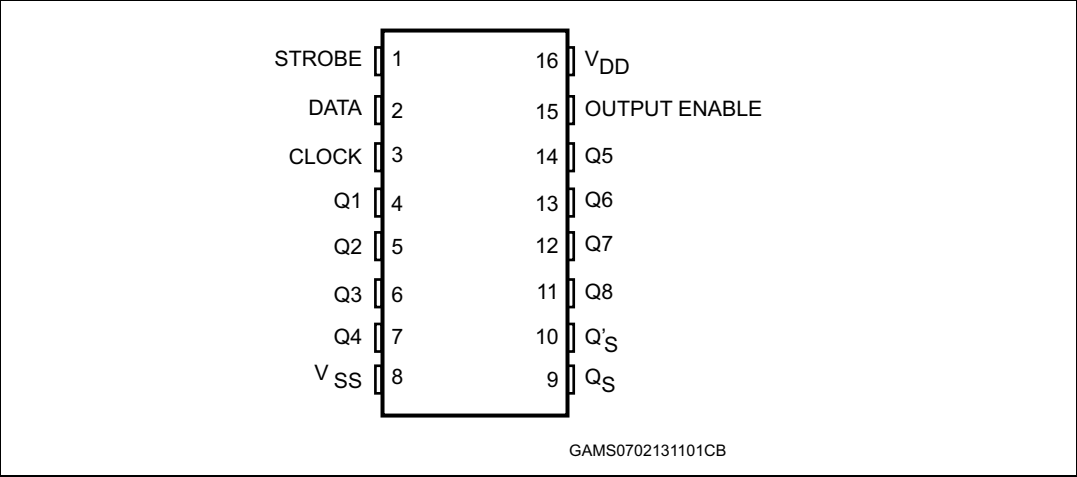


Table 2. Pin description

Pin no	Symbol	Name and function
2	DATA	Data input
1	STROBE	Strobe input
3	CLOCK	Clock input
9, 10	Q _S , Q' _S	Serial outputs
4, 5, 6, 7, 14, 13, 12, 11	Q1 to Q8	Parallel outputs
15	OUTPUT ENABLE	Output enable input
8	V _{SS}	Negative supply voltage
16	V _{DD}	Positive supply voltage

2 Functional description

Figure 2. Logic diagram

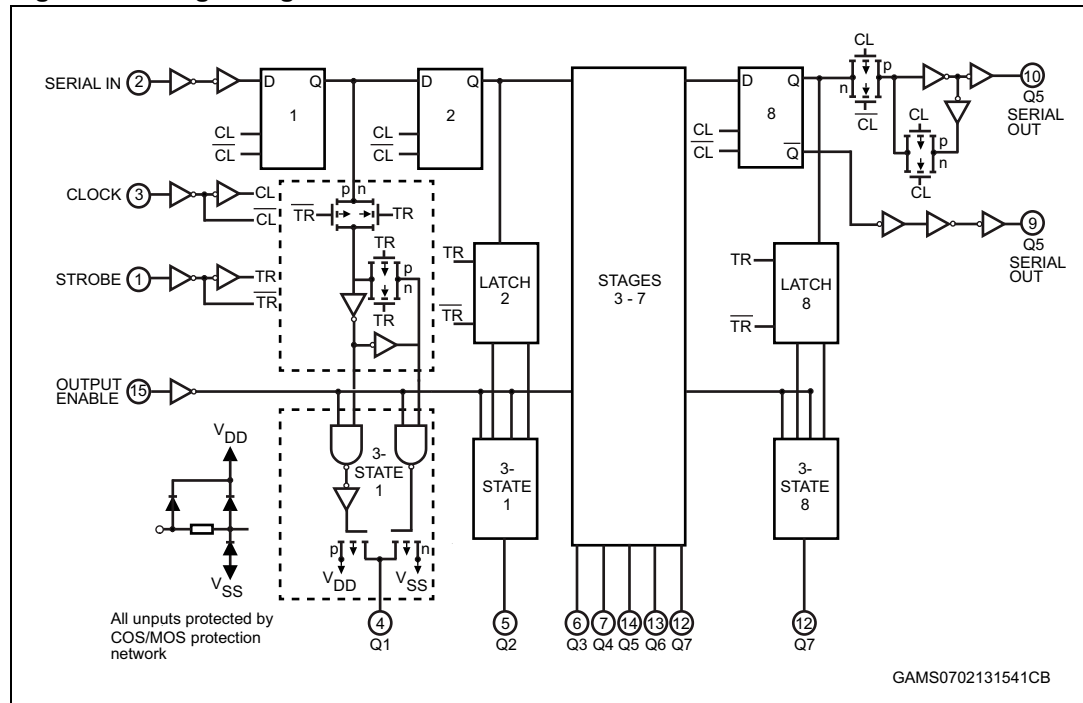








Table 3. Truth table

Clock	Output enable	Strobe	Data	Parallel outputs		Serial outputs	
				Q ₁	Q _n	Q _S ⁽¹⁾	Q' _S
	L	X ⁽²⁾	X ⁽²⁾	OC ⁽³⁾	OC ⁽³⁾	Q7	No change
	L	X ⁽²⁾	X ⁽²⁾	OC ⁽³⁾	OC ⁽³⁾	No change	Q7
	H	L	X ⁽²⁾	No change	No change	Q7	No change
	H	H	L	L	Q _n -1	Q7	No change
	H	H	H	H	Q _n -1	Q7	No change
	H	H	H	No change	No change	No change	Q7

1. At the positive clock edge, information on the 7th shift register stage is transferred to the 8th register stage and the Q_S output.
2. Don't care
3. Open circuit

Figure 3. Functional diagram

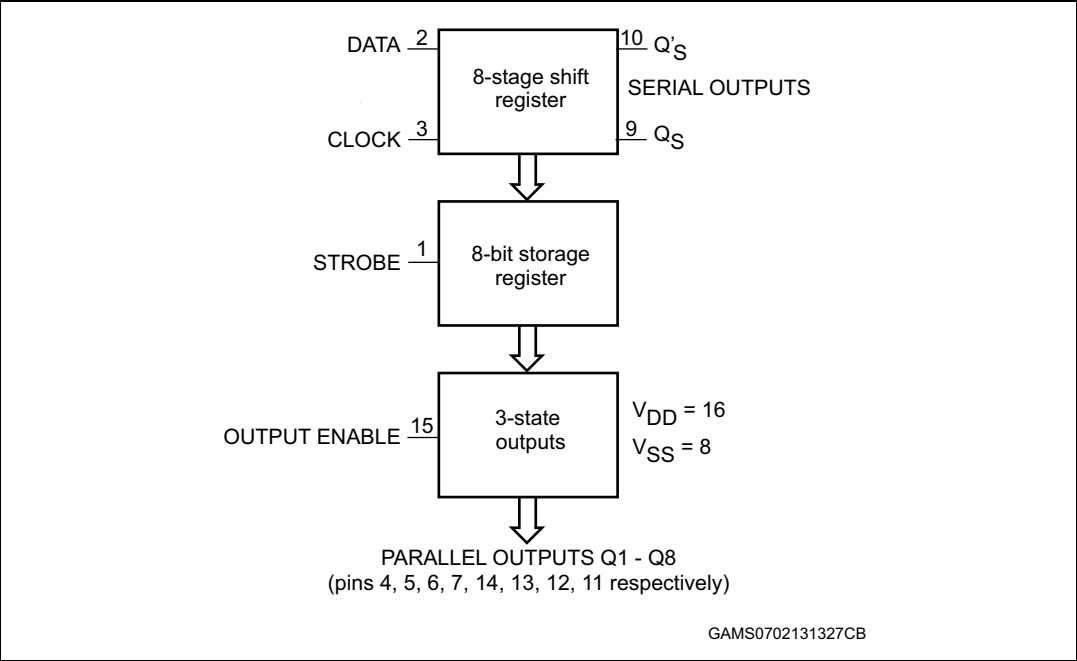


Figure 4. Input equivalent circuit

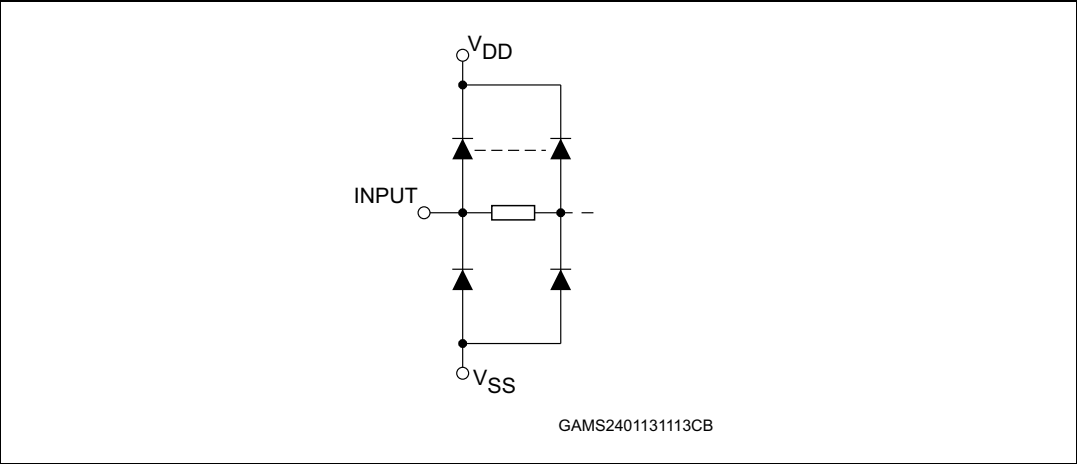
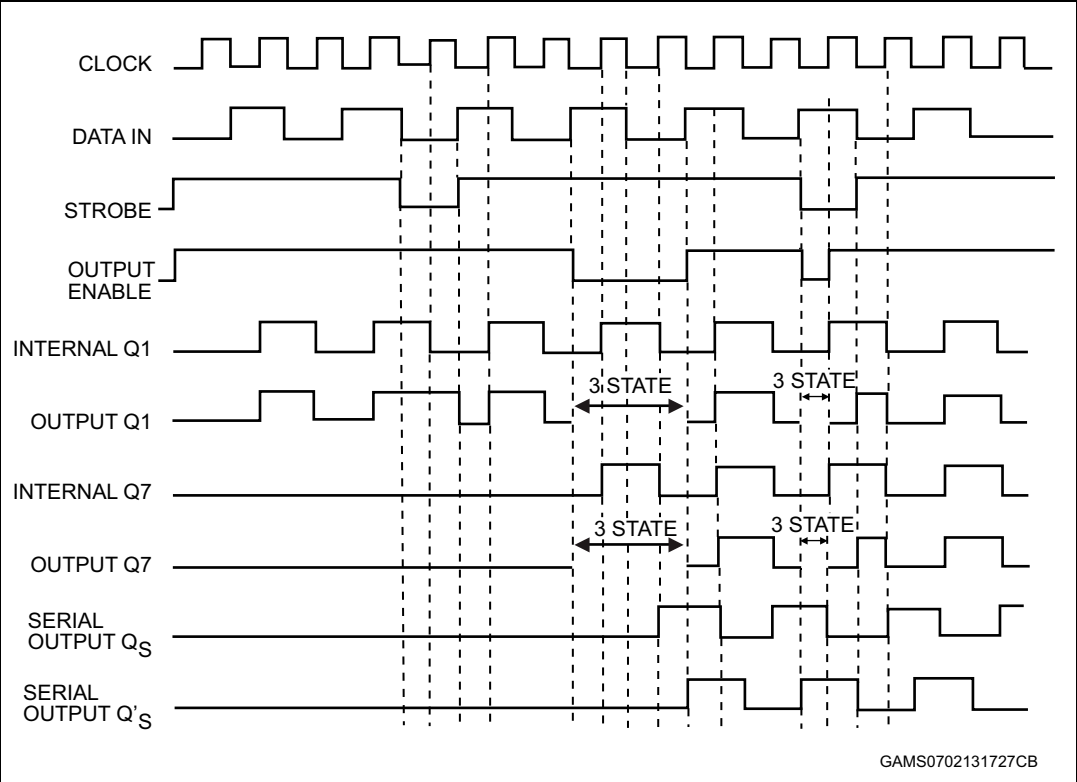


Figure 5. Timing chart



3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to V_{SS} pin voltage.

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to $V_{DD} + 0.5$	
I_I	DC input current	± 10	mA
P_D	Power dissipation per package	500 ⁽¹⁾	mW
	Power dissipation per output transistor	100	
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	

1. 500 mW at 65 °C; lower to 300 mW by 10 mW/°C from 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	
T_{op}	Operating temperature	-55 to 125	°C

Table 6. DC specifications⁽¹⁾

Sym.	Parameter	Test condition				Value							Unit
		V _I (V)	V _O (V)	I _{OL} (μA)	V _{DD} (V)	T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _L	Quiescent current	0/5			5			5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15			20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10			10	9.95			9.95		9.95		
		0/15			15	14.95			14.95		14.95		
V _{OL}	Low level output voltage	5/0		<1	5		0.05			0.05		0.05	
		10/0			10								
		15/0			15								
V _{IH}	High level input voltage		0.5/4.5	<1	5	3.5			3.5		3.5		
			1/9		10	7			7		7		
			1.5/13.5		15	11			11		11		
V _{IL}	Low level input voltage		4.5/0.5	<1	5			1.5		1.5		1.5	
			9/1		10			3		3		3	
			13.5/1.5		15			4		4		4	
I _{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
			4.6			-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36		
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I _I	Input leakage current	0/18	Any input		18		±10 ⁻⁵	±0.1		±1		±1	μA
I _{OH} , I _{OL}	3-state output leakage current	0/18			18		±10 ⁻⁴	±0.4		±12		±12	
C _I	Input capacitance		Any input				5	7.5					pF

1. The noise margin for both level "1" and "0" is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, and 2.5 V min. with V_{DD} = 15 V.

Table 7. Dynamic electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test condition	Value ⁽¹⁾			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH} , t_{PHL}	Propagation delay time (clock to serial output Q_S)	5		300	600	ns
		10		125	250	
		15		95	190	
	Propagation delay time (clock to serial output Q'_S)	5		230	460	
		10		110	220	
		15		75	150	
	Propagation delay time (clock to parallel output)	5		420	840	
		10		195	390	
		15		135	270	
	Propagation delay time (strobe to parallel output)	5		290	580	
		10		145	290	
		15		100	200	
t_{PZL} , t_{PZH}	Propagation delay time (output enable to parallel out: output high to high impedance)	5		140	280	ns
		10		75	150	
		15		55	110	
	Propagation delay time (output enable to parallel out: output low to high impedance)	5		225	450	
		10		95	190	
		15		70	140	
t_w	Strobe pulse width	5	200	100		
		10	80	40		
		15	70	35		
	Clock pulse width	5	200	100		
		10	100	50		
		15	83	40		
t_s	Data setup time	5	125	60		
		10	55	30		
		15	35	20		
t_h	Minimum hold time	5	0	0	0	
		10				
		15				
t_{TLH} , t_{THL}	Transition time	5		100	200	
		10		50	100	
		15		45	80	

Table 7. Dynamic electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, $t_r = t_f = 20\text{ ns}$) (continued)

Symbol	Parameter	Test condition	Value ⁽¹⁾			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_r, t_f	Clock input rise or fall time	5	15			μs
		10	5			
		15	5			
f_{max}	Maximum clock input frequency	5	1.25	2.5		MHz
		10	2.5	5		
		15	3	6		

1. The typical temperature coefficient for all V_{DD} values is 0.3 %/ $^{\circ}\text{C}$.

Figure 6. Typical application (remote control holding register)

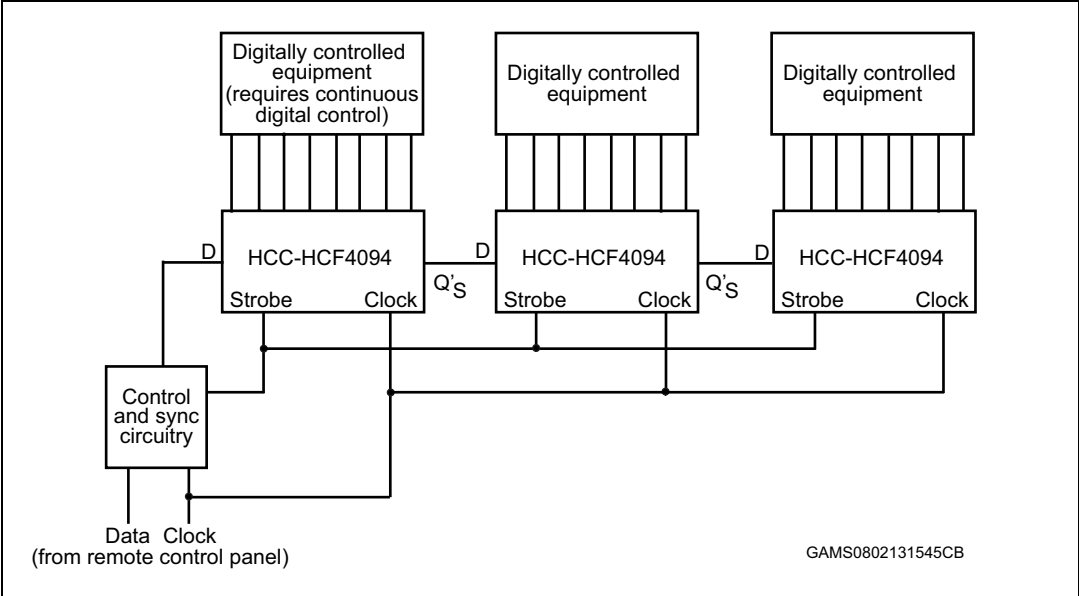
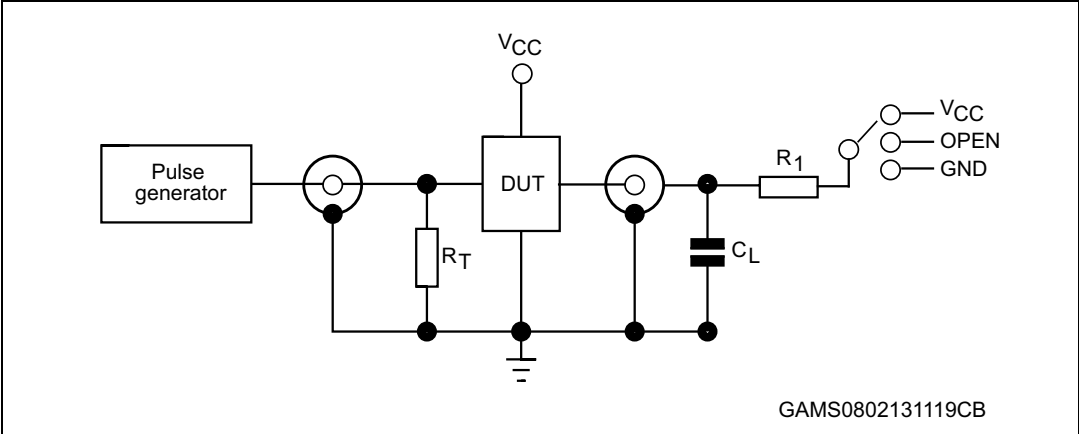


Figure 7. Test circuit



1. Legend: C_L = 50 pF or equivalent (includes jig and probe capacitance), R_L = 200 K Ω , R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Table 8. Propagation delay time configuration

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PZH}	V_{CC}
t_{PZH} , t_{PHZ}	GND

Figure 8. Waveform 1: Data in to Q_n timings (50 % clock duty cycle)

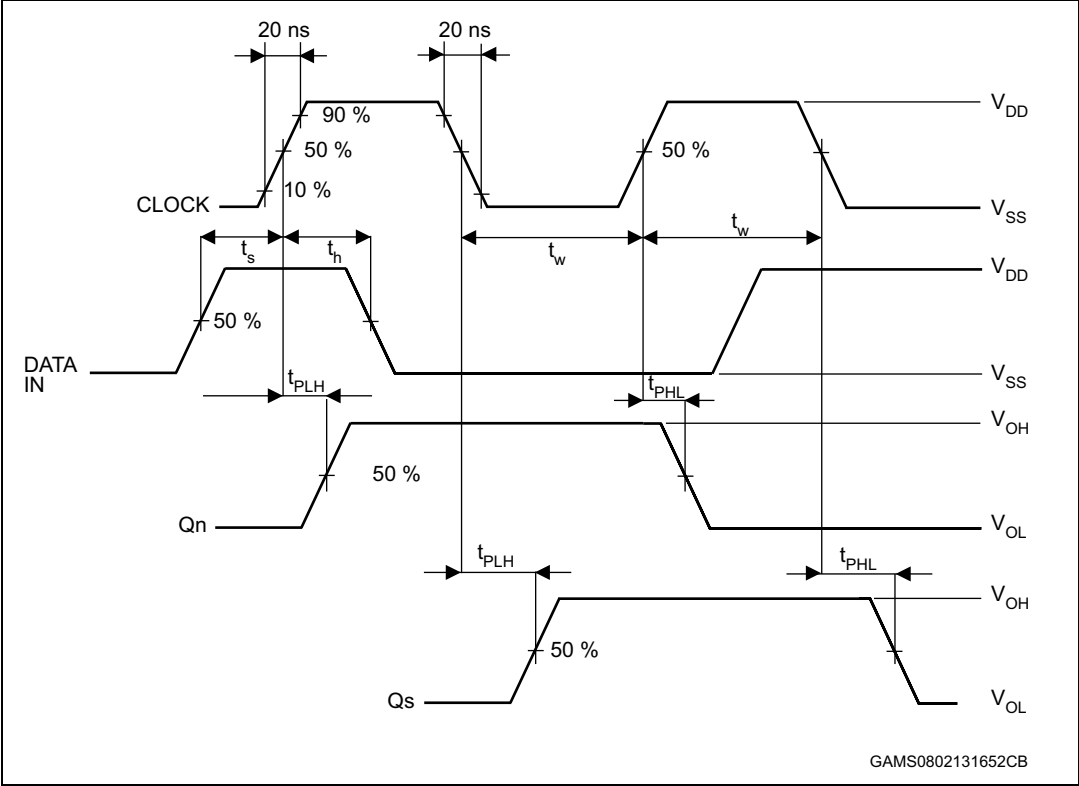


Figure 9. Waveform 2: Setup and hold times (SI to CLOCK)
(f = 1 MHz; 50 % duty cycle)

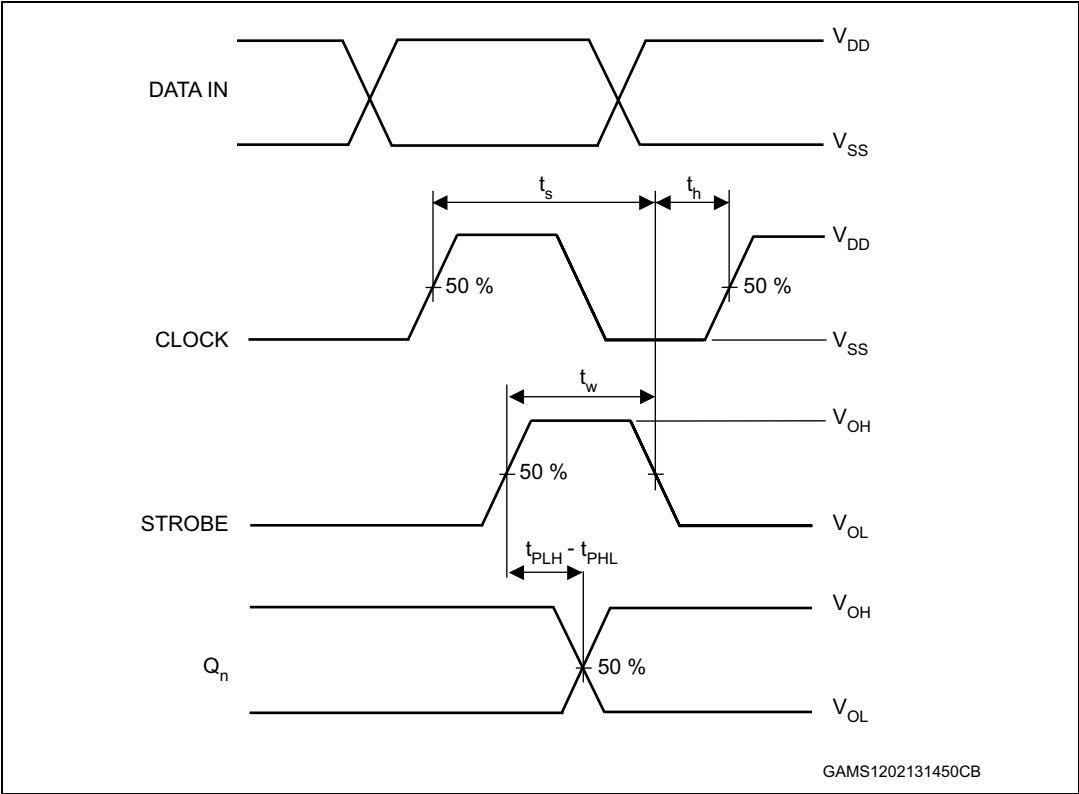
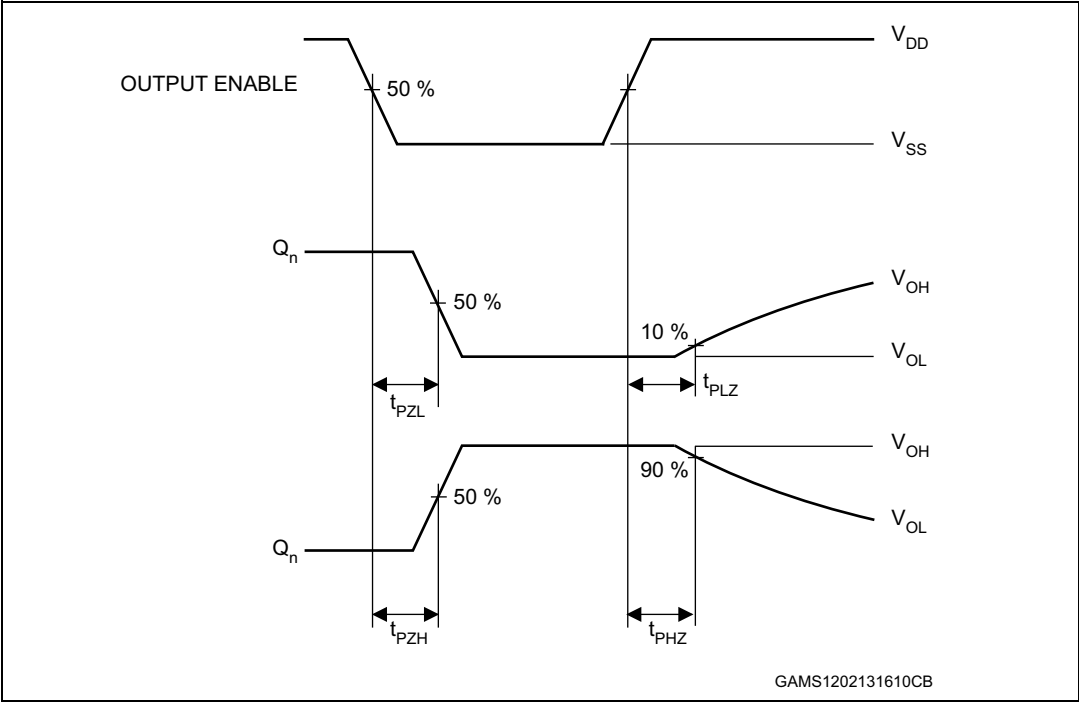


Figure 10. Waveform 3: Setup and hold time (PI to P/S)
(f = 1 MHz; 50 % duty cycle)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PDIP-16 package information

Figure 11. PDIP-16 package mechanical drawing

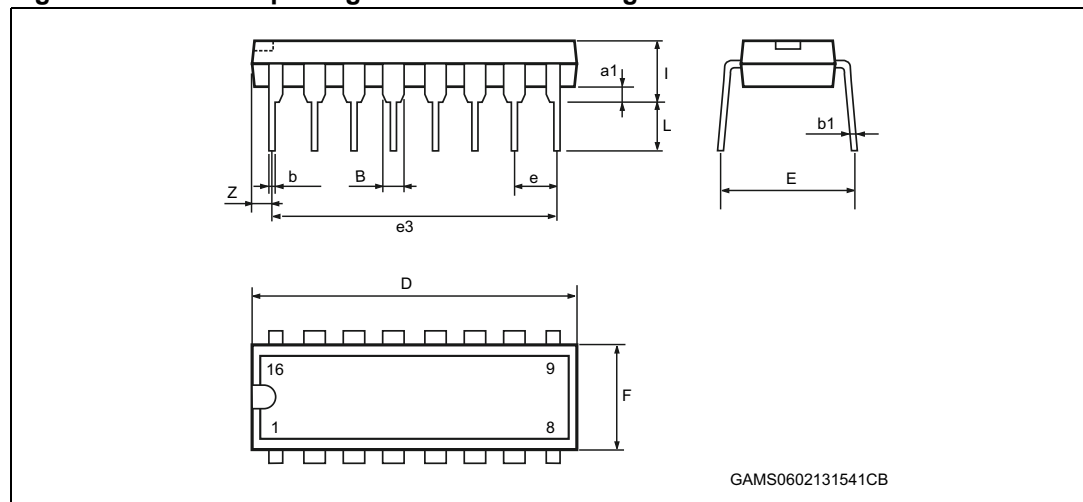


Table 9. PDIP-16 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		1.27	0.050		0.050

4.2 SO-16 package information

Figure 12. SO-16 package mechanical drawing

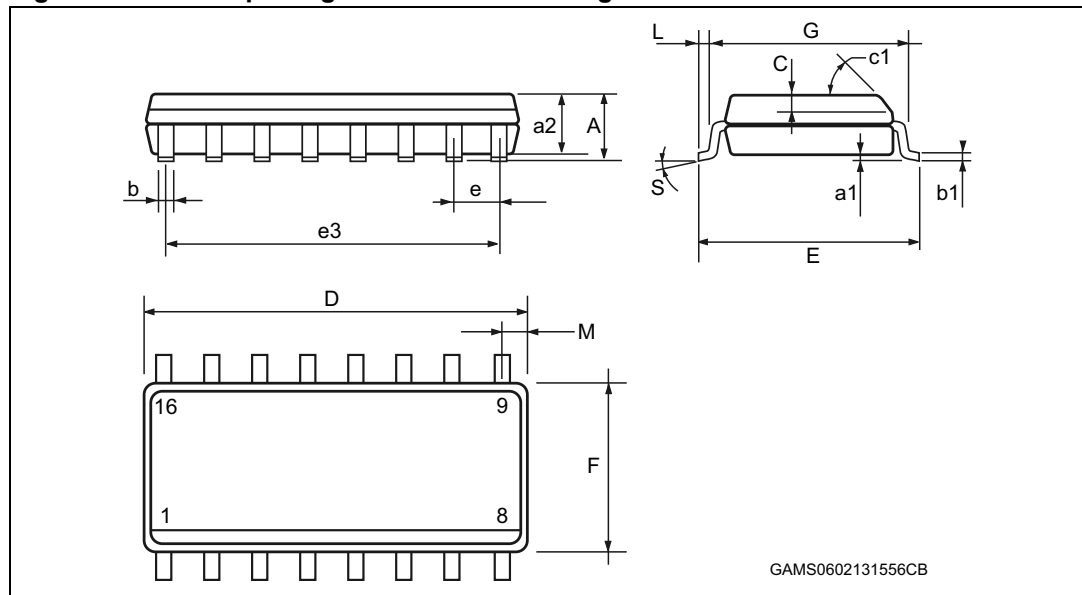
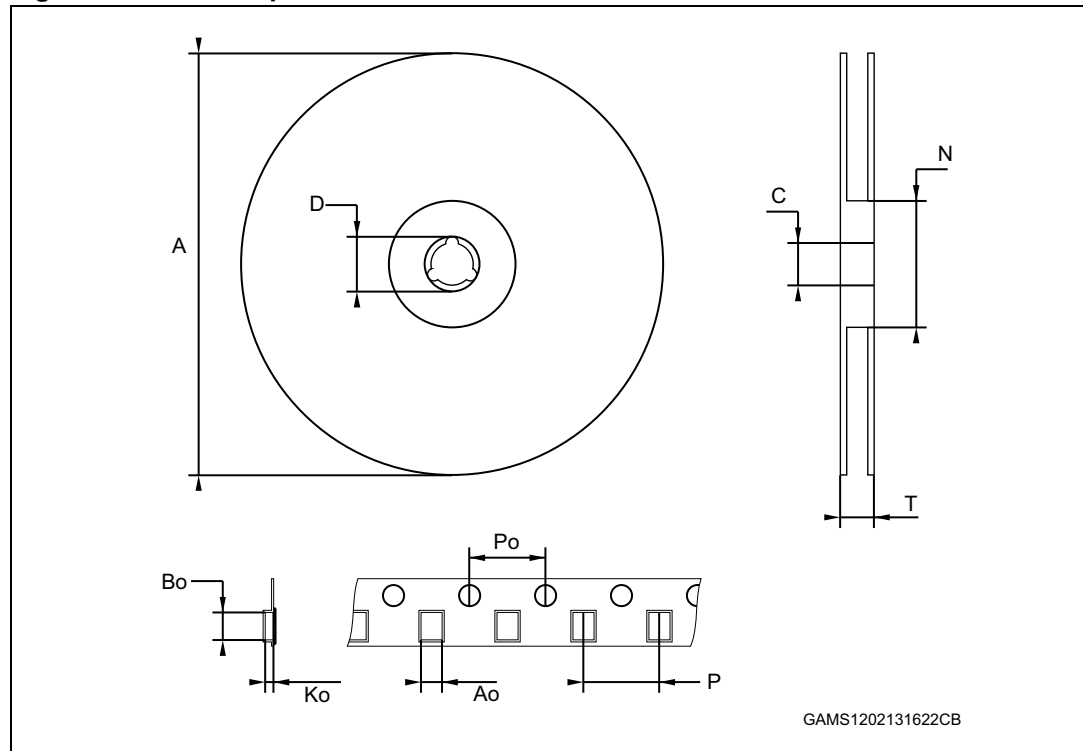


Table 10. SO-16 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S			8 °			8 °

Figure 13. SO-16 tape and reel information



1. Drawing is not to scale.

Table 11. SO-16 tape and reel information

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

5 Ordering information

Table 12. Order codes

Order code	Temperature range	Package	Packing	Marking
HCF4094M013TR	-55 ° C to +125 ° C	SO-16	Tape & reel	HCF4094
HCF4094YM013TR (1)	-40 ° C to +125 ° C	SO-16 (automotive grade) ⁽¹⁾		HCF4094Y
HCF4094BEY	-55 ° C to +125 ° C	PDIP-16	Tube	HCF4094BE

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent are ongoing.

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
19-Feb-2013	4	Document template and layout updated Removed "B" from part number Updated package names (PDIP-16 and SO-16 instead of DIP-16 and SOP-16). Added Applications Added Device summary table Updated symbol names in Table 7 Added Section 5: Ordering information

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