# 1 Characteristics

**Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ | ESD IEC 61000-4-2, air discharge<br>ESD IEC 61000-4-2, contact discharge | | 15<br>8 | kV |
| $P_{PP}$ | Peak pulse power dissipation (8/20 µs)(1) | $T_j$ initial = $T_{amb}$ | 25 | W |
| $I_{pp}$ | Repetitive peak pulse current typical value (8/20 µs) | | 2 | A |
| $T_j$ | Junction temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature range | | -55 + 150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10 s | | 260 | °C |

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

**Figure 2. Electrical characteristics (definitions)**

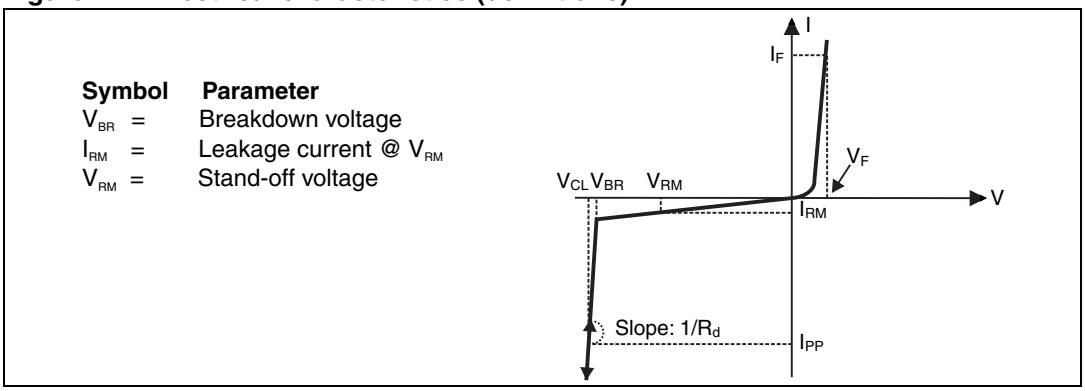



**Table 2. Electrical characteristics (values, $T_{amb}$ = 25 °C)**

| Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BR}$ | $I_R$ = 1 mA | 6.1 | | 7.2 | V |
| $I_{RM}$ | $V_{RM}$ = 3 V | | | 100 | nA |
| C | $V_R$ = 3 V DC, $F_{osc}$ = 1 MHz, $V_{osc}$ = 30 mV rms | | 7 | 9 | pF |

**Figure 3. Relative variation of peak pulse power versus initial junction temperature**

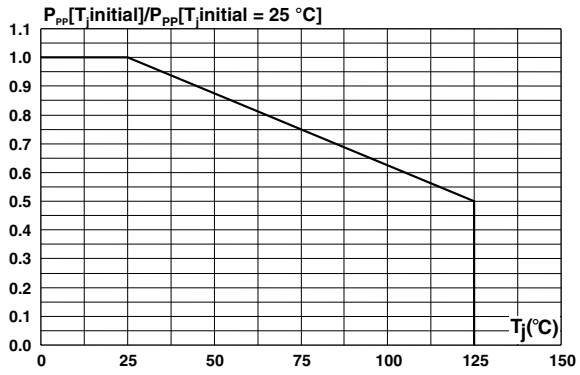



**Figure 4. Peak pulse power versus exponential pulse duration**

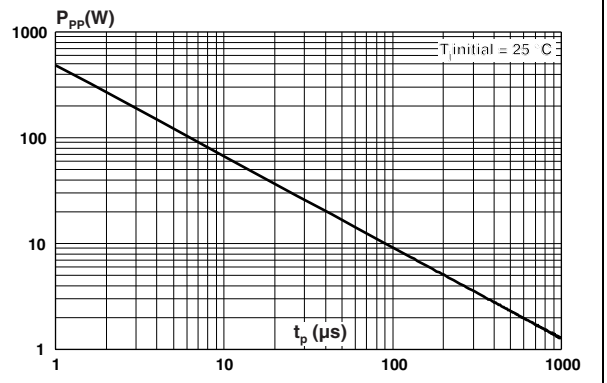



**Figure 5. Clamping voltage versus peak pulse current (typical values, exponential waveform)**

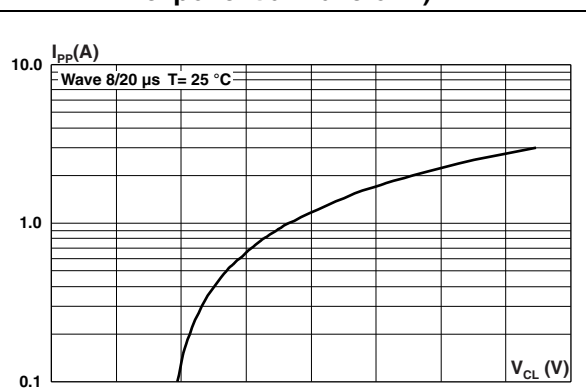



**Figure 6. Forward voltage drop versus peak forward current (typical values)**

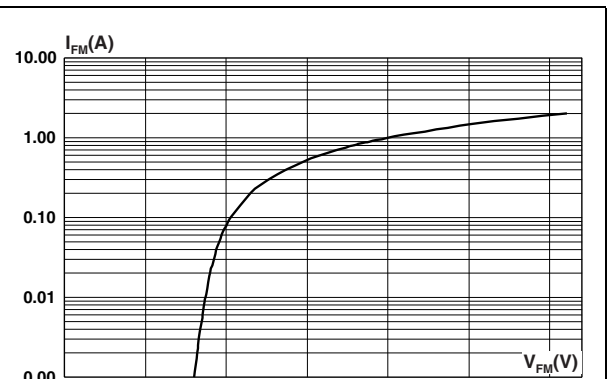



**Figure 7. Junction capacitance versus reverse voltage applied (typical values)**

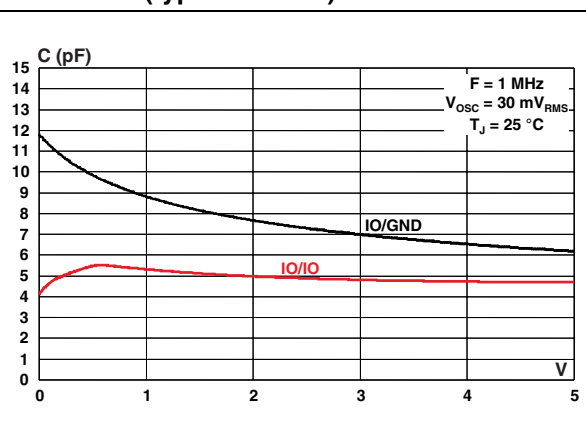



**Figure 8. Relative variation of leakage current versus junction temperature (typical values)**

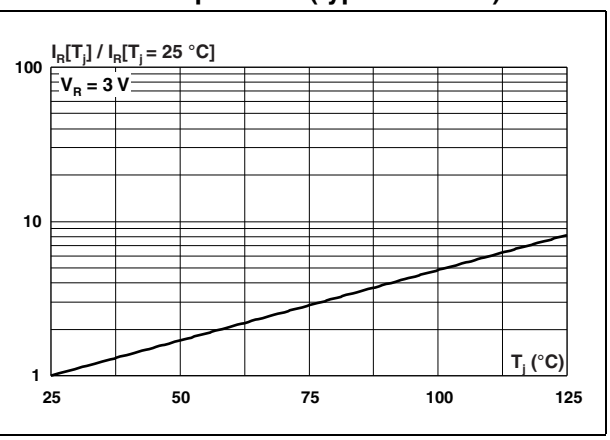


**Figure 9. S21 attenuation measurement results of each channel**

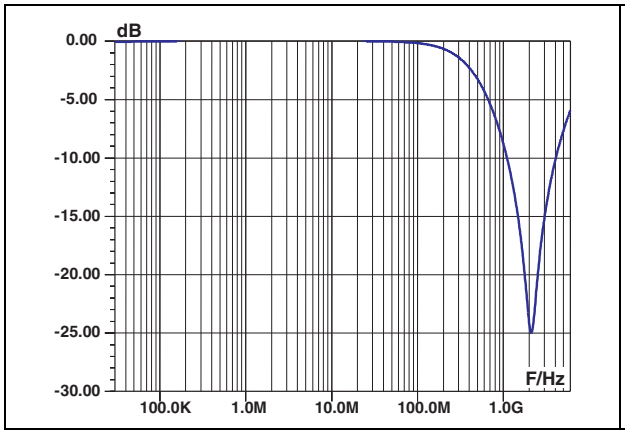



**Figure 10. Analog crosstalk measurements between channels**

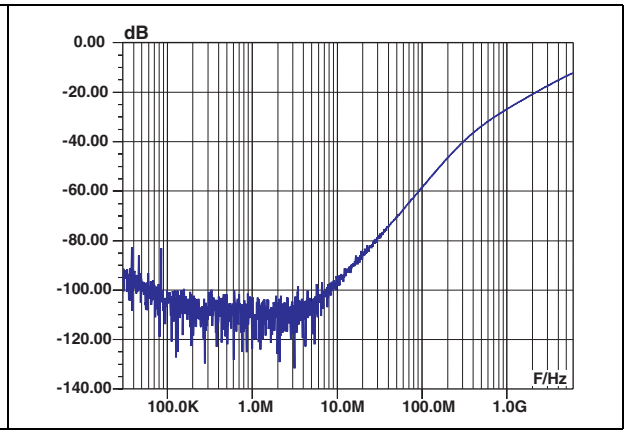



**Figure 11. ESD response to IEC 61000-4-2 (+15 kV air discharge) on each channel**

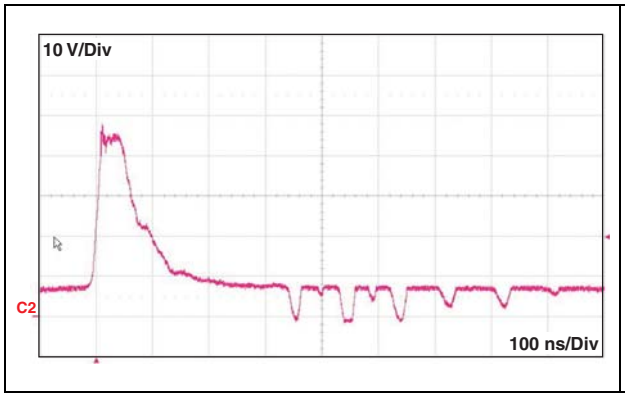
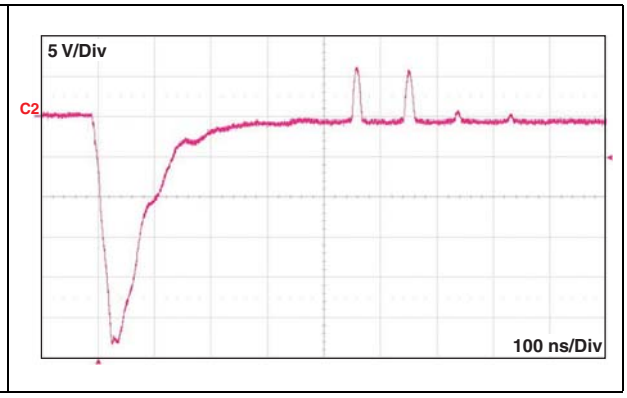
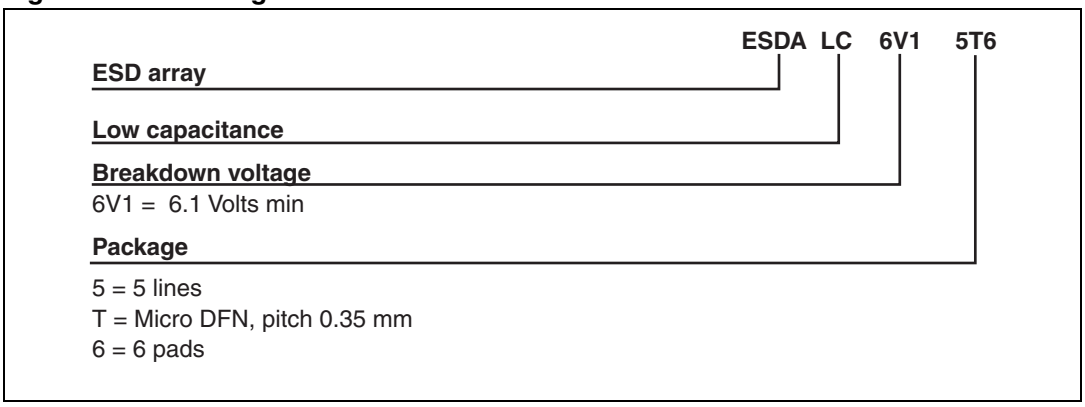



**Figure 12. ESD response to IEC 61000-4-2 (-15 kV air discharge) on each channel**




# 2 Ordering information scheme

**Figure 13. Ordering information scheme**

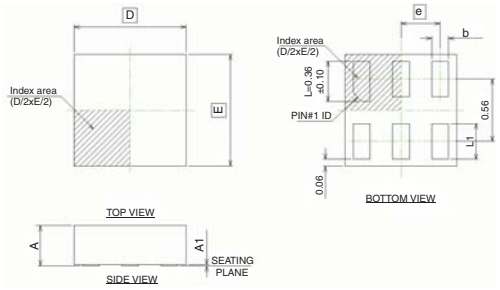


# 3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Table 3. Micro DFN 1.0 x 1.0-6L dimensions**




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.31 | - | 0.40 | 0.012 | - | 0.016 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.0008 | 0.002 |
| b | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| E | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| L1 | 0.22 | 0.32 | 0.42 | 0.009 | 0.012 | 0.016 |
| e | - | 0.35 | - | - | 0.014 | - |

**Figure 14. Footprint dimensions (in mm)**

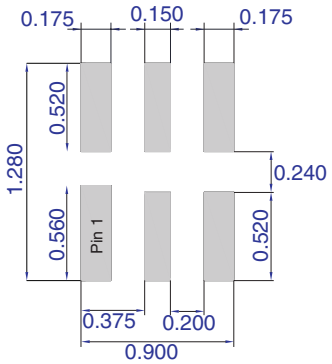
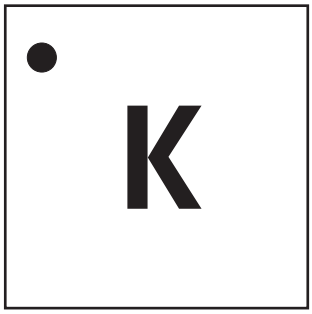
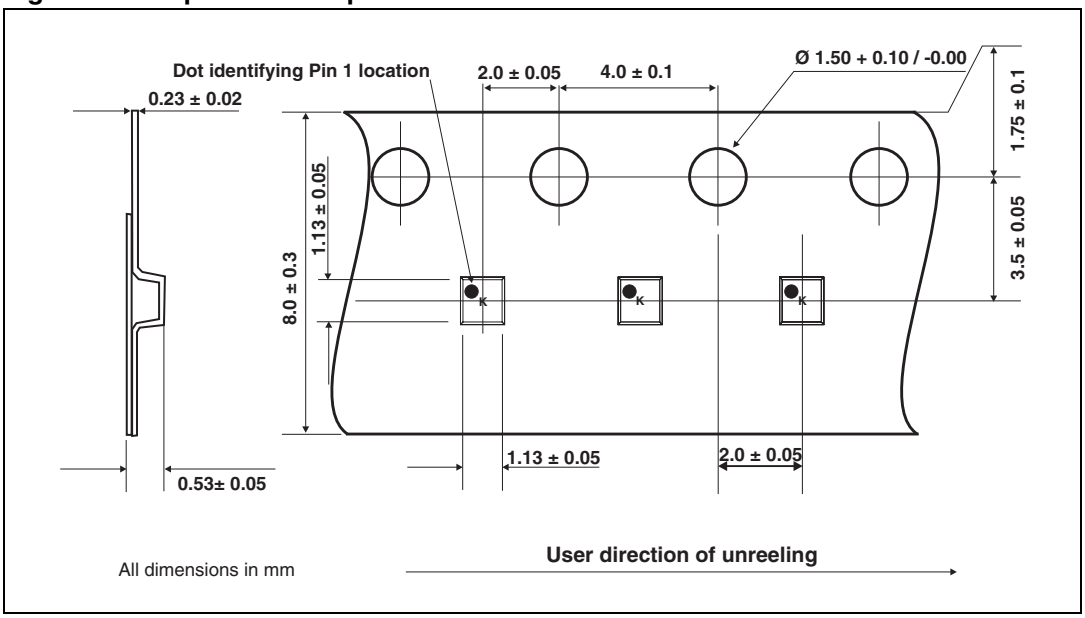



**Figure 15. Marking**




*Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*

**Figure 16. Tape and reel specifications**

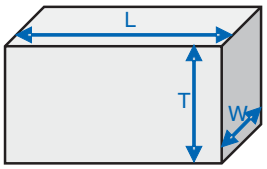


# 4 Recommendation on PCB assembly

## 4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

**Figure 17. Stencil opening dimensions**




   b) General design rule

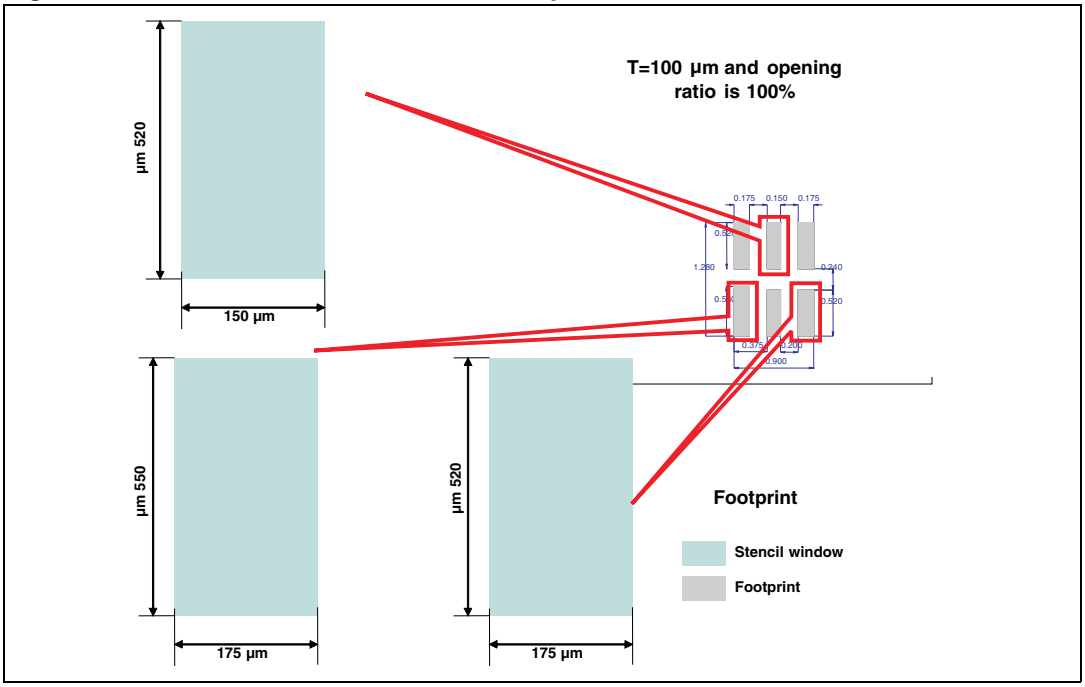
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 100%.

**Figure 18. Recommended stencil window position**



## 4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

## 4.3 Placement

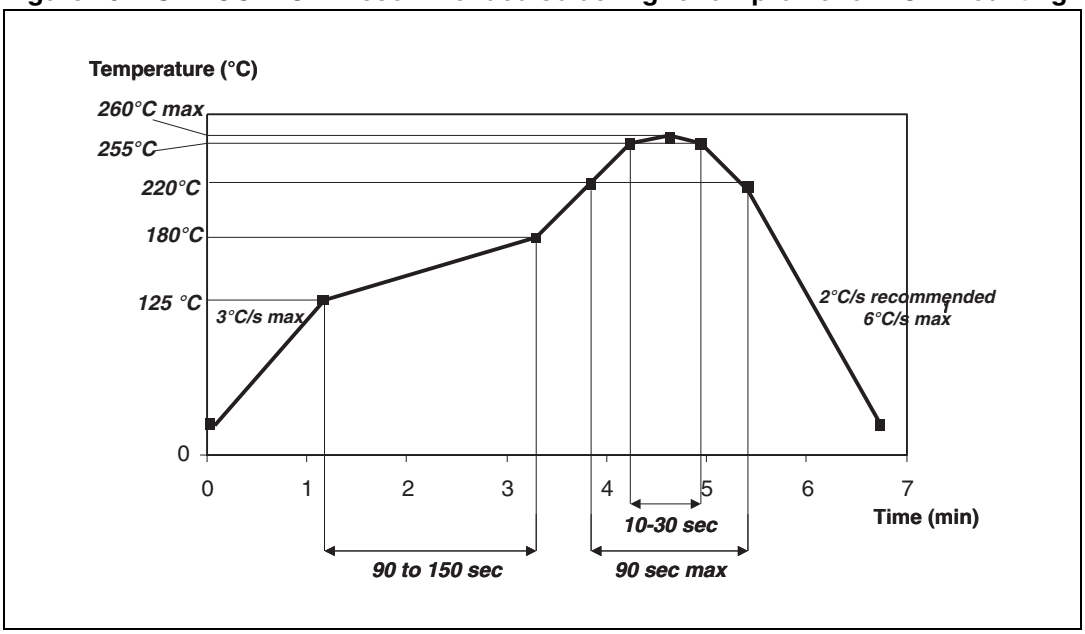
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 4.5 Reflow profile

**Figure 19. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*

# 5 Ordering information

**Table 4. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| ESDALC6V1-5T6 | K(1) | DFN1.0 x1.0-6L | 1.78 mg | 3000 | Tape and reel |

1. The marking can be rotated by multiples of 90° to differentiate assembly location

# 6 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Nov-2009 | 1 | Initial release. |
| 03-Mar-2011 | 2 | Added *Figure 15* and following note. Added footnote to *Table 4.* |

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