ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN5312QI	N5312	-40°C to +125°C	20-pin (5mm x 4mm x 1.1mm) QFN
EVB-EN5312QI	EVB-EN5312QI	QFN Evaluation Board	

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

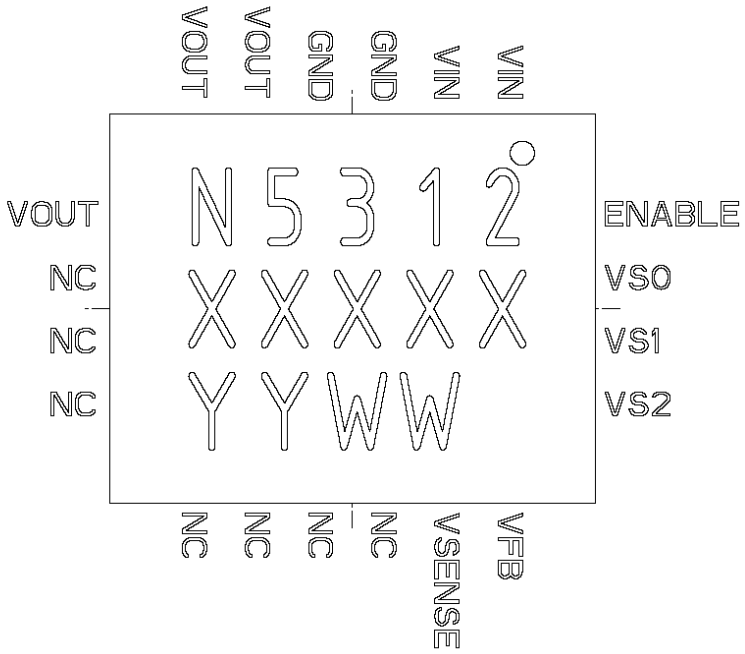


Figure 3. Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 2	VIN	Power	Input voltage pin. Supplies power to the IC.
3	Input Ground	Power	Input power ground. Connect this pin to the ground terminal of the input capacitor. Refer to Layout Recommendations for further details.
4	Ground	Power	Power ground. The output filter capacitor should be connected between this pin and V_{OUT}. Refer to Layout recommendations for further detail.
5- 7	VOUT	Power	Regulated converter output.
8- 14	NC	-	These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
15	VSENSE	Analog	Sense pin for output voltage regulation. Connect V_{SENSE} to the output voltage rail as close to the terminal of the output filter capacitor as possible.
16	VFB	Analog	Feedback pin for external divider option. When using the external divider option (VS0=VS1=VS2= high) connect this pin to the center of the external divider. Set the divider such that VFB = 0.603V.
17-19	VS0, VS1, VS2	Analog	Output voltage select. VS0=pin19, VS1=pin18, VS2=pin17. Selects one of seven preset output voltages or choose external divider by connecting pins to logic high or low. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.
20	ENABLE	Analog	Output enable. Enable = logic high, disable = logic low. Logic low is defined as $V_{LOW} \leq 0.2V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.
	Bottom Thermal Pad	Power	Device thermal pad to remove heat from package. Connect to PCB surface ground pad and PCB internal ground plane (see layout recommendations).

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	7.0	V
ENABLE, V_{SENSE}, V_{S0}- V_{S2}		-0.3	V_{IN}+0.3	V
V_{FB}		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Input Voltage Range (External Divider (VFB)) (1)	V_{IN}	2.4	6.6	V
Output Voltage Range	V_{OUT}	0.6	V_{IN} – 0.6	V
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	15	°C
Thermal Resistance: Junction to Ambient (0 LFM) (2)	θ_{JA}	65	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	15	°C/W

ELECTRICAL CHARACTERISTICS

NOTE: T_A = 25°C unless otherwise noted. Typical values are at V_{IN} = 3.6V, C_{IN} = 4.7µF, C_{OUT}=10µF.

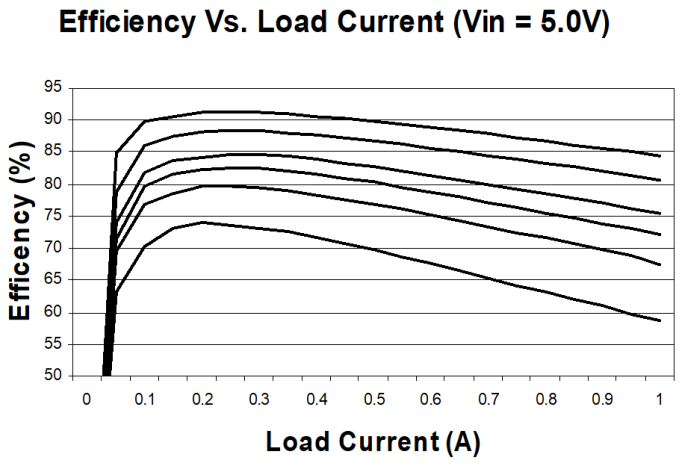
NOTE: V_{IN} must be greater than V_{OUT} + 0.6V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	Using VID	2.4		5.5	V
		Using External Divider (VFB) (1)	2.4		6.6	V
Under Voltage Lock-out	V_{UVLO}	VIN going low to high		2.2	2.3	V
UVLO Hysteresis				0.145		V
V_{OUT} Initial Accuracy (VID)	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 1A; T_A = 25C	-2.0		+2.0	%
V_{OUT} Variation for all Causes (VID)	V_{OUT}	2.4V ≤ V_{IN} ≤ 5.5V, I_{LOAD} = 0- 1A, T_A = -40°C to +85°C	-3.0		+3.0	%
Feedback Pin Voltage	V_{FB}	2.4V ≤ V_{IN} ≤ 6.6V, I_{LOAD} = 100mA, *T_A = 25°C, V_{SO}=V_{S1}=V_{S2}=1*	0.591	0.603	0.615	V
Feedback Pin Voltage	V_{FB}	2.4V ≤ V_{IN} ≤ 6.6V, I_{LOAD} = 0 -1A, T_A = -40°C to +85°C, V_{SO}=V_{S1}=V_{S2}=1	0.585	0.603	0.621	V
Feedback Pin Input Current	I_{FB}			1		nA
Dynamic Voltage Slew Rate (3)	V_{slew}		1.24	1.65	2.1	V/ms
Output Current	I_{OUT}		1000			mA
Shut-Down Current	I_{SD}	Enable = Low		0.75		µA
Quiescent Current		No switching		800		µA
PFET OCP Threshold	I_{LIM}	2.4V ≤ V_{IN} ≤ 6.6V, 0.6V ≤ V_{OUT} ≤ V_{IN} – 0.6V	1.4	2		A
VS0-VS1 Thresholds	V_{TH}	Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	
VS0-VS2 Pin Input Current	I_{VSX}			1		nA

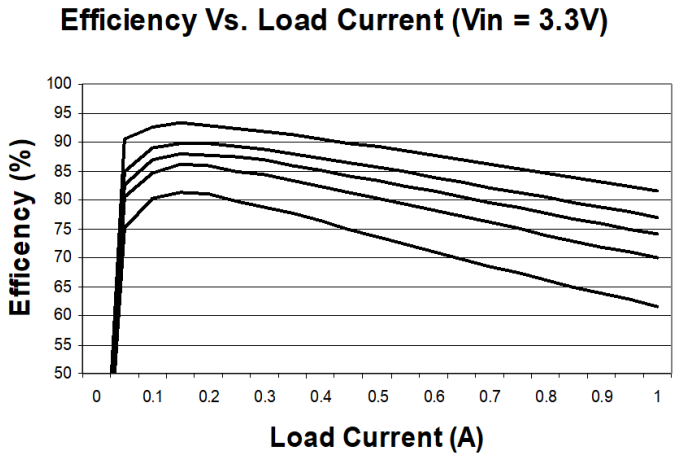
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Voltage Threshold		Logic Low Logic High	0.0 1.4		0.2 V_{IN}	
Enable Pin Input Current	I_{EN}	V_{IN} = 3.6V		2		µA
Operating Frequency	F_{OSC}			4		MHz
PFET On Resistance	$R_{DS(ON)}$			340		mΩ
NFET On Resistance	$R_{DS(ON)}$			270		mΩ
Typical inductor DCR				0.110		Ω
V_{OUT} Soft Start Slew Rate(3)	ΔV_{SS}	VID Mode (4)	1.24	1.65	2.1	V/ms
Soft Start Rise Time	ΔT_{SS}	VFB mode (4)	0.80	1.10	1.40	ms

(1) See Section “Application Information” for specific circuit requirements.
(2) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.
(3) Parameter not production tested but is guaranteed by design.
(4) Measured from when VIN ≥ VUVLO & ENABLE pin crosses its logic High threshold.

TYPICAL PERFORMANCE CURVES

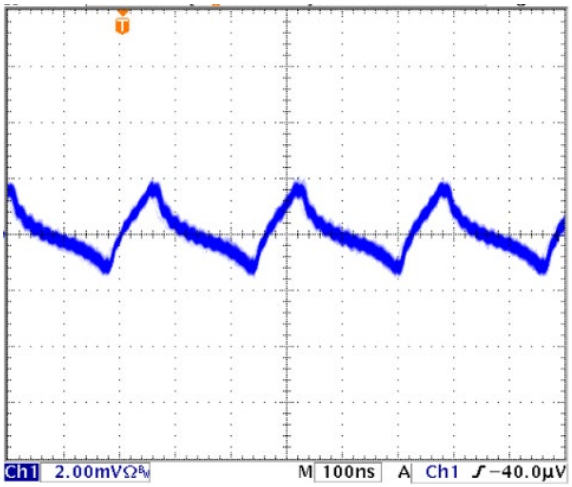


Top to Bottom: V_{OUT} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 0.8V

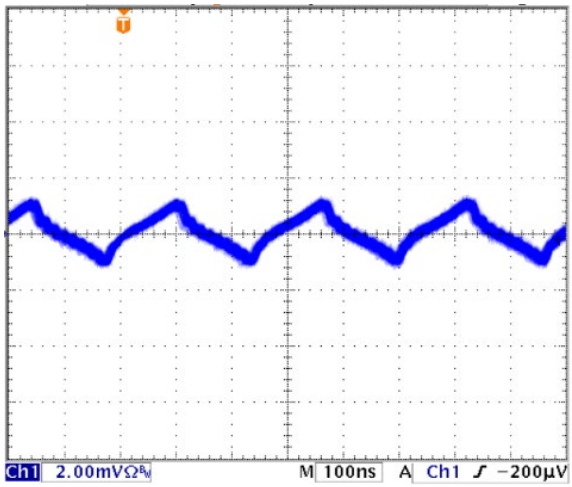


Top to Bottom: V_{OUT} = 2.5V, 1.8V, 1.5V, 1.2V, 0.8V

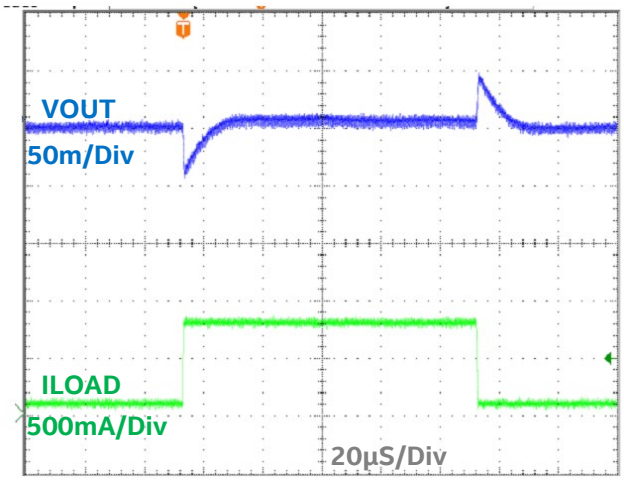
TYPICAL PERFORMANCE CHARACTERISTICS



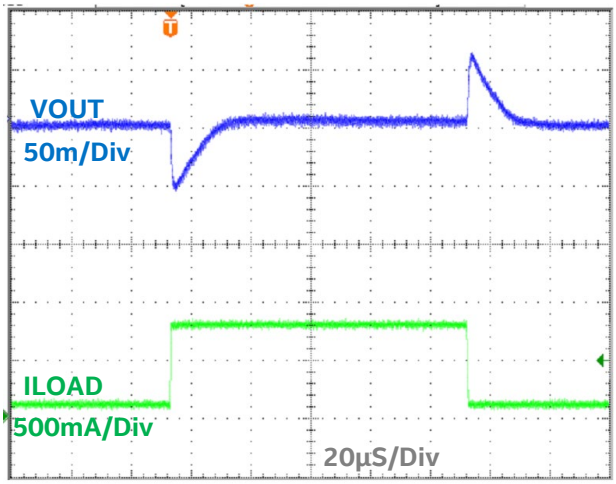
Output Ripple: V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{LOAD} = 1A, C_{OUT} = 1 x 10µF 0805



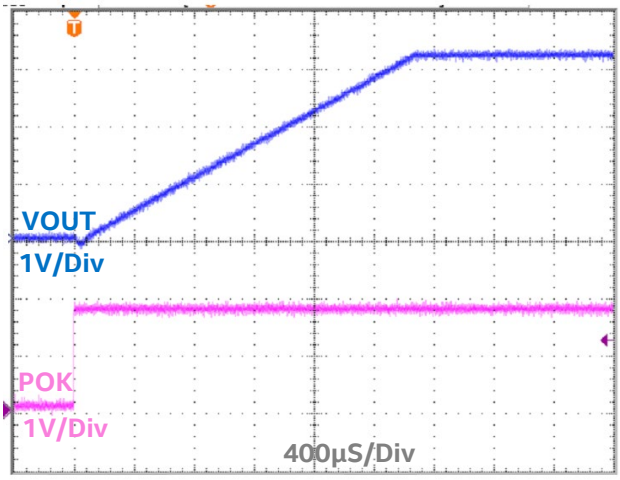
Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, I_{LOAD} = 1A, C_{OUT} = 1 x 10µF 0805



Load Transient: V_{IN} = 5.0V, V_{OUT} = 3.3V, I_{LOAD} = 100mA to 800mA



Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{LOAD} = 100mA to 800mA



Start-up: VIN = 5.0V, V_{OUT} = 3.3V

FUNCTIONAL BLOCK DIAGRAM

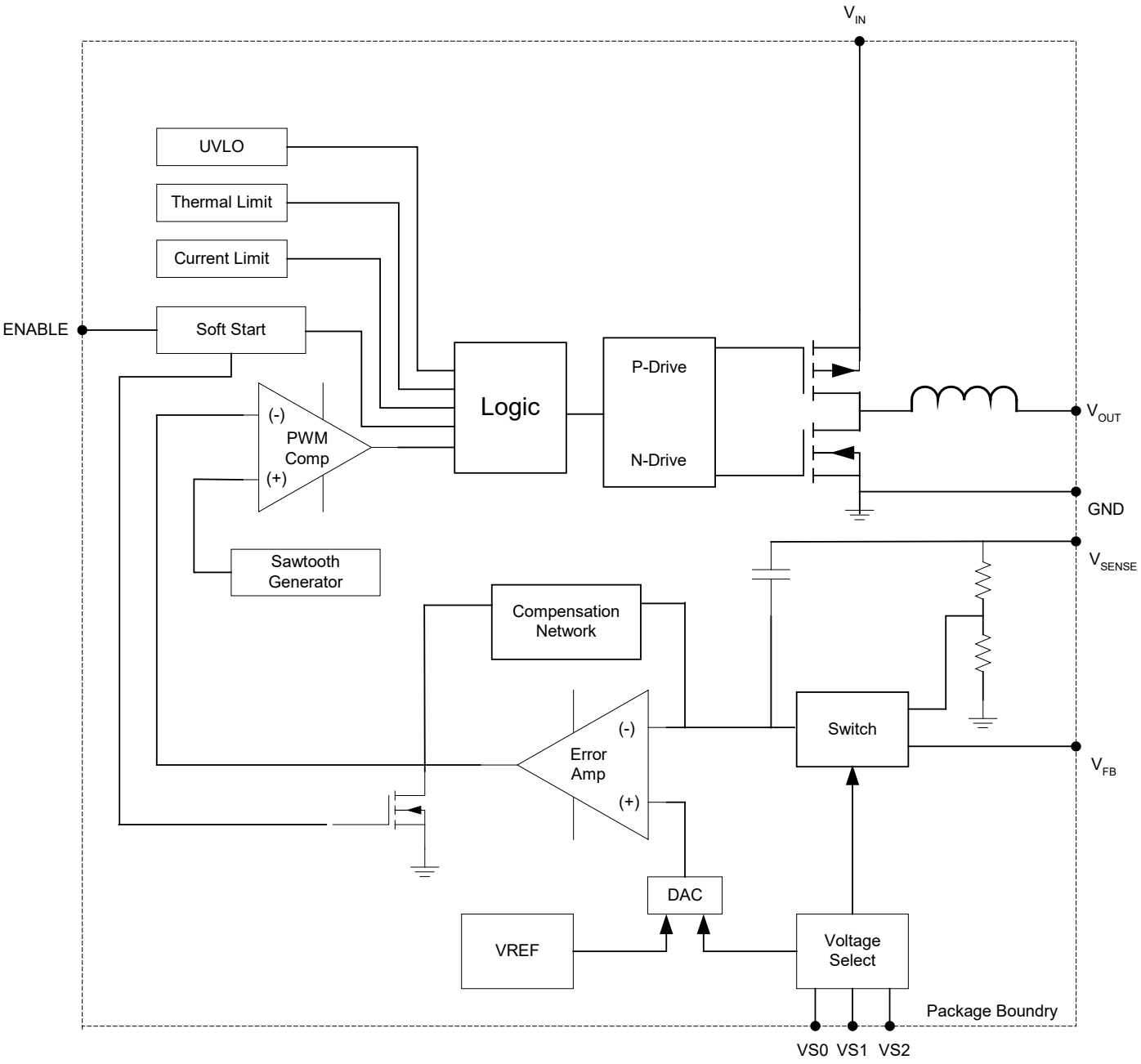


Figure 4. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN5312QI is a complete DC-DC converter solution requiring only two low cost MLCC capacitors. MOSFET switches, PWM controller, Gate-drive, compensation, and inductor are integrated into the tiny 5mm x 4mm x 1.1mm package to provide the smallest footprint possible while maintaining high efficiency, low ripple, and high performance. The converter uses voltage mode control to provide the simplest implementation and high noise immunity. The device operates at a high switching frequency. The high switching frequency allows for a wide control loop bandwidth providing excellent transient performance. The high switching frequency enables the use of very small components making possible this unprecedented level of integration.

Intel Enpirion's proprietary power MOSFET technology provides very low switching loss at frequencies of 4 MHz and higher, allowing for the use of very small internal components, and very wide control loop bandwidth. Unique magnetic design allows for integration of the inductor into the very low profile 1.1mm package. Integration of the inductor virtually eliminates the design/layout issues normally associated with switch-mode DC-DC converters. All of this enables much easier and faster integration into various applications to meet demanding EMI requirements.

Output voltage is chosen from seven preset values via a three pin VID voltage select scheme. An external divider option enables the selection of any voltage in the 0.6V to V_{IN}-0.6V range. This reduces the number of components that must be qualified and reduces inventory burden. The VID pins can be toggled on the fly to implement glitch free dynamic voltage scaling.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor

Intel Epirion has introduced the world's first product family featuring integrated inductors. The use of an internal inductor localizes the noises associated with the output loop currents. The inherent shielding and compact construction of the integrated inductor reduces the radiated noise that couples into the traces of the circuit board. Further, the package layout is optimized to reduce the electrical path length for the AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor significantly reduces parasitic effects that can harm loop stability, and makes layout very simple.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EN5312QI operates in a constant slew rate when the output voltage is programmed with an internal VID code. The EN5312QI, when in external resistor divider mode, has a constant start up time. Please refer to the Electrical Characteristics table for soft-start slew rates and soft-start time

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Assuming no-load at startup, the maximum total capacitance on the output, including the output filter capacitor, bulk and decoupling capacitance, at the load, is given as:

In VID Mode:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 700\mu F$

In external divider mode:

$C_{OUT\_TOTAL\_MAX} = 1.22x10^{-3}/V_{OUT}$ Farads

See the applications section for more details.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for a period of 1ms and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat in a "hick-up" mode.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. In shutdown mode, the device quiescent current will be less than 1 µA.

NOTE: This pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

APPLICATION INFORMATION

Output Voltage Setting

To provide the highest degree of flexibility in choosing output voltage, the EN5312QI uses a 3 pin VID, or Voltage ID, output voltage select arrangement. This allows the designer to choose one of seven preset voltages, or to use an external voltage divider. Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.

Table 1 shows the various VS0-VS2 pin logic states and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. These pins must not be left floating.

The External Voltage Divider pin, $V_{FB,}$ may be left floating for all VID settings other than the VS0=VS1=VS2= "1".

Table 1: VID Voltage Select Settings

VS2	VS1	VS0	V_{OUT}
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	User Selectable

External Voltage Divider

As described above, the external voltage divider option is chosen by connecting the VS0, VS1, and VS2 pins to V_{IN} or logic "high". The EN5312QI uses a separate feedback pin, VFB, when using the external divider.

For applications with $V_{IN} \leq 5.5V$, VSENSE must be connected to VOUT as indicated in Figure 5.

Figure 6 indicates the required connections for $V_{IN} > 5.5V$.

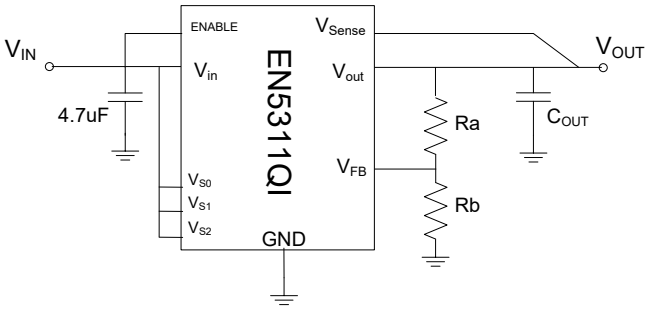


Figure 5. External Divider ($V_{IN} \leq 5.5V$)

The output voltage is selected by the following formula:

$$V_{OUT} = 0.603V\left(1 + \frac{Ra}{Rb}\right)$$

R_a must be chosen as 200KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{1.2x10^5}{V_{OUT} - 0.603}\Omega$$

V_{OUT} can be programmed over the range of 0.6V to V_{IN} – 0.6V (0.6 is the nominal full load dropout voltage including margin).

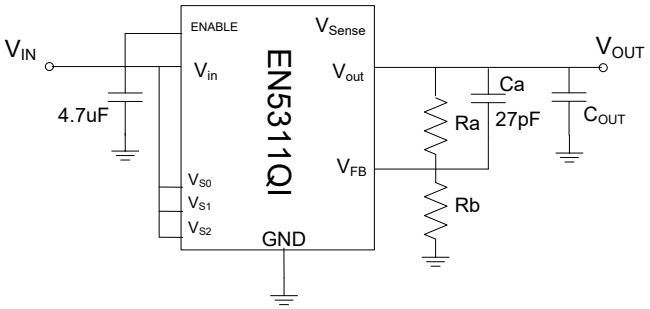


Figure 6. External Divider ($V_{IN} > 5.5V$)

For applications where $V_{IN} > 5.5V$, the V_{SENSE} connection is not necessary, but the addition of C_A = 27pF is required.

Dynamically Adjustable Output

The EN5312QI is designed to allow for dynamic switching between the predefined VID voltage levels. The inter-voltage slew rate is optimized to prevent excess undershoot or overshoot as the output voltage levels transition. The slew rate is identical to the soft-start slew rate of 1.65V/ms.

Dynamic transitioning between internal VID settings and the external divider is not allowed.

Input and Output Capacitors

The **input** capacitance requirement is 4.7µF. Intel Enpirion recommends that a low ESR MLCC capacitor be used. The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input and output filter applications.

Table 2. Input Capacitor Recommendations

Manufacturer	Part	Value	W VDC	Case Size
Murata	GRM219R61A47KE19D	4.7µF	10V	0805
	GRM319R61A475KA01D	4.7µF	10V	1206
	GRM219R60J475KE01D	4.7µF	10V	0805
	GRM31MR60J475KA01L	4.7µF	10V	1206
Panasonic	ECJ-2FB1A475K	4.7µF	10V	0805
	ECJ-3YB1A475K	4.7µF	10V	1206
	ECJ-2FB0J475K	4.7µF	6.3V	0805
	ECJ-3YB0J475K	4.7µF	6.3V	1206
Taiyo Yuden	LMK212BJ475KG-T	4.7µF	10V	0805
	LMK316BJ475KG-T	4.7µF	10V	1206
	JMK212BJ475KG-T	4.7µF	6.3V	0805

The output capacitance requirement is a minimum of 10µF. The control loop is designed to be stable with up to 60µF of total output capacitance next to the output pins of the device without requiring modification to the compensation network. V_{OUT} has to be sensed at the last output filter capacitor next to the device. Capacitance above the 10uF minimum should be added if the transient performance is not sufficient using the 10µF. Intel Enpirion recommends a low ESR MLCC type capacitor be used.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance. The separation provides an inductance that isolates the control loop from the bulk capacitance.

Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter input and output filter applications.

Table 3. Output Capacitor Recommendations

Manufacturer	Part	Value	W VDC	Case Size
Murata	GRM219R60J106KE19D	10µF	6.3V	0805
	GRM319R60J106KE01D	10µF	6.3V	1206
Panasonic	ECJ-2FB0J106K	10µF	6.3V	0805
	ECJ-3YB0J106K	10µF	6.3V	1206
Taiyo Yuden	JMK212BJ106KD-T	10µF	6.3V	0805
	JMK316BJ106KF-T	10µF	6.3V	1206

Power-Up Sequencing

During power-up, ENABLE should not be asserted before VIN. Tying these pins together meets these requirements.

Startup into Pre-Bias

The EN5312QI does not support startup into a pre-biased output. The output of the EN5312QI cannot be pre-biased with a voltage when it is first enabled.

LAYOUT RECOMMENDATIONS

*Optimized PCB Layout file downloadable from the Intel Enpirion Website to assure first pass design success.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5312QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5312QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: DO NOT connect GND pins 3 and 4 together. Pin 3 should be used for the Input capacitor local ground and pin 4 should be used for the output capacitor ground. The ground pad for the input and output filter capacitors should be isolated ground islands and should be connected to system ground as indicated in recommendation 3 and recommendation 5.

Recommendation 3: Multiple small vias (0.25mm after copper plating) should be used to connect ground terminals of the Input capacitor and the output capacitor to the system ground plane. This provides a low inductance path for the high-frequency AC currents; thereby reducing ripple and suppressing EMI (see Fig. 7, Fig. 8, and Fig. 9).

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many thermal vias as possible. The vias should use 0.33mm drill size with minimum one ounce copper plating (0.035mm plating thickness). This provides the path for heat dissipation from the converter.

Recommendation 5: The system ground plane referred to in recommendations 3 and 4 should be the first layer immediately below the surface layer (PCB layer 2). This ground plane should be continuous and un-interrupted below the converter and the input and output capacitors that carry large AC currents. If it is not possible to make PCB layer 2 a continuous ground plane, an uninterrupted ground “island” should be created on PCB layer 2 immediately underneath the EN5312QI and its input and output capacitors. The vias that connect the input and output capacitor grounds, and the thermal pad to the ground island, should continue through to the PCB GND layer as well.

Recommendation 6: As with any switch-mode DC-DC converter, do not run sensitive signal or control lines underneath the converter package.

Recommendation 7: The VOUT sense point should be just after the last output filter capacitor next to the device. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_a, C_a, and R_b close to the VFB pin (see Figures 4 and 5). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_b directly to the GND pin instead of going through the GND plane.

Figure 7 shows an example schematic for the EN5312QI using the internal voltage select. In this example, the device is set to a VOUT of 1.5V (VS2=0, VS1=1, VS0=1).

Figure 8 shows an example schematic using an external voltage divider. VS0=VS1=VS2= “1”. The resistor values are chosen to give an output voltage of 2.6V.

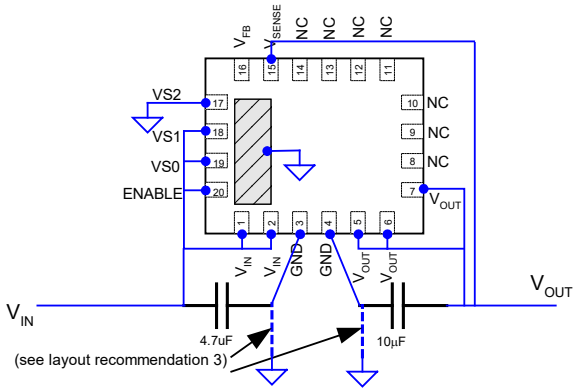


Figure 7. Example application, Vout=1.5V

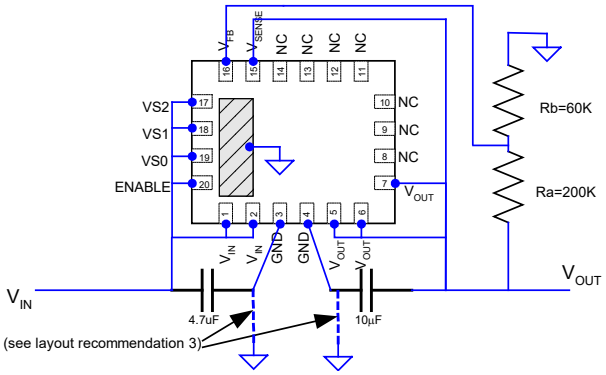


Figure 8. Example Application, external divider, Vout = 2.6V

Figure 9 shows an example board layout. The left side of the figure demonstrates construction of the PCB top layer. Note the placement of the vias from the input and output filter capacitor grounds, and the thermal pad, to the PCB ground on layer 2 (1st layer below PCB surface). The right side of the figure shows the layout with the components populated. Note the placement of the vias per recommendation 3.

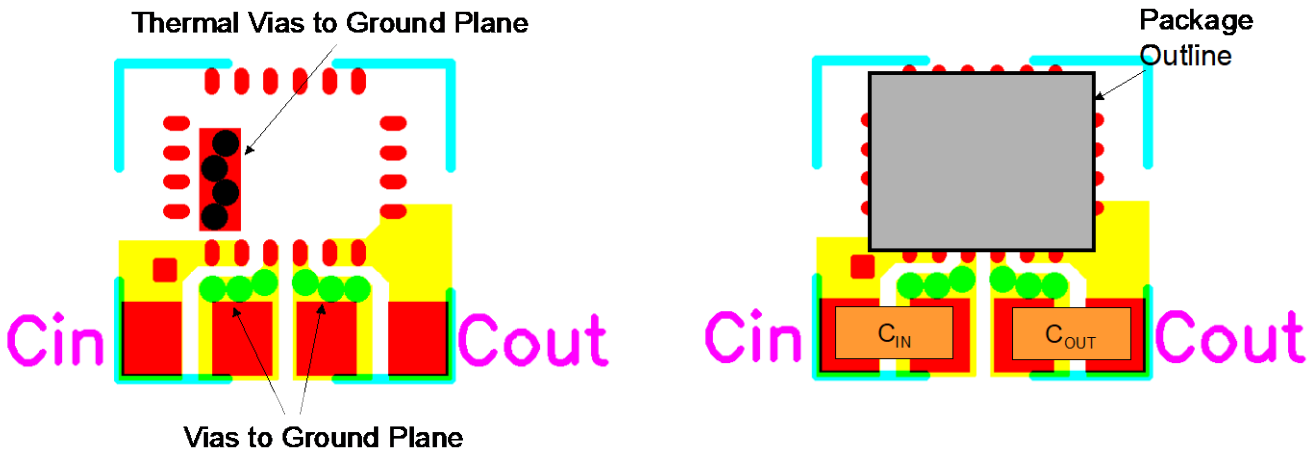


Figure 9. Example layout showing PCB top layer, as well as demonstrating use of vias from input, output filter capacitor local grounds, and thermal pad, to PCB system ground.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Intel has developed a break-through in package technology that utilizes the lead frame as part of the electrical circuit. The lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, it does require some special considerations.

As part of the package assembly process, lead frame construction requires that for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pin pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5312QI should be clear of any metal except for the large thermal pad. The "grayed-out" area in Figure 10 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

NOTE: Clearance between the various exposed metal pads, the thermal ground pad, and the perimeter pins, meets or exceeds JEDEC requirements for lead frame package construction (JEDEC MO-220, Issue J, Date May 2005). The separation between the large thermal pad and the nearest adjacent metal pad or pin is a minimum of 0.20mm, including tolerances. This is shown in Figure 11.

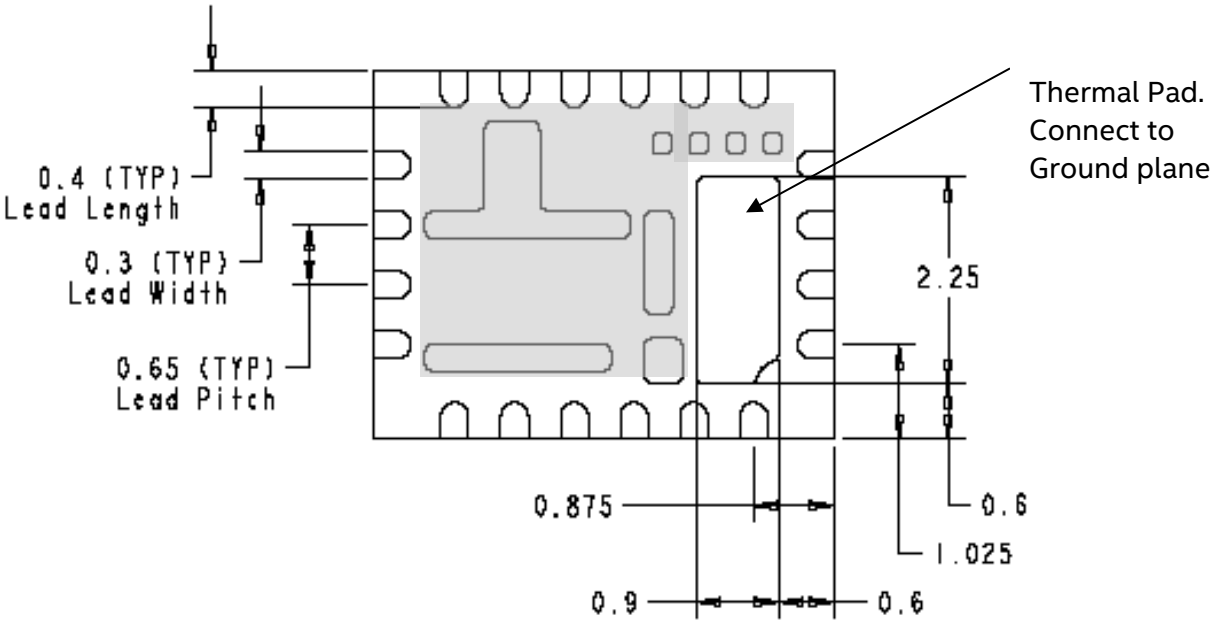


Figure 10. Exposed metal and mechanical dimensions of the package. Gray area represents bottom metal no-connect and area that should be clear of any traces, planes, or vias, on the top layer of the PCB.

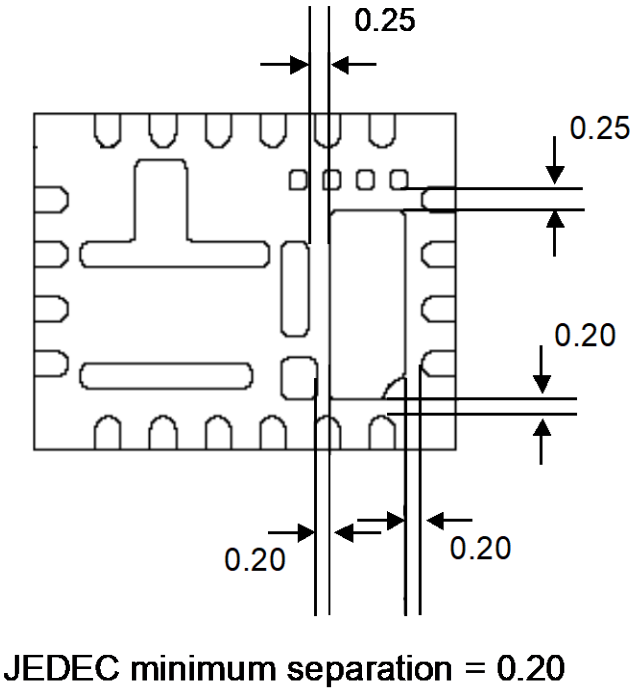


Figure 11. Exposed pad clearances; the Intel Enpirion lead frame package complies with JEDEC requirements.

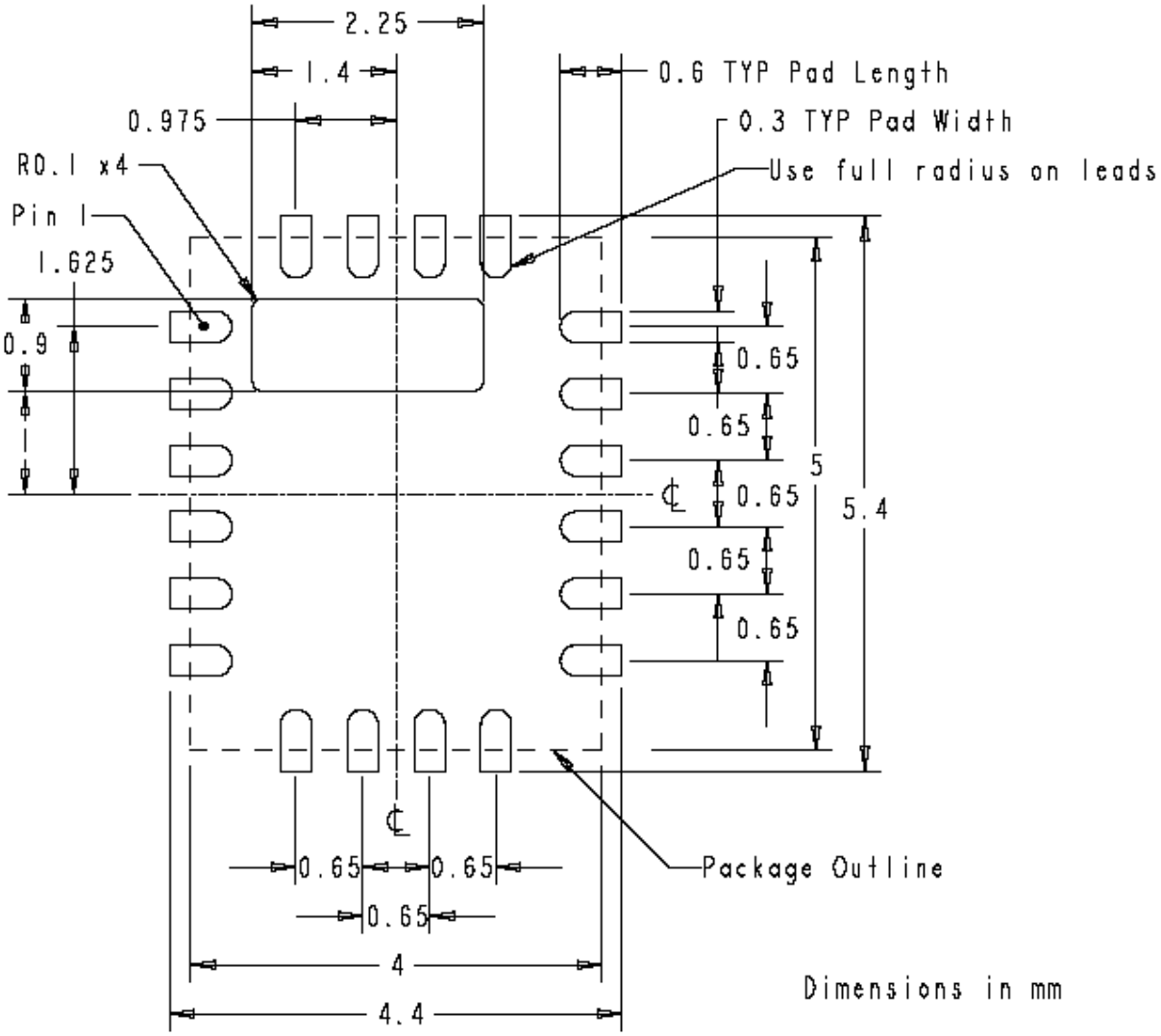


Figure 12. Recommended solder mask opening

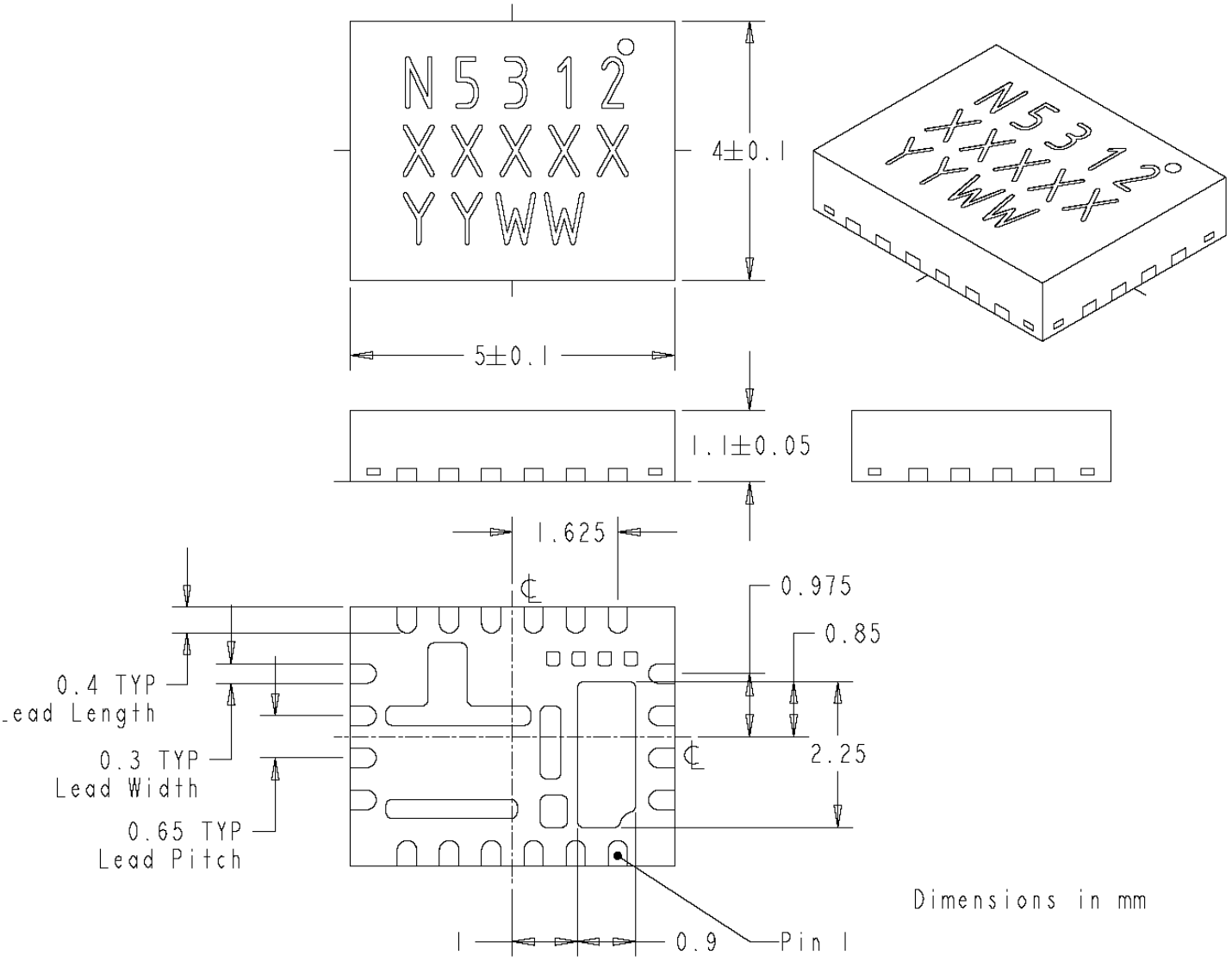


Figure 13. Package mechanical dimensions.

REVISION HISTORY

Rev	Date	Change(s)
F	March. 2019	• Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.Intel.com/enpirion