1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	25 25	kV
V_{in}	Maximum input voltage	5.5	V
T_j	Maximum junction temperature	125	° C
T_{op}	Operating temperature range	- 40 to + 85	° C
T_{stg}	Storage temperature range	125	° C

Figure 1. EMIF06-mSD01F2 configuration

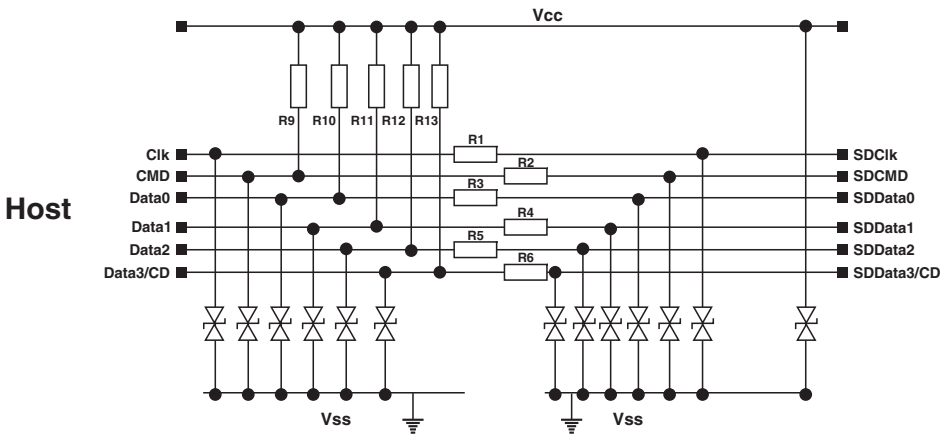


Table 2. Electrical characteristics

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	14	16		V
I_{RM}	V_{RM} = 3 V			0.1	µA
R1, R2, R3, R4, R5, R6	Tolerance ±20%		40		Ω
R9, R10, R11, R12, R13	Tolerance ±30%		25		kΩ
C_{line}	V = 0 V, F = 1 MHz V_{osc} = 30 mV		17	20	pF

Figure 2. Frequency response for line D3/D2 - V_{CC} not connected

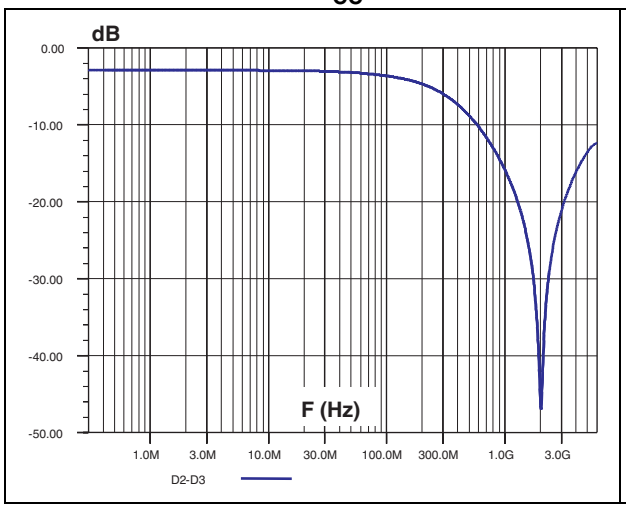


Figure 3. Frequency response for line C1/B4 - V_{CC} not connected

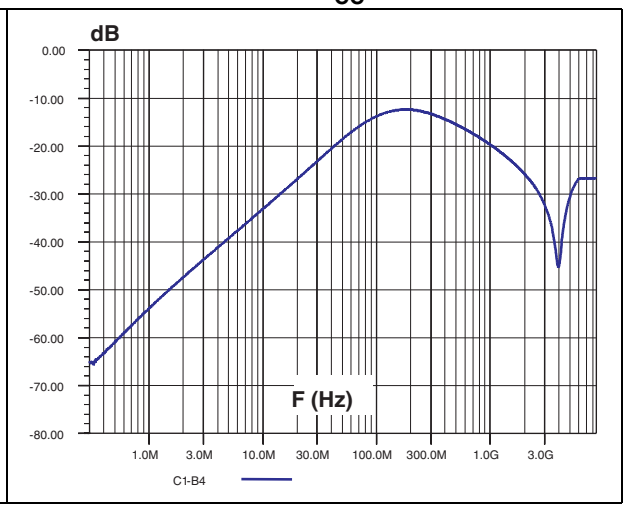


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one imput (V_{in}) and one output (V_{out})

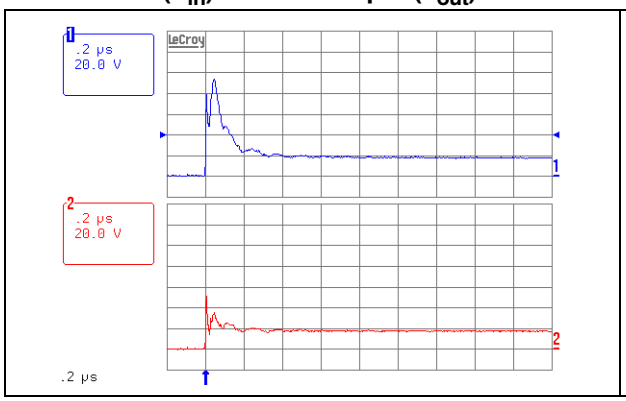


Figure 5. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one imput (V_{in}) and one output (V_{out})

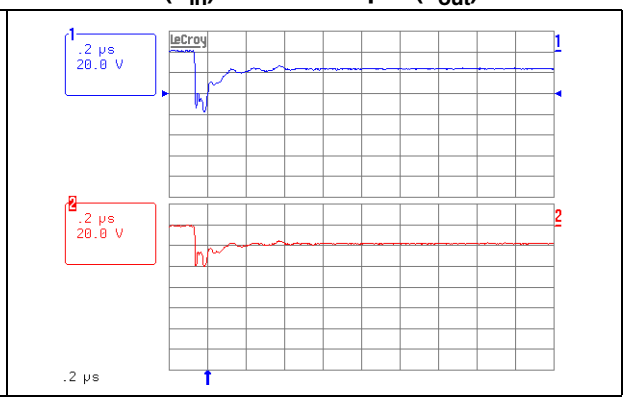
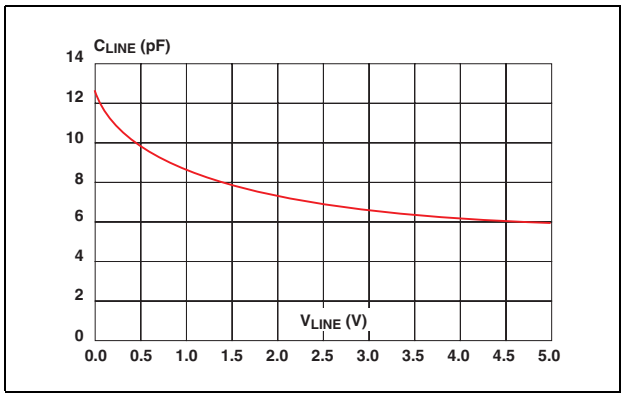
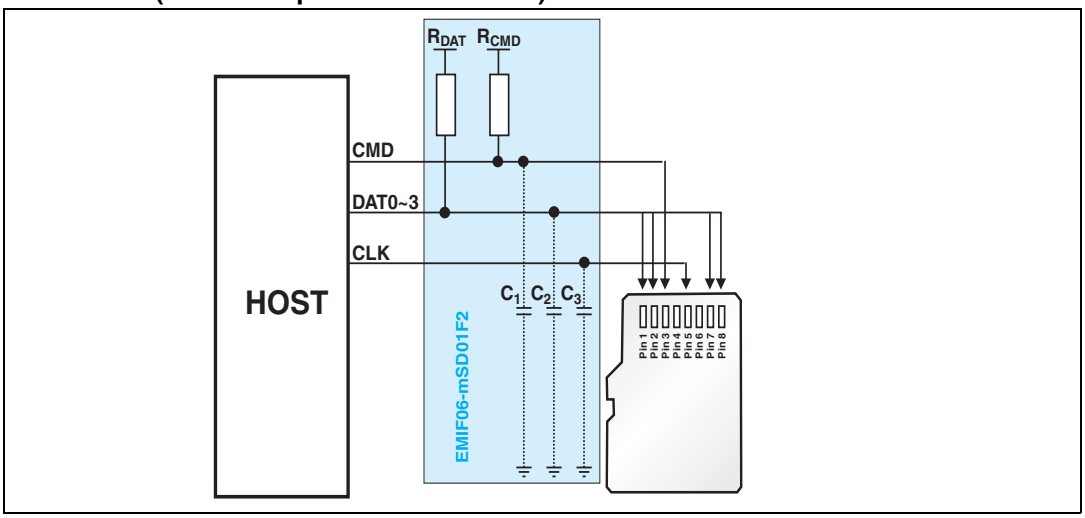


Figure 6. Junction capacitance versus reverse applied voltage CLK line (typical values)



2 Technical information

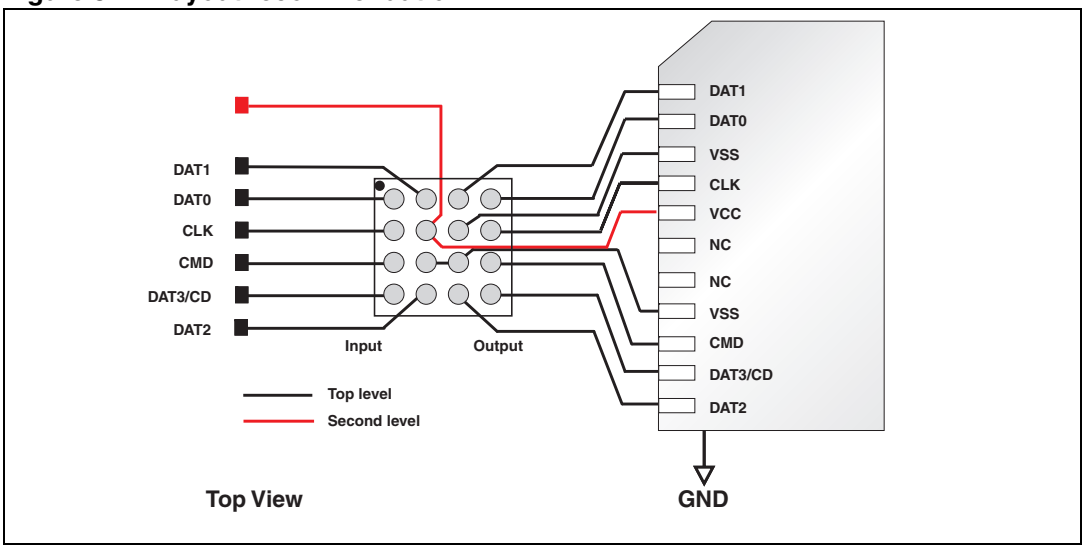
Figure 7. T-Flash connection diagram recommendation (MicroSD Specification Ver 1.0)



Pull-up resistance R_{DAT} and R_{CMD} are implemented to prevent bus floating when no card is inserted or when all card drivers are in high impedance mode. Resistance values should be set between 10 kΩ and 100 kΩ .

The pull-up resistors and capacitors described in the above recommendation are integrated in the EMIF06-mSD01F2. This makes the EMIF06-mSD01F2 an easy "plug and play" solution to implement secured T-flash, mini-SD card terminations.

Figure 8. Layout recommendation



3 Ordering information scheme

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 2: Lead free Pitch = 500 µm, Bump = 315 µm

4 Package information

Figure 9. Flip-Chip Package dimensions

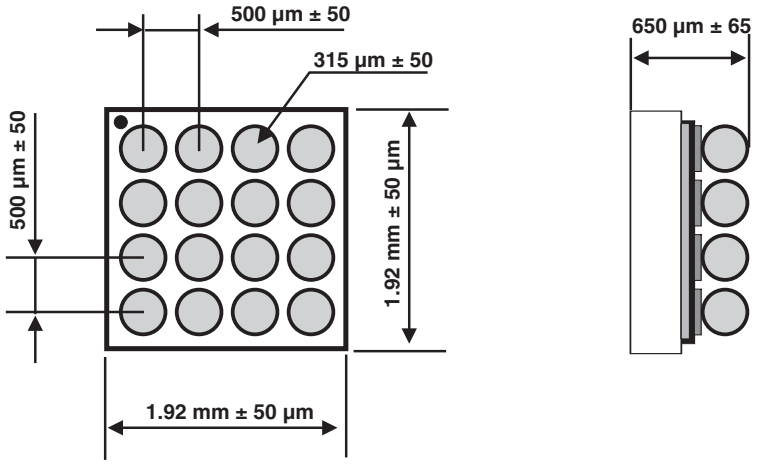


Figure 10. Foot print recommendations

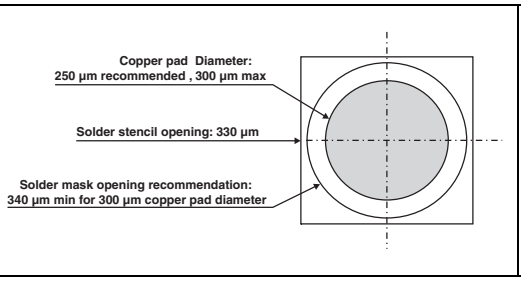


Figure 11. Marking

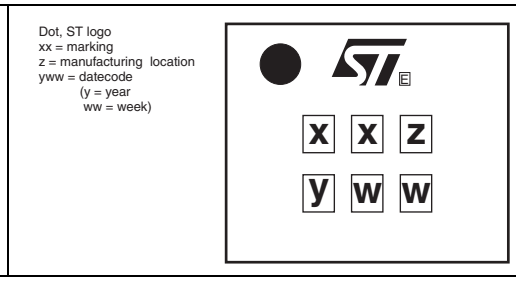
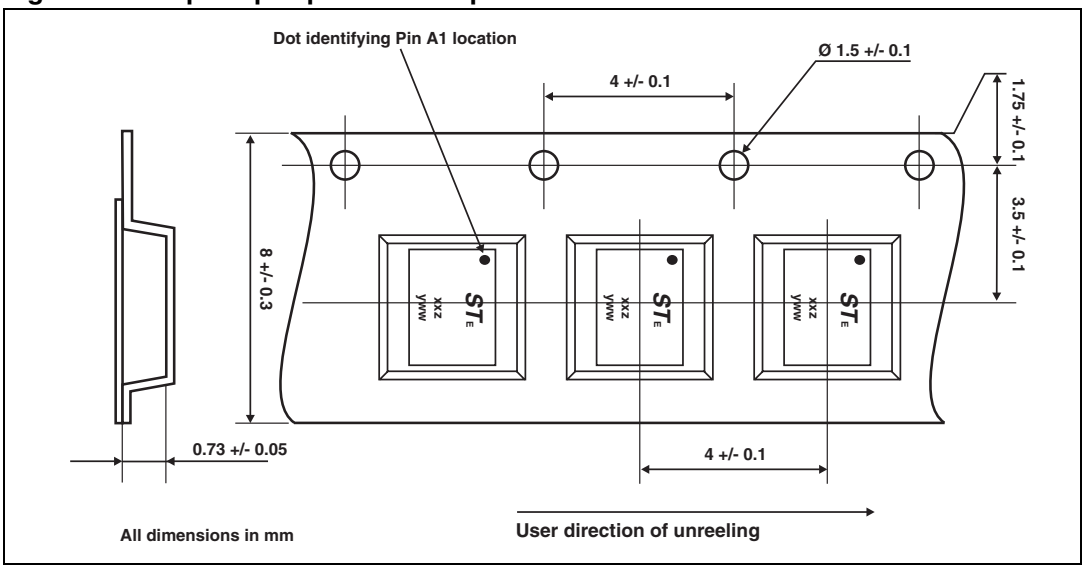


Figure 12. Flip-Chip Tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More packing information is available in the application notes:

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

5 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-mSD01F2	HJ	Flip-Chip	5.3 mg	5000	Tape and reel 7"

6 Revision history

Date	Revision	Description of Changes
02-Feb-2007	1	First issue.

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