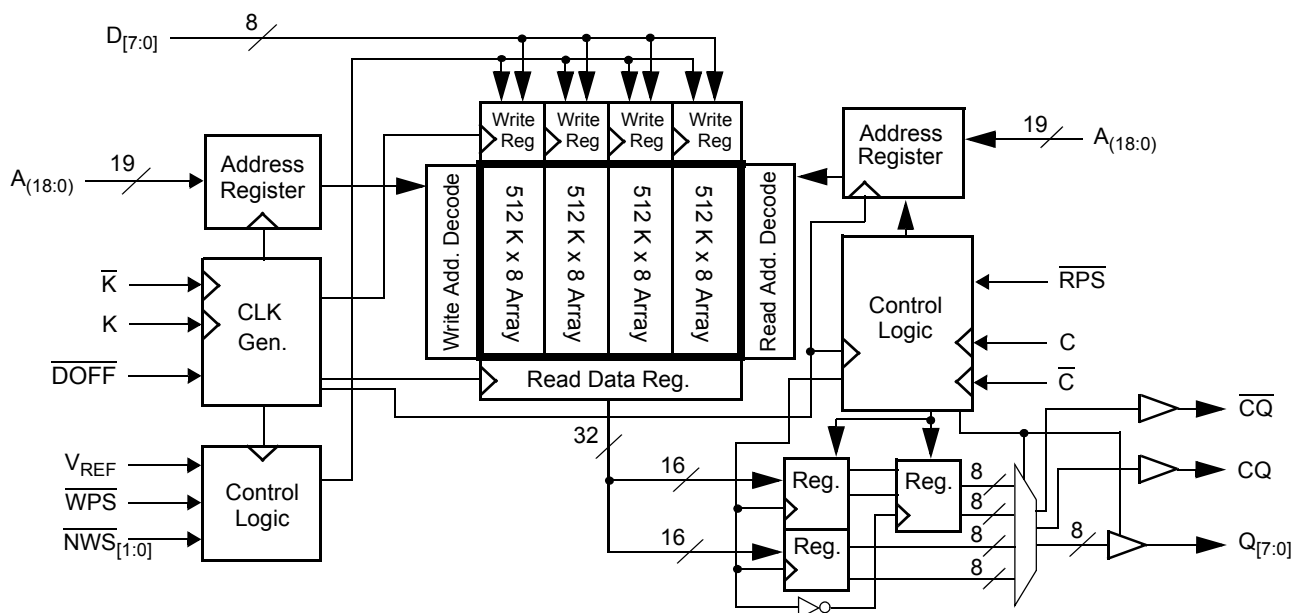
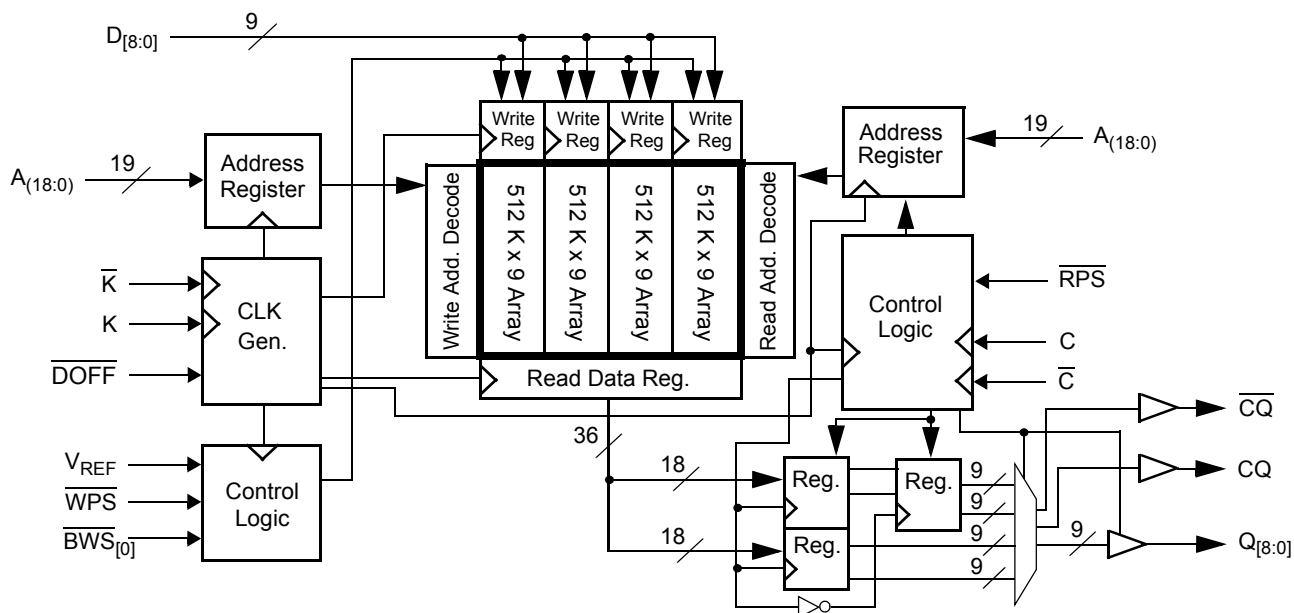
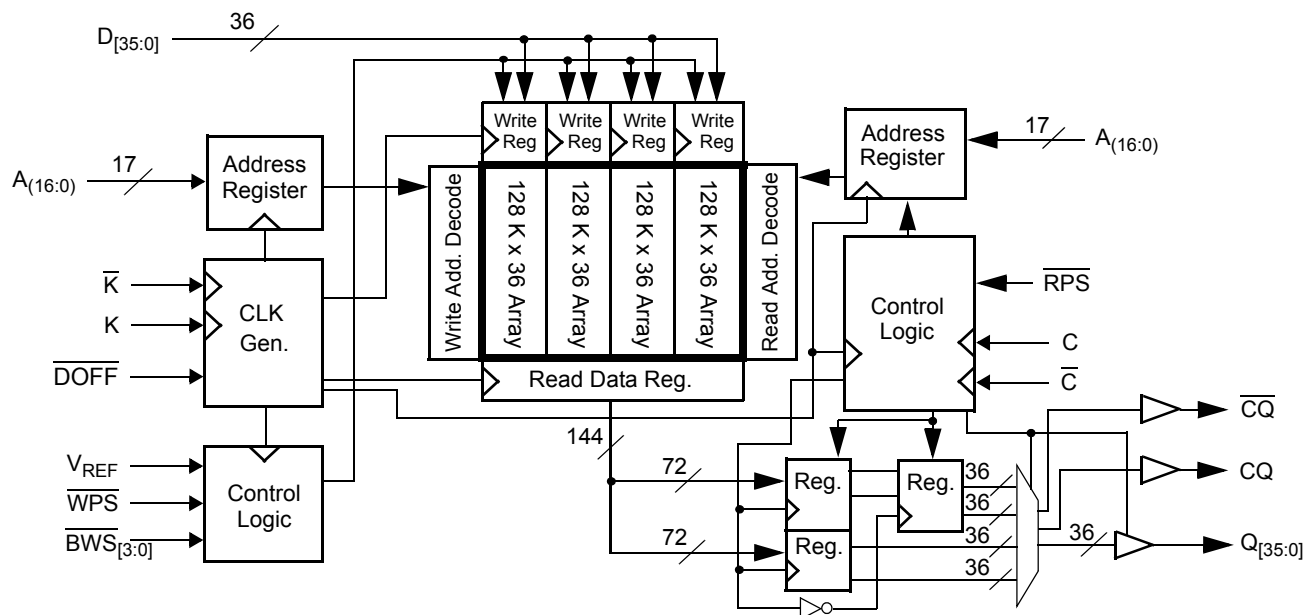
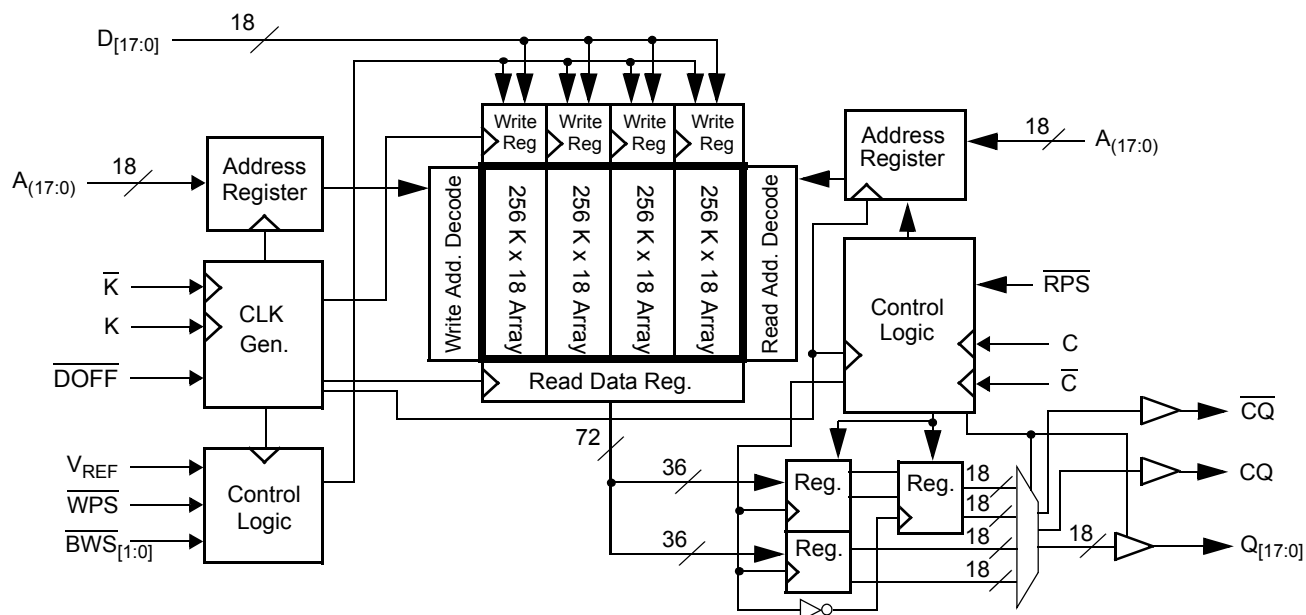


## Logic Block Diagram – CY7C1311KV18



## Logic Block Diagram – CY7C1911KV18





## Contents

<b>Pin Configurations</b> .....	<b>5</b>	<b>Instruction Codes</b> .....	<b>20</b>
<b>Pin Definitions</b> .....	<b>7</b>	<b>Boundary Scan Order</b> .....	<b>21</b>
<b>Functional Overview</b> .....	<b>8</b>	<b>Power Up Sequence in QDR II SRAM</b> .....	<b>22</b>
Read Operations .....	9	Power Up Sequence .....	22
Write Operations .....	9	PLL Constraints .....	22
Byte Write Operations .....	9	<b>Maximum Ratings</b> .....	<b>23</b>
Single Clock Mode .....	9	<b>Operating Range</b> .....	<b>23</b>
Concurrent Transactions .....	9	<b>Neutron Soft Error Immunity</b> .....	<b>23</b>
Depth Expansion .....	9	<b>Electrical Characteristics</b> .....	<b>23</b>
Programmable Impedance .....	9	DC Electrical Characteristics .....	23
Echo Clocks .....	10	AC Electrical Characteristics .....	25
PLL .....	10	<b>Capacitance</b> .....	<b>25</b>
<b>Application Example</b> .....	<b>10</b>	<b>Thermal Resistance</b> .....	<b>25</b>
<b>Truth Table</b> .....	<b>11</b>	<b>AC Test Loads and Waveforms</b> .....	<b>25</b>
<b>Write Cycle Descriptions</b> .....	<b>12</b>	<b>Switching Characteristics</b> .....	<b>26</b>
<b>Write Cycle Descriptions</b> .....	<b>12</b>	<b>Switching Waveforms</b> .....	<b>28</b>
<b>Write Cycle Descriptions</b> .....	<b>13</b>	<b>Ordering Information</b> .....	<b>29</b>
<b>IEEE 1149.1 Serial Boundary Scan (JTAG)</b> .....	<b>14</b>	Ordering Code Definitions .....	29
Disabling the JTAG Feature .....	14	<b>Package Diagram</b> .....	<b>30</b>
Test Access Port .....	14	<b>Acronyms</b> .....	<b>31</b>
Performing a TAP Reset .....	14	<b>Document Conventions</b> .....	<b>31</b>
TAP Registers .....	14	Units of Measure .....	31
TAP Instruction Set .....	14	<b>Document History Page</b> .....	<b>32</b>
<b>TAP Controller State Diagram</b> .....	<b>16</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>33</b>
<b>TAP Controller Block Diagram</b> .....	<b>17</b>	Worldwide Sales and Design Support .....	33
<b>TAP Electrical Characteristics</b> .....	<b>17</b>	Products .....	33
<b>TAP AC Switching Characteristics</b> .....	<b>18</b>	PSoC® Solutions .....	33
<b>TAP Timing and Test Conditions</b> .....	<b>19</b>	Cypress Developer Community .....	33
<b>Identification Register Definitions</b> .....	<b>20</b>	Technical Support .....	33
<b>Scan Register Sizes</b> .....	<b>20</b>		

## Pin Configurations

The pin configurations for CY7C1311KV18, CY7C1911KV18, CY7C1313KV18, and CY7C1315KV18 follow. <sup>[1]</sup>

**Figure 1. 165-ball FBGA (13 × 15 × 1.4 mm) pinout**

**CY7C1311KV18 (2M × 8)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/72M	A	$\overline{\text{WPS}}$	$\overline{\text{NWS}}_1$	$\overline{\text{K}}$	NC/144M	$\overline{\text{RPS}}$	A	NC/36M	CQ
<b>B</b>	NC	NC	NC	A	NC/288M	K	$\overline{\text{NWS}}_0$	A	NC	NC	Q3
<b>C</b>	NC	NC	NC	$V_{SS}$	A	NC	A	$V_{SS}$	NC	NC	D3
<b>D</b>	NC	D4	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>E</b>	NC	NC	Q4	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D2	Q2
<b>F</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>G</b>	NC	D5	Q5	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>H</b>	$\overline{\text{DOFF}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q1	D1
<b>K</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>L</b>	NC	Q6	D6	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q0
<b>M</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D0
<b>N</b>	NC	D7	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>P</b>	NC	NC	Q7	A	A	C	A	A	NC	NC	NC
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

**CY7C1911KV18 (2M × 9)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/72M	A	$\overline{\text{WPS}}$	NC	$\overline{\text{K}}$	NC/144M	$\overline{\text{RPS}}$	A	NC/36M	CQ
<b>B</b>	NC	NC	NC	A	NC/288M	K	$\overline{\text{BWS}}_0$	A	NC	NC	Q4
<b>C</b>	NC	NC	NC	$V_{SS}$	A	NC	A	$V_{SS}$	NC	NC	D4
<b>D</b>	NC	D5	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	NC
<b>E</b>	NC	NC	Q5	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D3	Q3
<b>F</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>G</b>	NC	D6	Q6	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>H</b>	$\overline{\text{DOFF}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q2	D2
<b>K</b>	NC	NC	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	NC
<b>L</b>	NC	Q7	D7	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q1
<b>M</b>	NC	NC	NC	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D1
<b>N</b>	NC	D8	NC	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	NC
<b>P</b>	NC	NC	Q8	A	A	C	A	A	NC	D0	Q0
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

**Note**

1. NC/36M, NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.

## Pin Configurations (continued)

The pin configurations for CY7C1311KV18, CY7C1911KV18, CY7C1313KV18, and CY7C1315KV18 follow. <sup>[1]</sup>

**Figure 1. 165-ball FBGA (13 × 15 × 1.4 mm) pinout**

**CY7C1313KV18 (1M × 18)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/144M	NC/36M	$\overline{\text{WPS}}$	$\overline{\text{BWS}}_1$	$\overline{\text{K}}$	NC/288M	$\overline{\text{RPS}}$	A	NC/72M	CQ
<b>B</b>	NC	Q9	D9	A	NC	K	$\overline{\text{BWS}}_0$	A	NC	NC	Q8
<b>C</b>	NC	NC	D10	$V_{SS}$	A	NC	A	$V_{SS}$	NC	Q7	D8
<b>D</b>	NC	D11	Q10	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D7
<b>E</b>	NC	NC	Q11	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D6	Q6
<b>F</b>	NC	Q12	D12	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	Q5
<b>G</b>	NC	D13	Q13	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	D5
<b>H</b>	$\overline{\text{DOFF}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	NC	NC	D14	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q4	D4
<b>K</b>	NC	NC	Q14	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	D3	Q3
<b>L</b>	NC	Q15	D15	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q2
<b>M</b>	NC	NC	D16	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	Q1	D2
<b>N</b>	NC	D17	Q16	$V_{SS}$	A	A	A	$V_{SS}$	NC	NC	D1
<b>P</b>	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

**CY7C1315KV18 (512K × 36)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/288M	NC/72M	$\overline{\text{WPS}}$	$\overline{\text{BWS}}_2$	$\overline{\text{K}}$	$\overline{\text{BWS}}_1$	$\overline{\text{RPS}}$	NC/36M	NC/144M	CQ
<b>B</b>	Q27	Q18	D18	A	$\overline{\text{BWS}}_3$	K	$\overline{\text{BWS}}_0$	A	D17	Q17	Q8
<b>C</b>	D27	Q28	D19	$V_{SS}$	A	NC	A	$V_{SS}$	D16	Q7	D8
<b>D</b>	D28	D20	Q19	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	Q16	D15	D7
<b>E</b>	Q29	D29	Q20	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	Q15	D6	Q6
<b>F</b>	Q30	Q21	D21	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	D14	Q14	Q5
<b>G</b>	D30	D22	Q22	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	Q13	D13	D5
<b>H</b>	$\overline{\text{DOFF}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
<b>J</b>	D31	Q31	D23	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	D12	Q4	D4
<b>K</b>	Q32	D32	Q23	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	Q12	D3	Q3
<b>L</b>	Q33	Q24	D24	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	D11	Q11	Q2
<b>M</b>	D33	Q34	D25	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	D10	Q1	D2
<b>N</b>	D34	D26	Q25	$V_{SS}$	A	A	A	$V_{SS}$	Q10	D9	D1
<b>P</b>	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

## Pin Definitions

Pin Name	I/O	Pin Description
$D_{[x:0]}$	Input-synchronous	<b>Data Input Signals.</b> Sampled on the rising edge of K and $\bar{K}$ clocks when valid write operations are active. CY7C1311KV18 – $D_{[7:0]}$ CY7C1911KV18 – $D_{[8:0]}$ CY7C1313KV18 – $D_{[17:0]}$ CY7C1315KV18 – $D_{[35:0]}$
$\overline{WPS}$	Input-synchronous	<b>Write Port Select – Active LOW.</b> Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$ .
$\overline{NWS}_0$ , $\overline{NWS}_1$	Input-synchronous	<b>Nibble Write Select 0, 1 – Active LOW (CY7C1311KV18 only).</b> Sampled on the rising edge of the K and $\bar{K}$ clocks when write operations are active. Used to select which nibble is written into the device during the current portion of the write operations. $\overline{NWS}_0$ controls $D_{[3:0]}$ and $\overline{NWS}_1$ controls $D_{[7:4]}$ . All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select ignores the corresponding nibble of data and it is not written into the device.
$\overline{BWS}_0$ , $\overline{BWS}_1$ , $\overline{BWS}_2$ , $\overline{BWS}_3$	Input-synchronous	<b>Byte Write Select 0, 1, 2, and 3 – Active LOW.</b> Sampled on the rising edge of the K and $\bar{K}$ clocks when write operations are active. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1911KV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ CY7C1313KV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9]}$ . CY7C1315KV18 – $\overline{BWS}_0$ controls $D_{[8:0]}$ , $\overline{BWS}_1$ controls $D_{[17:9]}$ , $\overline{BWS}_2$ controls $D_{[26:18]}$ and $\overline{BWS}_3$ controls $D_{[35:27]}$ . All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-synchronous	<b>Address Inputs.</b> Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 2 M × 8 (4 arrays each of 512 K × 8) for CY7C1311KV18, 2 M × 9 (4 arrays each of 512 K × 9) for CY7C1911KV18, 1 M × 18 (4 arrays each of 256 K × 18) for CY7C1313KV18 and 512 K × 36 (4 arrays each of 128 K × 36) for CY7C1315KV18. Therefore, only 19 address inputs are needed to access the entire memory array of CY7C1311KV18 and CY7C1911KV18, 18 address inputs for CY7C1313KV18 and 17 address inputs for CY7C1315KV18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-synchronous	<b>Data Output Signals.</b> These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of the C and $\bar{C}$ clocks during read operations, or K and $\bar{K}$ when in single clock mode. On deselecting the read port, $Q_{[x:0]}$ are automatically tristated. CY7C1311KV18 – $Q_{[7:0]}$ CY7C1911KV18 – $Q_{[8:0]}$ CY7C1313KV18 – $Q_{[17:0]}$ CY7C1315KV18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-synchronous	<b>Read Port Select – Active LOW.</b> Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tristated following the next rising edge of the C clock. Each read access consists of a burst of four sequential transfers.
C	Input clock	<b>Positive Input Clock for Output Data.</b> C is used in conjunction with $\bar{C}$ to clock out the read data from the device. C and $\bar{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See <a href="#">Application Example on page 10</a> for further details.
$\bar{C}$	Input clock	<b>Negative Input Clock for Output Data.</b> $\bar{C}$ is used in conjunction with C to clock out the read data from the device. C and $\bar{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See <a href="#">Application Example on page 10</a> for further details.
K	Input clock	<b>Positive Input Clock Input.</b> The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\bar{K}$	Input clock	<b>Negative Input Clock Input.</b> $\bar{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.

## Pin Definitions (continued)

Pin Name	I/O	Pin Description
CQ	Echo clock	<b>CQ Referenced with Respect to C.</b> This is a free running clock and is synchronized to the input clock for output data (C) of the QDR II. In the single clock mode, CQ is generated with respect to K. The timings for the echo clocks are shown in the <a href="#">Switching Characteristics on page 26</a> .
$\overline{\text{CQ}}$	Echo clock	<b><math>\overline{\text{CQ}}</math> Referenced with Respect to <math>\overline{\text{C}}</math>.</b> This is a free running clock and is synchronized to the input clock for output data ( $\overline{\text{C}}$ ) of the QDR II. In the single clock mode, $\overline{\text{CQ}}$ is generated with respect to K. The timings for the echo clocks are shown in the <a href="#">Switching Characteristics on page 26</a> .
ZQ	Input	<b>Output Impedance Matching Input.</b> This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{\text{CQ}}$ , and $\text{Q}_{[x:0]}$ output impedance are set to $0.2 \times \text{RQ}$ , where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to $\text{V}_{\text{DDQ}}$ , which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
DOFF	Input	<b>PLL Turn Off – Active LOW.</b> Connecting this pin to ground turns off the PLL inside the device. The timings in the PLL turned off operation differs from those listed in this data sheet. For normal operation, this pin is connected to a pull up through a 10 k $\Omega$ or less pull up resistor. The device behaves in QDR I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR I timing.
TDO	Output	<b>TDO Pin for JTAG.</b>
TCK	Input	<b>TCK Pin for JTAG.</b>
TDI	Input	<b>TDI Pin for JTAG.</b>
TMS	Input	<b>TMS Pin for JTAG.</b>
NC	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/36M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/72M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/144M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/288M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
$\text{V}_{\text{REF}}$	Input-reference	<b>Reference Voltage Input.</b> Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
$\text{V}_{\text{DD}}$	Power supply	<b>Power Supply Inputs to the Core of the Device.</b>
$\text{V}_{\text{SS}}$	Ground	<b>Ground for the Device.</b>
$\text{V}_{\text{DDQ}}$	Power supply	<b>Power Supply Inputs for the Outputs of the Device.</b>

## Functional Overview

The CY7C1311KV18, CY7C1911KV18, CY7C1313KV18, CY7C1315KV18 are synchronous pipelined Burst SRAMs with a read port and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and flows out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR II completely eliminates the need to turn around the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of four 8-bit data transfers in the case of CY7C1311KV18, four 9-bit data transfers in the case of CY7C1911KV18, four 18-bit data transfers in the case of CY7C1313KV18, and four 36-bit data transfers in the case of CY7C1315KV18 in two clock cycles.

This device operates with a read latency of one and half cycles when DOFF pin is tied HIGH. When DOFF pin is set LOW or connected to  $\text{V}_{\text{SS}}$  then device behaves in QDR I mode with a read latency of one clock cycle.

Accesses for both ports are initiated on the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and  $\overline{\text{K}}$ ) and all output timing is referenced to the output clocks (C and  $\overline{\text{C}}$ , or K and  $\overline{\text{K}}$  when in single clock mode).

All synchronous data inputs ( $\text{D}_{[x:0]}$ ) pass through input registers controlled by the input clocks (K and  $\overline{\text{K}}$ ). All synchronous data outputs ( $\text{Q}_{[x:0]}$ ) pass through output registers controlled by the rising edge of the output clocks (C and  $\overline{\text{C}}$ , or K and  $\overline{\text{K}}$  when in single clock mode).

All synchronous control ( $\overline{\text{RPS}}$ ,  $\overline{\text{WPS}}$ ,  $\overline{\text{BWS}}_{[x:0]}$ ) inputs pass through input registers controlled by the rising edge of the input clocks (K and  $\overline{\text{K}}$ ).



CY7C1313KV18 is described in the following sections. The same basic descriptions apply to CY7C1311KV18, CY7C1911KV18 and CY7C1315KV18.

## Read Operations

The CY7C1313KV18 is organized internally as four arrays of 256 K × 18. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting  $\overline{RPS}$  active at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next K clock rise, the corresponding lowest order 18-bit word of data is driven onto the  $Q_{[17:0]}$  using  $\overline{C}$  as the output timing reference. On the subsequent rising edge of  $\overline{C}$ , the next 18-bit data word is driven onto the  $Q_{[17:0]}$ . This process continues until all four 18-bit data words are driven out onto  $Q_{[17:0]}$ . The requested data is valid 0.45 ns from the rising edge of the output clock ( $\overline{C}$  or  $\overline{C}$ , or K or K when in single clock mode). To maintain the internal logic, each read access must be enabled to complete. Each read access consists of four 18-bit data words and takes two clock cycles to complete. Therefore, read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second read request. Read accesses can be initiated on every other K clock rise. Doing so pipelines the data flow such that data is transferred out of the device on every rising edge of the output clocks ( $\overline{C}$  and  $\overline{C}$ , or K and K when in single clock mode).

When the read port is deselected, the CY7C1313KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tristates the outputs following the next rising edge of the positive output clock ( $\overline{C}$ ). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

## Write Operations

Write operations are initiated by asserting  $\overline{WPS}$  active at the rising edge of the positive input clock (K). On the following K clock rise the data presented to  $D_{[17:0]}$  is latched and stored into the lower 18-bit write data register, provided  $\overline{BWS}_{[1:0]}$  are both asserted active. On the subsequent rising edge of the negative input clock (K) the information presented to  $D_{[17:0]}$  is also stored into the write data register, provided  $\overline{BWS}_{[1:0]}$  are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, write accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second write request. Write accesses can be initiated on every other rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and K).

When deselected, the write port ignores all inputs after the pending write operations are completed.

## Byte Write Operations

Byte write operations are supported by the CY7C1313KV18. A write operation is initiated as described in the [Write Operations](#) section. The bytes that are written are determined by  $\overline{BWS}_0$  and

$\overline{BWS}_1$ , which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature is used to simplify read, modify, or write operations to a byte write operation.

## Single Clock Mode

The CY7C1313KV18 is used with a single clock that controls both the input and output registers. In this mode the device recognizes only a single pair of input clocks (K and K) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/K and C/C clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and  $\overline{C}$  HIGH at power on. This function is a strap option and not alterable during device operation.

## Concurrent Transactions

The read and write ports on the CY7C1313KV18 operate independently of one another. As each port latches the address inputs on different clock edges, the user can read or write to any location, regardless of the transaction on the other port. If the ports access the same location when a read follows a write in successive clock cycles, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Read access and write access must be scheduled such that one transaction is initiated on any clock cycle. If both ports are selected on the same K clock rise, the arbitration depends on the previous state of the SRAM. If both ports are deselected, the read port takes priority. If a read was initiated on the previous cycle, the write port takes priority (as read operations cannot be initiated on consecutive cycles). If a write was initiated on the previous cycle, the read port takes priority (as write operations cannot be initiated on consecutive cycles). Therefore, asserting both port selects active from a deselected state results in alternating read or write operations being initiated, with the first access being a read.

## Depth Expansion

The CY7C1313KV18 has a port select input for each port. This enables for easy depth expansion. Both port selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting a port does not affect the other port. All pending transactions (read and write) are completed before the device is deselected.

## Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and  $V_{SS}$  to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5 × the value of the intended line impedance driven by the SRAM, the allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with  $V_{DDQ} = 1.5$  V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.



## Echo Clocks

Echo clocks are provided on the QDR II to simplify data capture on high speed systems. Two echo clocks are generated by the QDR II. CQ is referenced with respect to C and  $\overline{CQ}$  is referenced with respect to  $\overline{C}$ . These are free running clocks and are synchronized to the output clock of the QDR II. In the single clock mode, CQ is generated with respect to K and  $\overline{CQ}$  is generated with respect to  $\overline{K}$ . The timing for the echo clocks is shown in the [Switching Characteristics on page 26](#).

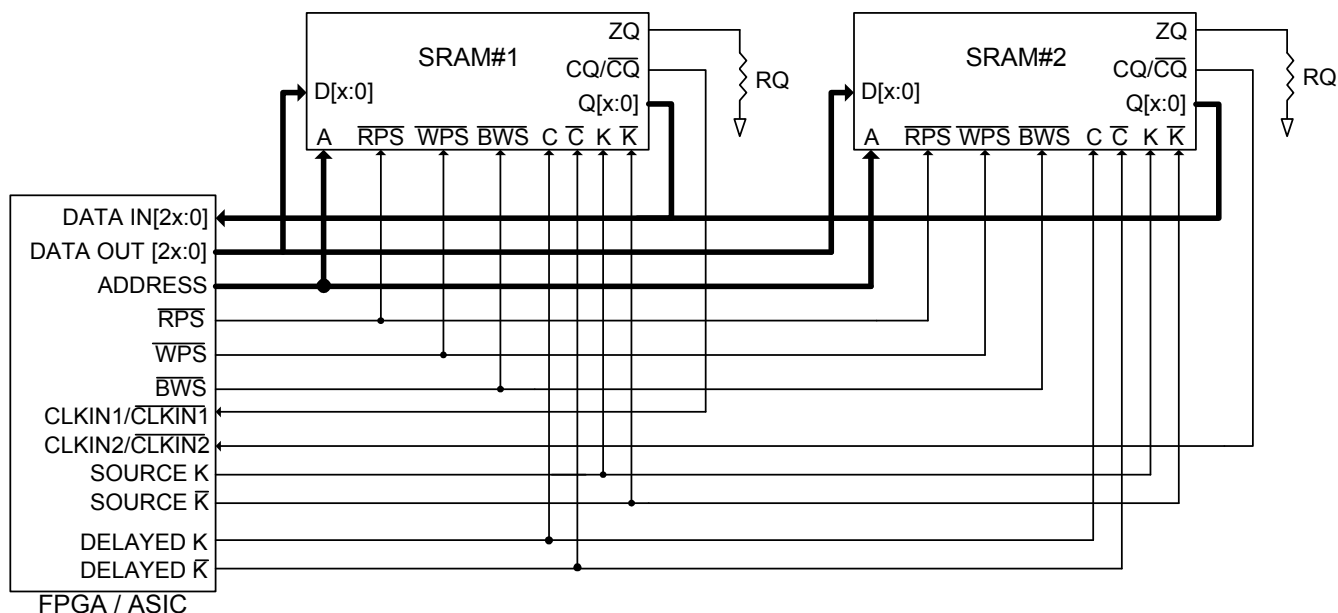
## PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the  $\overline{DOFF}$  is tied HIGH, the PLL is locked after 20  $\mu$ s of stable clock. The PLL can also be reset by slowing or stopping the input clocks K and  $\overline{K}$  for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20  $\mu$ s after a stable clock is presented. The PLL may be disabled by applying ground to the  $\overline{DOFF}$  pin. When the PLL is turned off, the device behaves in QDR I mode (with one cycle latency and a longer access time).

## Application Example

Figure 2 shows four QDR II used in an application.

**Figure 2. Application Example (Width Expansion)**



## Truth Table

The truth table for CY7C1311KV18, CY7C1911KV18, CY7C1313KV18, and CY7C1315KV18 follow. [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{\text{RPS}}$	$\overline{\text{WPS}}$	DQ	DQ	DQ	DQ
Write cycle: Load address on the rising edge of K; input write data on two consecutive K and $\overline{\text{K}}$ rising edges.	L–H	H <sup>[8]</sup>	L <sup>[9]</sup>	D(A) at K(t + 1)↑	D(A + 1) at $\overline{\text{K}}$ (t + 1)↑	D(A + 2) at K(t + 2)↑	D(A + 3) at $\overline{\text{K}}$ (t + 2)↑
Read cycle: Load address on the rising edge of K; wait one and a half cycle; read data on two consecutive $\overline{\text{C}}$ and C rising edges.	L–H	L <sup>[9]</sup>	X	Q(A) at $\overline{\text{C}}$ (t + 1)↑	Q(A + 1) at C(t + 2)↑	Q(A + 2) at $\overline{\text{C}}$ (t + 2)↑	Q(A + 3) at C(t + 3)↑
NOP: No operation	L–H	H	H	D = X Q = High Z	D = X Q = High Z	D = X Q = High Z	D = X Q = High Z
Standby: Clock stopped	Stopped	X	X	Previous state	Previous state	Previous state	Previous state

### Notes

- X = 'Don't Care', H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
- Device powers up deselected with the outputs in a tristate condition.
- 'A' represents address location latched by the devices when transaction was initiated. A + 1, A + 2, and A + 3 represents the address sequence in the burst.
- 't' represents the cycle at which a read/write operation is started. t + 1, t + 2, and t + 3 are the first, second and third clock cycles respectively succeeding the 't' clock cycle.
- Data inputs are registered at K and  $\overline{\text{K}}$  rising edges. Data outputs are delivered on C and  $\overline{\text{C}}$  rising edges, except when in single clock mode.
- Ensure that when the clock is stopped K = K and C = C = HIGH. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
- If this signal was LOW to initiate the previous cycle, this signal becomes a 'Don't Care' for this operation.
- This signal was HIGH on previous K clock rise. Initiating consecutive read or write operations on consecutive K clock rises is not permitted. The device ignores the second read or write request.

## Write Cycle Descriptions

The write cycle description table for CY7C1311KV18 and CY7C1313KV18 are as follows. <sup>[10, 11]</sup>

$\overline{\text{BWS}}_0$ / $\overline{\text{NWS}}_0$	$\overline{\text{BWS}}_1$ / $\overline{\text{NWS}}_1$	K	$\overline{\text{K}}$	Comments
L	L	L–H	–	During the data portion of a write sequence: CY7C1311KV18 – both nibbles ( $D_{[7:0]}$ ) are written into the device. CY7C1313KV18 – both bytes ( $D_{[17:0]}$ ) are written into the device.
L	L	–	L–H	During the data portion of a write sequence: CY7C1311KV18 – both nibbles ( $D_{[7:0]}$ ) are written into the device. CY7C1313KV18 – both bytes ( $D_{[17:0]}$ ) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: CY7C1311KV18 – only the lower nibble ( $D_{[3:0]}$ ) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1313KV18 – only the lower byte ( $D_{[8:0]}$ ) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: CY7C1311KV18 – only the lower nibble ( $D_{[3:0]}$ ) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1313KV18 – only the lower byte ( $D_{[8:0]}$ ) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: CY7C1311KV18 – only the upper nibble ( $D_{[7:4]}$ ) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1313KV18 – only the upper byte ( $D_{[17:9]}$ ) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: CY7C1311KV18 – only the upper nibble ( $D_{[7:4]}$ ) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1313KV18 – only the upper byte ( $D_{[17:9]}$ ) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

## Write Cycle Descriptions

The write cycle description table for CY7C1911KV18 is as follows. <sup>[10, 11]</sup>

$\overline{\text{BWS}}_0$	K	$\overline{\text{K}}$	Comments
L	L–H	–	During the data portion of a write sequence, the single byte ( $D_{[8:0]}$ ) is written into the device.
L	–	L–H	During the data portion of a write sequence, the single byte ( $D_{[8:0]}$ ) is written into the device.
H	L–H	–	No data is written into the device during this portion of a write operation.
H	–	L–H	No data is written into the device during this portion of a write operation.

### Notes

10. X = 'Don't Care', H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.

11. Is based on a write cycle that was initiated in accordance with the [Truth Table on page 11](#).  $\overline{\text{NWS}}_0$ ,  $\overline{\text{NWS}}_1$ ,  $\overline{\text{BWS}}_0$ ,  $\overline{\text{BWS}}_1$ ,  $\overline{\text{BWS}}_2$ , and  $\overline{\text{BWS}}_3$  can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

## Write Cycle Descriptions

The write cycle description table for CY7C1315KV18 follows. [12, 13]

$\overline{\text{BWS}}_0$	$\overline{\text{BWS}}_1$	$\overline{\text{BWS}}_2$	$\overline{\text{BWS}}_3$	K	$\overline{\text{K}}$	Comments
L	L	L	L	L-H	-	During the data portion of a write sequence, all four bytes ( $D_{[35:0]}$ ) are written into the device.
L	L	L	L	-	L-H	During the data portion of a write sequence, all four bytes ( $D_{[35:0]}$ ) are written into the device.
L	H	H	H	L-H	-	During the data portion of a write sequence, only the lower byte ( $D_{[8:0]}$ ) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	-	L-H	During the data portion of a write sequence, only the lower byte ( $D_{[8:0]}$ ) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[17:9]}$ ) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[17:9]}$ ) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[26:18]}$ ) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[26:18]}$ ) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[35:27]}$ ) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[35:27]}$ ) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L-H	No data is written into the device during this portion of a write operation.

### Notes

12. X = 'Don't Care', H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.

13. Is based on a write cycle that was initiated in accordance with the [Truth Table on page 11](#) table.  $\overline{\text{NWS}}_0$ ,  $\overline{\text{NWS}}_1$ ,  $\overline{\text{BWS}}_0$ ,  $\overline{\text{BWS}}_1$ ,  $\overline{\text{BWS}}_2$ , and  $\overline{\text{BWS}}_3$  can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8 V I/O logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to  $V_{DD}$  through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

### Test Access Port

#### Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

#### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the [TAP Controller State Diagram on page 16](#). TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

#### Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see [Instruction Codes on page 20](#)). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This reset does not affect the operation of the SRAM and can be performed when the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### Instruction Register

Three-bit instructions are serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in [TAP Controller Block Diagram on page 17](#). Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary '01' pattern to allow for fault isolation of the board level serial test path.

#### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that is placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions are used to capture the contents of the input and output ring.

The [Boundary Scan Order on page 21](#) shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in [Identification Register Definitions on page 20](#).

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in [Instruction Codes on page 20](#). Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

### **IDCODE**

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

### **SAMPLE Z**

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

### **SAMPLE/PRELOAD**

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

### **BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### **EXTEST**

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

### **EXTEST OUTPUT BUS TRISTATE**

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the 'extest output bus tristate', is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

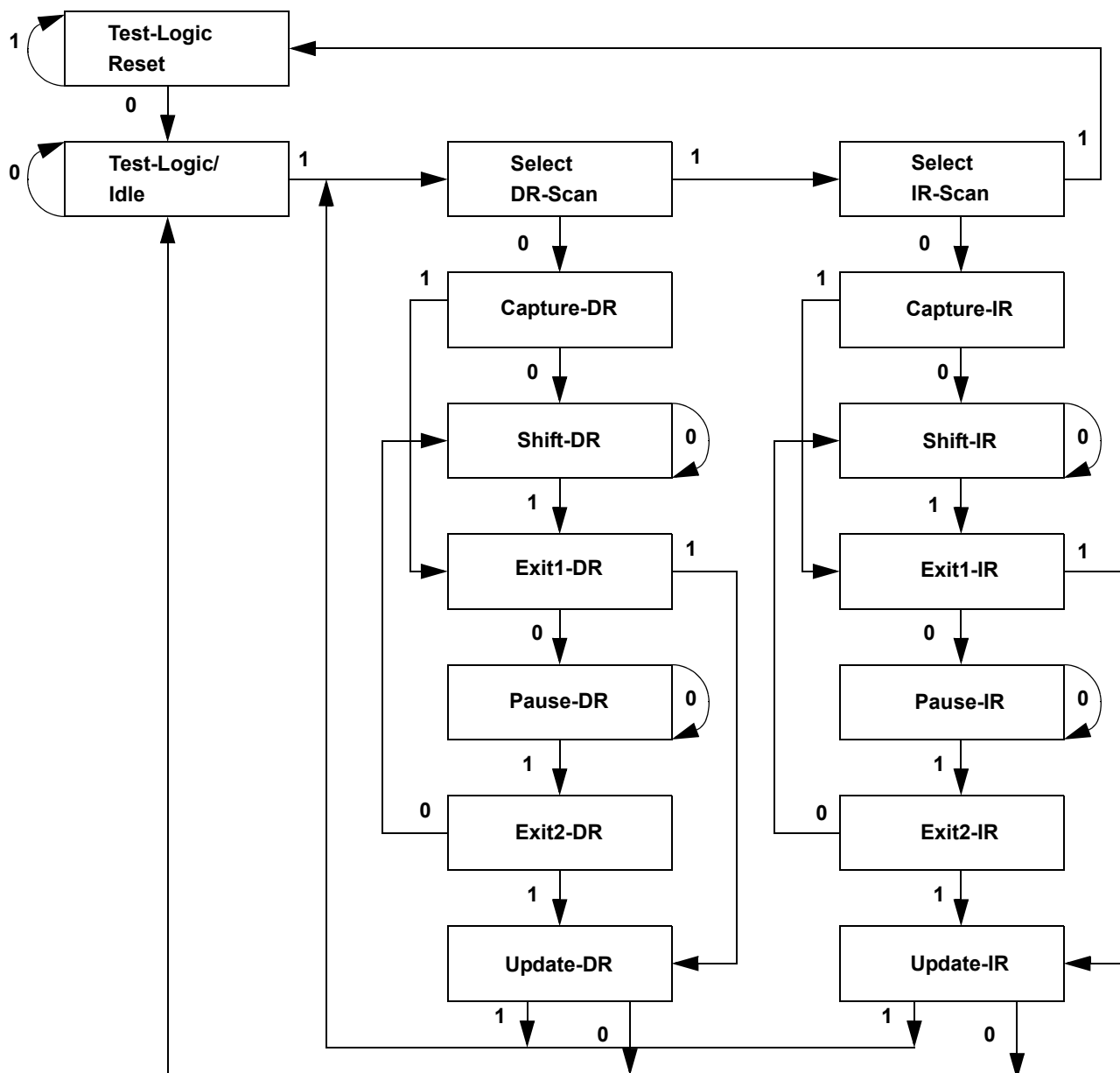
This bit is set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

### **Reserved**

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

The state diagram for the TAP controller follows. <sup>[14]</sup>

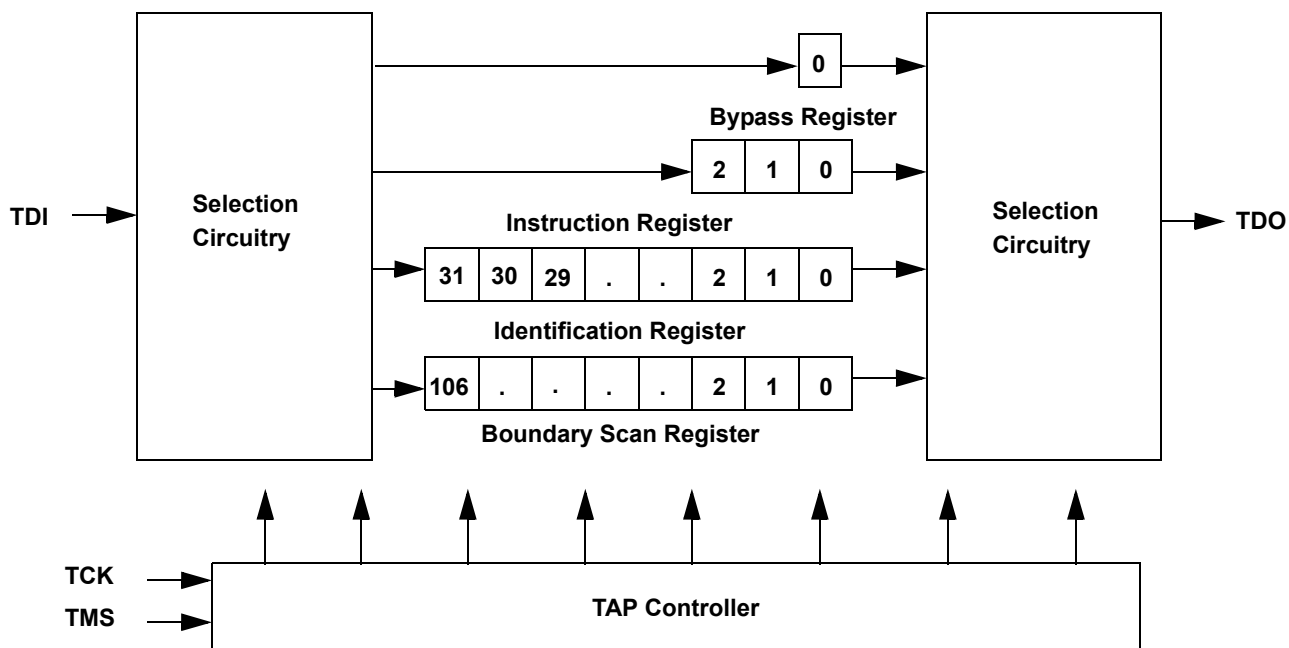


### Note

14. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.



## TAP Controller Block Diagram



## TAP Electrical Characteristics

Over the Operating Range

Parameter <sup>[15, 16, 17]</sup>	Description	Test Conditions	Min	Max	Unit
V <sub>OH1</sub>	Output HIGH voltage	I <sub>OH</sub> = -2.0 mA	1.4	—	V
V <sub>OH2</sub>	Output HIGH voltage	I <sub>OH</sub> = -100 µA	1.6	—	V
V <sub>OL1</sub>	Output LOW voltage	I <sub>OL</sub> = 2.0 mA	—	0.4	V
V <sub>OL2</sub>	Output LOW voltage	I <sub>OL</sub> = 100 µA	—	0.2	V
V <sub>IH</sub>	Input HIGH voltage	—	0.65 × V <sub>DD</sub>	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage	—	-0.3	0.35 × V <sub>DD</sub>	V
I <sub>X</sub>	Input and output load current	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	-5	5	µA

### Notes

15. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the [Electrical Characteristics on page 23](#).

16. Overshoot: V<sub>IH(AC)</sub> < V<sub>DDQ</sub> + 0.85 V (Pulse width less than t<sub>CYC/2</sub>), Undershoot: V<sub>IL(AC)</sub> > -1.5 V (Pulse width less than t<sub>CYC/2</sub>).

17. All voltage referenced to Ground.

## TAP AC Switching Characteristics

Over the Operating Range

Parameter <sup>[18, 19]</sup>	Description	Min	Max	Unit
$t_{TCYC}$	TCK Clock Cycle Time	50	–	ns
$t_{TF}$	TCK Clock Frequency	–	20	MHz
$t_{TH}$	TCK Clock HIGH	20	–	ns
$t_{TL}$	TCK Clock LOW	20	–	ns
<b>Setup Times</b>				
$t_{TMSS}$	TMS Setup to TCK Clock Rise	5	–	ns
$t_{TDIS}$	TDI Setup to TCK Clock Rise	5	–	ns
$t_{CS}$	Capture Setup to TCK Rise	5	–	ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK Clock Rise	5	–	ns
$t_{TDIH}$	TDI Hold after Clock Rise	5	–	ns
$t_{CH}$	Capture Hold after Clock Rise	5	–	ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid	–	10	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0	–	ns

### Notes

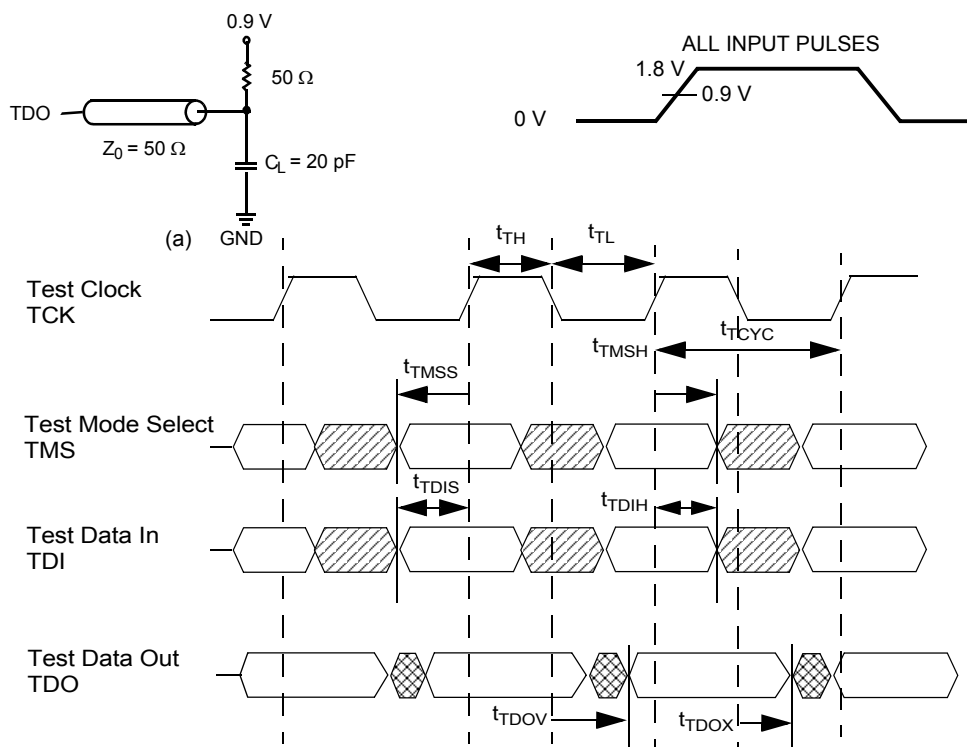
18.  $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.

19. Test conditions are specified using the load in TAP AC Test Conditions.  $t_P/t_F = 1$  ns.

## TAP Timing and Test Conditions

Figure 3 shows the TAP timing and test conditions. [20]

**Figure 3. TAP Timing and Test Conditions**



### Note

20. Test conditions are specified using the load in TAP AC Test Conditions.  $t_R/t_F = 1 \text{ ns}$ .

## Identification Register Definitions

Instruction Field	Value				Description
	CY7C1311KV18	CY7C1911KV18	CY7C1313KV18	CY7C1315KV18	
Revision number (31:29)	000	000	000	000	Version number.
Cypress device ID (28:12)	11010011011000101	11010011011001101	11010011011010101	11010011011100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID register presence (0)	1	1	1	1	Indicates the presence of an ID register.

## Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

## Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

## Boundary Scan Order

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
0	6R	28	10G	56	6A	84	2J
1	6P	29	9G	57	5B	85	3K
2	6N	30	11F	58	5A	86	3J
3	7P	31	11G	59	4A	87	2K
4	7N	32	9F	60	5C	88	1K
5	7R	33	10F	61	4B	89	2L
6	8R	34	11E	62	3A	90	3L
7	8P	35	10E	63	1H	91	1M
8	9R	36	10D	64	1A	92	1L
9	11P	37	9E	65	2B	93	3N
10	10P	38	10C	66	3B	94	3M
11	10N	39	11D	67	1C	95	1N
12	9P	40	9C	68	1B	96	2M
13	10M	41	9D	69	3D	97	3P
14	11N	42	11B	70	3C	98	2N
15	9M	43	11C	71	1D	99	2P
16	9N	44	9B	72	2C	100	1P
17	11L	45	10B	73	3E	101	3R
18	11M	46	11A	74	2D	102	4R
19	9L	47	Internal	75	2E	103	4P
20	10L	48	9A	76	1E	104	5P
21	11K	49	8B	77	2F	105	5N
22	10K	50	7C	78	3F	106	5R
23	9J	51	6C	79	1G		
24	9K	52	8A	80	1F		
25	10J	53	7A	81	3G		
26	11J	54	7B	82	2G		
27	11H	55	6B	83	1J		

## Power Up Sequence in QDR II SRAM

QDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

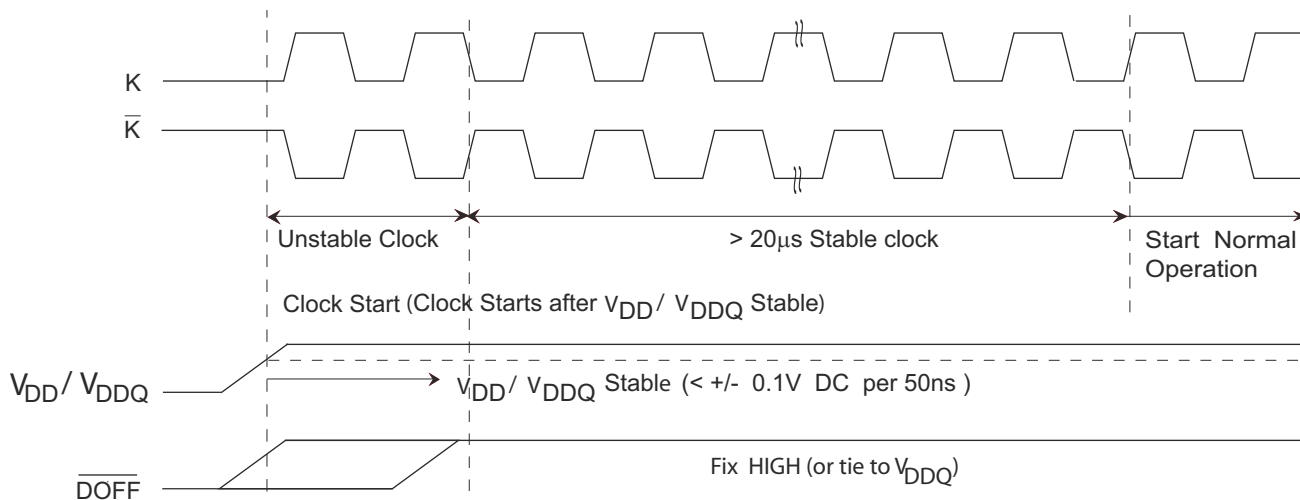
### Power Up Sequence

- Apply power and drive  $\overline{\text{DOFF}}$  either HIGH or LOW (All other inputs can be HIGH or LOW).
  - Apply  $V_{\text{DD}}$  before  $V_{\text{DDQ}}$ .
  - Apply  $V_{\text{DDQ}}$  before  $V_{\text{REF}}$  or at the same time as  $V_{\text{REF}}$ .
  - Drive  $\overline{\text{DOFF}}$  HIGH.
- Provide stable  $\overline{\text{DOFF}}$  (HIGH), power and clock ( $K, \bar{K}$ ) for 20  $\mu\text{s}$  to lock the PLL.

### PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as  $t_{\text{KC Var}}$ .
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20  $\mu\text{s}$  of stable clock to relock to the desired clock frequency.

**Figure 4. Power Up Waveforms**



## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{DD}$  relative to GND ..... -0.5 V to +2.9 V

Supply voltage on  $V_{DDQ}$  relative to GND ..... -0.5 V to + $V_{DD}$

DC applied to outputs in High Z ..... -0.5 V to  $V_{DDQ} + 0.3$  V

DC input voltage <sup>[21]</sup> ..... -0.5 V to  $V_{DD} + 0.3$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, M. 3015) ..... > 2001 V

Latch up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ )	$V_{DD}$ <sup>[22]</sup>	$V_{DDQ}$ <sup>[22]</sup>
Commercial	0 °C to +70 °C	1.8 ± 0.1 V	1.4 V to $V_{DD}$
Industrial	-40 °C to +85 °C		

## Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	197	216	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note [Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates - AN54908](#)

## Electrical Characteristics

Over the Operating Range

### DC Electrical Characteristics

Over the Operating Range

Parameter <sup>[23]</sup>	Description	Test Conditions	Min	Typ	Max	Unit
$V_{DD}$	Power supply voltage	—	1.7	1.8	1.9	V
$V_{DDQ}$	I/O supply voltage	—	1.4	1.5	$V_{DD}$	V
$V_{OH}$	Output HIGH voltage	Note 24	$V_{DDQ}/2 - 0.12$	—	$V_{DDQ}/2 + 0.12$	V
$V_{OL}$	Output LOW voltage	Note 25	$V_{DDQ}/2 - 0.12$	—	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH voltage	$I_{OH} = -0.1$ mA, nominal impedance	$V_{DDQ} - 0.2$	—	$V_{DDQ}$	V
$V_{OL(LOW)}$	Output LOW voltage	$I_{OL} = 0.1$ mA, nominal impedance	$V_{SS}$	—	0.2	V
$V_{IH}$	Input HIGH voltage	—	$V_{REF} + 0.1$	—	$V_{DDQ} + 0.3$	V
$V_{IL}$	Input LOW voltage	—	-0.3	—	$V_{REF} - 0.1$	V
$I_X$	Input leakage current	$GND \leq V_I \leq V_{DDQ}$	-5	—	5	μA
$I_{OZ}$	Output leakage current	$GND \leq V_I \leq V_{DDQ}$ , output disabled	-5	—	5	μA
$V_{REF}$	Input reference voltage <sup>[26]</sup>	Typical value = 0.75 V	0.68	0.75	0.95	V

### Notes

21. Overshoot:  $V_{IH(AC)} < V_{DDQ} + 0.85$  V (Pulse width less than  $t_{CYC}/2$ ), Undershoot:  $V_{IL(AC)} > -1.5$  V (Pulse width less than  $t_{CYC}/2$ ).

22. Power up: Assumes a linear ramp from 0 V to  $V_{DD(min)}$  within 200 ms. During this time  $V_{IH} < V_{DD}$  and  $V_{DDQ} \leq V_{DD}$ .

23. All voltage referenced to Ground.

24. Output are impedance controlled.  $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$  for values of 175 ohms  $\leq RQ \leq 350$  Ω.

25. Output are impedance controlled.  $I_{OL} = (V_{DDQ}/2)/(RQ/5)$  for values of 175 ohms  $\leq RQ \leq 350$  ohms.

26.  $V_{REF(min)} = 0.68$  V or  $0.46 V_{DDQ}$ , whichever is larger,  $V_{REF(max)} = 0.95$  V or  $0.54 V_{DDQ}$ , whichever is smaller.



## Electrical Characteristics (continued)

Over the Operating Range

### DC Electrical Characteristics (continued)

Over the Operating Range

Parameter <sup>[23]</sup>	Description	Test Conditions			Min	Typ	Max	Unit
I <sub>DD</sub> <sup>[27]</sup>	V <sub>DD</sub> operating supply	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	333 MHz	(× 9)	–	–	520	mA
				(× 18)	–	–	530	
				(× 36)	–	–	730	
			300 MHz	(× 9)	–	–	490	mA
				(× 18)	–	–	500	
				(× 36)	–	–	670	
			250 MHz	(× 8)	–	–	430	mA
				(× 9)	–	–	430	
				(× 18)	–	–	440	
		(× 36)		–	–	590		
I <sub>SB1</sub>	Automatic power down current	Max V <sub>DD</sub> , Both ports deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> f = f <sub>MAX</sub> = 1/t <sub>CYC</sub> , inputs static	333 MHz	(× 9)	–	–	270	mA
				(× 18)	–	–	270	
				(× 36)	–	–	270	
			300 MHz	(× 9)	–	–	260	mA
				(× 18)	–	–	260	
				(× 36)	–	–	260	
			250 MHz	(× 8)	–	–	250	mA
				(× 9)	–	–	250	
				(× 18)	–	–	250	
		(× 36)		–	–	250		

#### Note

27. The operation current is calculated with 50% read cycle and 50% write cycle.

## AC Electrical Characteristics

Over the Operating Range

Parameter <sup>[28]</sup>	Description	Test Conditions	Min	Typ	Max	Unit
$V_{IH}$	Input HIGH voltage	—	$V_{REF} + 0.2$	—	—	V
$V_{IL}$	Input LOW voltage	—	—	—	$V_{REF} - 0.2$	V

## Capacitance

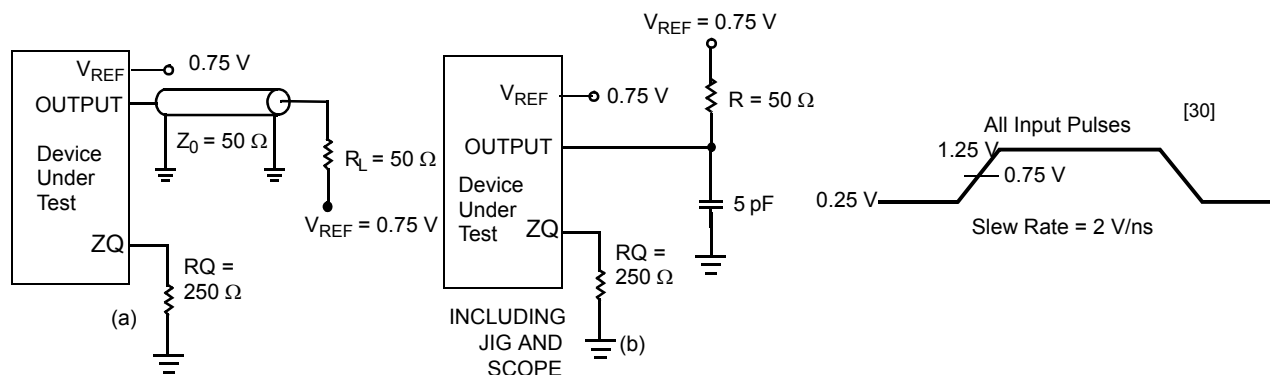
Parameter <sup>[29]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 1.8\text{ V}$ , $V_{DDQ} = 1.5\text{ V}$	4	pF
$C_O$	Output capacitance		4	pF

## Thermal Resistance

Parameter <sup>[29]</sup>	Description	Test Conditions	165-ball FBGA Package	Unit
$\theta_{JA}$ (0 m/s)	Thermal resistance (junction to ambient)	Socketed on a $170 \times 220 \times 2.35\text{ mm}$ , eight-layer printed circuit board	18.96	$^\circ\text{C/W}$
$\theta_{JA}$ (1 m/s)			17.89	$^\circ\text{C/W}$
$\theta_{JA}$ (3 m/s)			17.12	$^\circ\text{C/W}$
$\theta_{JB}$	Thermal resistance (junction to board)		15.94	$^\circ\text{C/W}$
$\theta_{JC}$	Thermal resistance (junction to case)		5.79	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



### Notes

28. Overshoot:  $V_{IH(AC)} < V_{DDQ} + 0.85\text{ V}$  (Pulse width less than  $t_{CYC}/2$ ). Undershoot:  $V_{IL(AC)} > -1.5\text{ V}$  (Pulse width less than  $t_{CYC}/2$ ).

29. Tested initially and after any design or process change that may affect these parameters.

30. Unless otherwise noted, test conditions are based on signal transition time of 2 V/ns, timing reference levels of 0.75 V,  $V_{REF} = 0.75\text{ V}$ ,  $R_Q = 250\ \Omega$ ,  $V_{DDQ} = 1.5\text{ V}$ , input pulse levels of 0.25 V to 1.25 V, and output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance shown in (a) of Figure 5.

## Switching Characteristics

Over the Operating Range

Parameters [31, 32]		Description	333 MHz		300 MHz		250 MHz		Unit
Cypress Parameter	Consortium Parameter		Min	Max	Min	Max	Min	Max	
t <sub>POWER</sub>		V <sub>DD</sub> (typical) to the first access [33]	1	–	1	–	1	–	ms
t <sub>CYC</sub>	t <sub>KHKH</sub>	K clock and C clock cycle time	3.0	8.4	3.3	8.4	4.0	8.4	ns
t <sub>KH</sub>	t <sub>KHKL</sub>	Input clock (K/ $\bar{K}$ ; C/ $\bar{C}$ ) HIGH	1.20	–	1.32	–	1.6	–	ns
t <sub>KL</sub>	t <sub>KLKH</sub>	Input clock (K/ $\bar{K}$ ; C/ $\bar{C}$ ) LOW	1.20	–	1.32	–	1.6	–	ns
t <sub>KH<math>\bar{K}</math>H</sub>	t <sub>KH<math>\bar{K}</math>H</sub>	K clock rise to $\bar{K}$ clock rise and C to $\bar{C}$ Rise (rising edge to rising edge)	1.35	–	1.49	–	1.8	–	ns
t <sub>KHCH</sub>	t <sub>KHCH</sub>	K/ $\bar{K}$ clock rise to C/ $\bar{C}$ clock rise (rising edge to rising edge)	0	1.30	0	1.45	0	1.8	ns
<b>Setup Times</b>									
t <sub>SA</sub>	t <sub>AVKH</sub>	Address setup to K clock rise	0.4	–	0.4	–	0.5	–	ns
t <sub>SC</sub>	t <sub>IVKH</sub>	Control setup to K clock rise (RPS, WPS)	0.4	–	0.4	–	0.5	–	ns
t <sub>SCDDR</sub>	t <sub>IVKH</sub>	Double data rate control setup to clock (K/ $\bar{K}$ ) rise (BWS <sub>0</sub> , BWS <sub>1</sub> , BWS <sub>2</sub> , BWS <sub>3</sub> )	0.3	–	0.3	–	0.35	–	ns
t <sub>SD</sub>	t <sub>DVKH</sub>	D <sub>[X:0]</sub> setup to clock (K/ $\bar{K}$ ) rise	0.3	–	0.3	–	0.35	–	ns
<b>Hold Times</b>									
t <sub>HA</sub>	t <sub>KHAX</sub>	Address hold after K clock rise	0.4	–	0.4	–	0.5	–	ns
t <sub>HC</sub>	t <sub>KHIX</sub>	Control hold after K clock rise (RPS, WPS)	0.4	–	0.4	–	0.5	–	ns
t <sub>HCDDR</sub>	t <sub>KHIX</sub>	Double data rate control hold after clock (K/ $\bar{K}$ ) rise (BWS <sub>0</sub> , BWS <sub>1</sub> , BWS <sub>2</sub> , BWS <sub>3</sub> )	0.3	–	0.3	–	0.35	–	ns
t <sub>HD</sub>	t <sub>KHDX</sub>	D <sub>[X:0]</sub> hold after clock (K/ $\bar{K}$ ) rise	0.3	–	0.3	–	0.35	–	ns

### Notes

31. Unless otherwise noted, test conditions are based on signal transition time of 2 V/ns, timing reference levels of 0.75 V, V<sub>REF</sub> = 0.75 V, R<sub>Q</sub> = 250  $\Omega$ , V<sub>DDQ</sub> = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and load capacitance shown in (a) of Figure 5 on page 25.

32. When a part with a maximum frequency above 250 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is operated and outputs data with the output timings of that frequency range.

33. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power must be supplied above V<sub>DD(minimum)</sub> initially before a read or write operation is initiated.

## Switching Characteristics (continued)

Over the Operating Range

Parameters <sup>[31, 32]</sup>		Description	333 MHz		300 MHz		250 MHz		Unit
Cypress Parameter	Consortium Parameter		Min	Max	Min	Max	Min	Max	
Output Times									
t <sub>CO</sub>	t <sub>CHQV</sub>	C/ $\overline{C}$ clock rise (or K/ $\overline{K}$ in single clock mode) to data valid	–	0.45	–	0.45	–	0.45	ns
t <sub>DOH</sub>	t <sub>CHQX</sub>	Data output hold after output C/ $\overline{C}$ clock rise (active to active)	–0.45	–	–0.45	–	–0.45	–	ns
t <sub>CCQO</sub>	t <sub>CHCQV</sub>	C/ $\overline{C}$ clock rise to echo clock valid	–	0.45	–	0.45	–	0.45	ns
t <sub>CQOH</sub>	t <sub>CHCQX</sub>	Echo clock hold after C/ $\overline{C}$ clock rise	–0.45	–	–0.45	–	–0.45	–	ns
t <sub>CQD</sub>	t <sub>CQHQV</sub>	Echo clock high to data valid	–	0.25	–	0.27	–	0.30	ns
t <sub>CQDOH</sub>	t <sub>CQHQX</sub>	Echo clock high to data invalid	–0.25	–	–0.27	–	–0.30	–	ns
t <sub>CQH</sub>	t <sub>CQHCQL</sub>	OutPut clock (CQ/ $\overline{CQ}$ ) HIGH <sup>[34]</sup>	1.25	–	1.4	–	1.75	–	ns
t <sub>CQH<math>\overline{CQ}</math></sub>	t <sub>CQH<math>\overline{CQ}</math></sub>	CQ clock rise to $\overline{CQ}$ clock rise (rising edge to rising edge) <sup>[34]</sup>	1.25	–	1.4	–	1.75	–	ns
t <sub>CHZ</sub>	t <sub>CHQZ</sub>	Clock (C/ $\overline{C}$ ) rise to high Z (active to high Z) <sup>[35, 36]</sup>	–	0.45	–	0.45	–	0.45	ns
t <sub>CLZ</sub>	t <sub>CHQX1</sub>	Clock (C/ $\overline{C}$ ) rise to low Z <sup>[35, 36]</sup>	–0.45	–	–0.45	–	–0.45	–	ns
PLL Timing									
t <sub>KC Var</sub>	t <sub>KC Var</sub>	Clock phase jitter	–	0.20	–	0.20	–	0.20	ns
t <sub>KC lock</sub>	t <sub>KC lock</sub>	PLL lock time (K, C) <sup>[37]</sup>	20	–	20	–	20	–	μs
t <sub>KC Reset</sub>	t <sub>KC Reset</sub>	K static to PLL reset	30	–	30	–	30	–	ns

### Notes

34. These parameters are extrapolated from the input timing parameters ( $t_{CYC}/2 - 250$  ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.

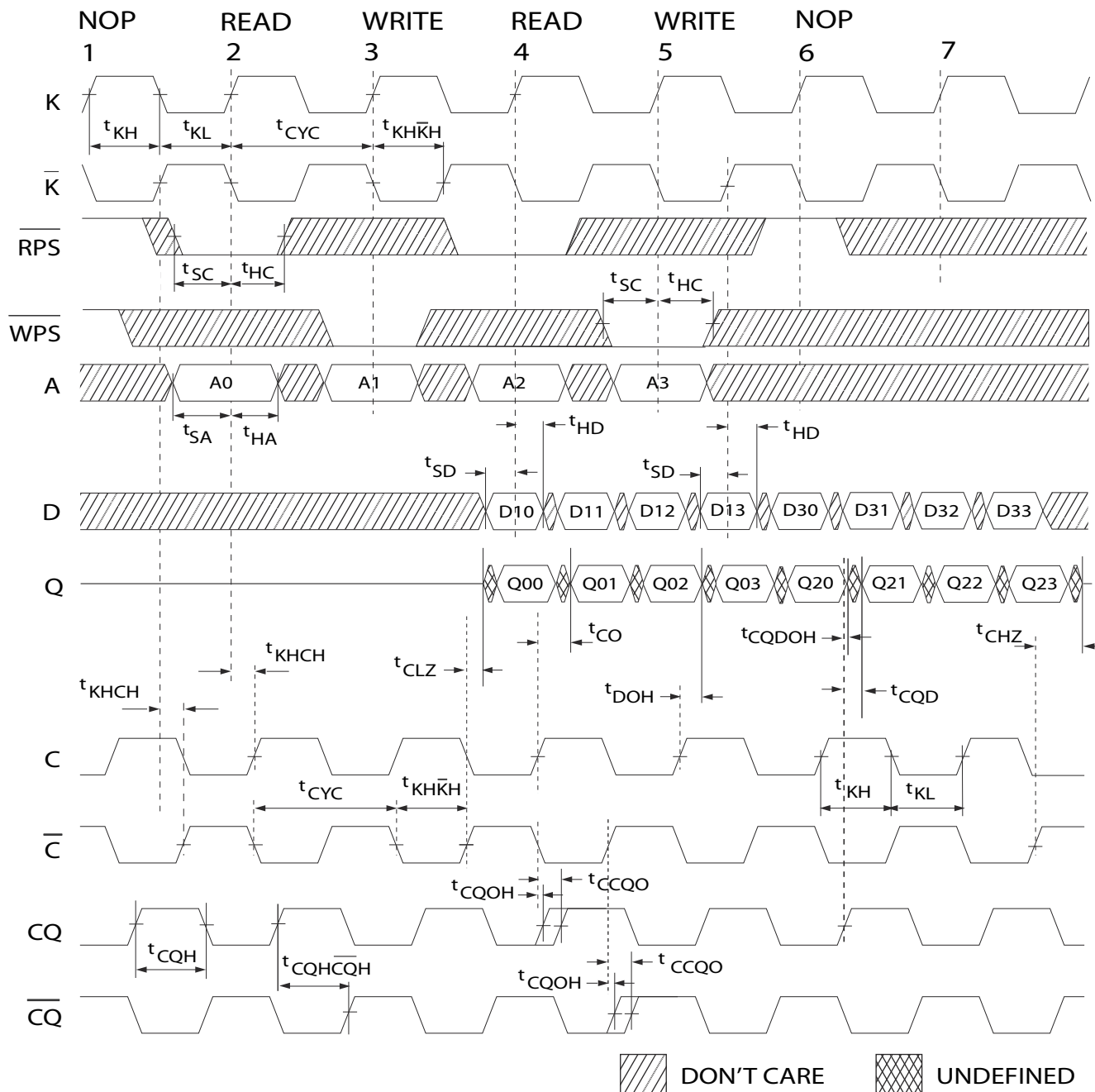
35.  $t_{CHZ}$ ,  $t_{CLZ}$ , are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 25. Transition is measured  $\pm 100$  mV from steady-state voltage.

36. At any voltage and temperature  $t_{CHZ}$  is less than  $t_{CLZ}$  and  $t_{CHZ}$  less than  $t_{CO}$ .

37. For frequencies 300 MHz or below, the Cypress QDR II devices surpass the QDR consortium specification for PLL lock time ( $t_{KC\ lock}$ ) of 20 μs (min. spec.) and will lock after 1024 clock cycles (min. spec.), after a stable clock is presented, per the previous 90 nm version.

## Switching Waveforms

Figure 6. Read/Write/Deselect Sequence [38, 39, 40]



### Notes

38. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.

39. Outputs are disabled (High Z) one clock cycle after a NOP.

40. In this example, if address A2 = A1, then data Q20 = D10, Q21 = D11, Q22 = D12, and Q23 = D13. Write data is forwarded immediately as read results. This note applies to the whole diagram.

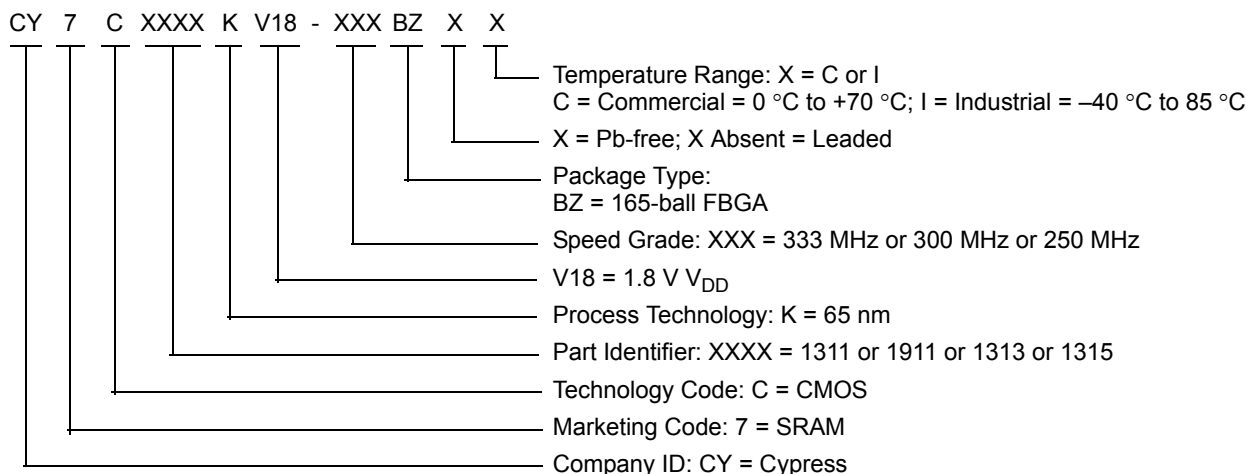
## Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

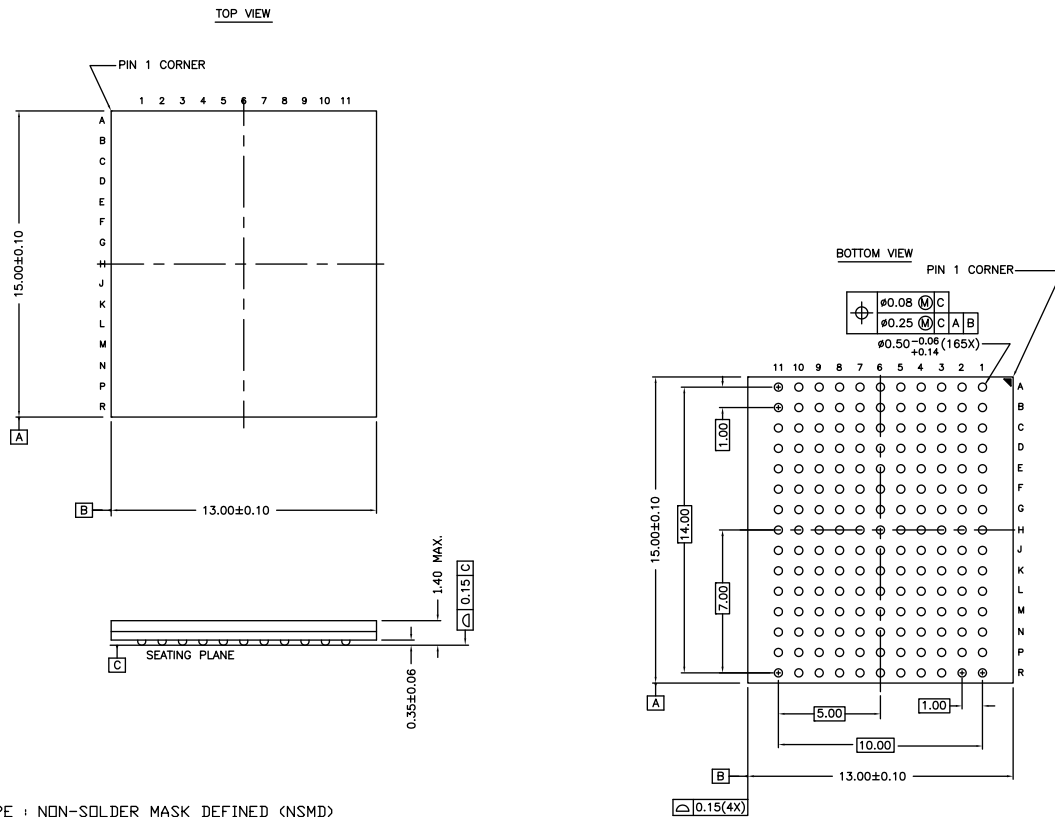
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
333	CY7C1911KV18-333BZC	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	Commercial
	CY7C1315KV18-333BZC			
	CY7C1315KV18-333BZXC		165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
300	CY7C1911KV18-300BZC	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	Commercial
	CY7C1911KV18-300BZXC		165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
250	CY7C1311KV18-250BZC	51-85180	165-ball FBGA (13 × 15 × 1.4 mm)	Commercial
	CY7C1911KV18-250BZC			
	CY7C1313KV18-250BZC			
	CY7C1315KV18-250BZC			
	CY7C1313KV18-250BZXC		165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
	CY7C1315KV18-250BZXC			
	CY7C1315KV18-250BZI		165-ball FBGA (13 × 15 × 1.4 mm)	Industrial
	CY7C1313KV18-250BZXI		165-ball FBGA (13 × 15 × 1.4 mm) Pb-free	
	CY7C1315KV18-250BZXI			

## Ordering Code Definitions



## Package Diagram

Figure 7. 165-ball FBGA (13 × 15 × 1.4 mm) BB165D/BW165D (0.5 Ball Diameter) Package Outline, 51-85180



NOTES :

SOLDER PAD TYPE : NON-SOLDER MASK DEFINED (NSMD)

JEDEC REFERENCE : MO-216 / ISSUE E

PACKAGE CODE : BB0AC/BW0AC

PACKAGE WEIGHT : SEE CYPRESS PACKAGE MATERIAL DECLARATION

DATASHEET (PMDD) POSTED ON THE CYPRESS WEB.

51-85180 \*G



## Acronyms

Acronym	Description
DDR	Double Data Rate
FBGA	Fine-Pitch Ball Grid Array
HSTL	High-Speed Transceiver Logic
I/O	Input/Output
JTAG	Joint Test Action Group
LMBU	Logical Multiple Bit Upset
LSB	Least Significant Bit
LSBU	Logical Single Bit Upset
MSB	Most Significant Bit
PLL	Phase Locked Loop
QDR	Quad Data Rate
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TAP	Test Access Port
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data-In
TDO	Test Data-Out

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1311KV18/CY7C1911KV18/CY7C1313KV18/CY7C1315KV18, 18-Mbit QDR® II SRAM Four-Word Burst Architecture Document Number: 001-58904				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of change
**	2860800	VKN	01/20/2010	New data sheet.
*A	2897083	AJU	03/22/10	Updated <a href="#">Ordering Information</a> (Removed inactive parts).
*B	3076901	NJY	11/03/2010	Changed status from Preliminary to Final. Updated <a href="#">Ordering Information</a> (Updated part numbers) and added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .
*C	3167511	NJY	02/09/2011	Updated <a href="#">Switching Characteristics</a> (Added Note 37 and referred the same note in the description of $t_{KC\ lock}$ parameter). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*D	3549641	NJY	03/22/2012	Updated <a href="#">Selection Guide</a> (Removed 167 MHz and 200 MHz frequency related information, also updated the value of Maximum operating current for $\times 8$ as "Not Offered" for 300 MHz and 330 MHz frequencies). Updated <a href="#">Electrical Characteristics</a> (Updated <a href="#">DC Electrical Characteristics</a> (Removed 167 MHz and 200 MHz frequency related information), also removed the values of $I_{DD}$ and $I_{SB1}$ parameters for $\times 8$ for 300 MHz and 330 MHz frequencies). Updated <a href="#">Switching Characteristics</a> (Removed 167 MHz and 200 MHz frequency related information). Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagram</a> .
*E	3819971	PRIT	11/23/2012	Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated <a href="#">Package Diagram</a> (spec 51-85180 (Changed revision from *E to *F)).
*F	3860026	NJY	01/10/2013	Updated <a href="#">Ordering Information</a> (Updated part numbers).
*G	4374845	PRIT	05/09/2014	Updated <a href="#">Application Example</a> : Updated <a href="#">Figure 2</a> . Updated <a href="#">Thermal Resistance</a> : Updated values of $\theta_{JA}$ parameter. Included $\theta_{JB}$ parameter and its details. Updated to new template.
*H	4578255	PRIT	11/25/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated <a href="#">Ordering Information</a> : Removed pruned parts mentioned below: CY7C1313KV18-333BZC, CY7C1315KV18-300BZXC, CY7C1911KV18-250BZXC and CY7C1313KV18-250BZI.
*I	4785448	PRIT	06/03/2015	Updated <a href="#">Ordering Information</a> (Updated part numbers). Updated to new template.
*J	5097221	PRIT	01/21/2016	Updated <a href="#">Package Diagram</a> : spec 51-85180 – Changed revision from *F to *G. Completing Sunset Review.
*K	5980484	AESATMP8	12/01/2017	Updated logo and Copyright.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

### Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2010-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.