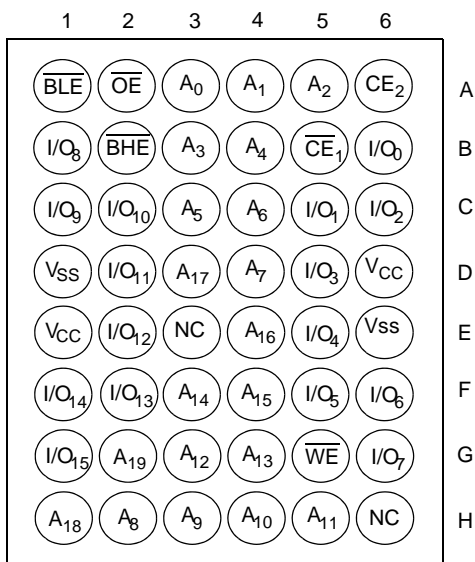


## Contents

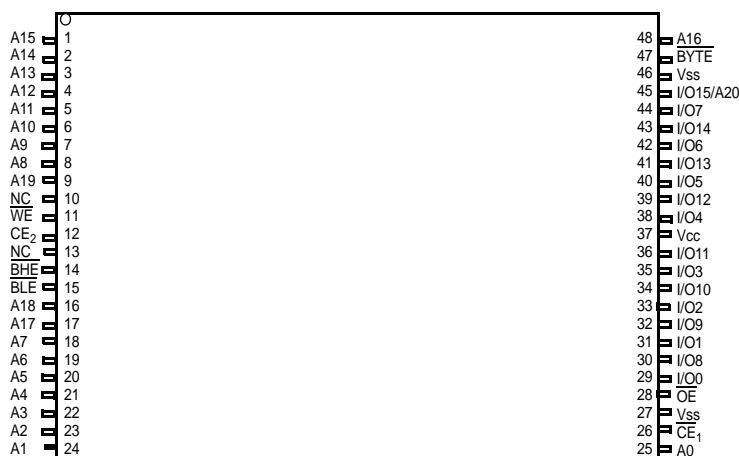
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## Pin Configuration

**Figure 1. 48-ball VFBGA pinout (Top View)** <sup>[1, 2]</sup>



**Figure 2. 48-pin TSOP I pinout (Top View)** <sup>[2, 3]</sup>



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[4]</sup>	Max		Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max
CY62167EV30LL	Industrial/Automotive-A	2.2	3.0	3.6	45	2.2	4.0	25	30	1.5	12

### Notes

- Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
- NC pins are not connected on the die.
- The BYTE pin in the 48-pin TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 1 M x 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M x 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2 M x 8 configuration, Pin 45 is A20, while BHE, BLE and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature  
with power applied ..... -55 °C to + 125 °C

Supply voltage  
to ground potential [5, 6] .... -0.3 V to 3.9 V ( $V_{CC(max)}$  + 0.3 V)

DC voltage applied to outputs  
in High Z state [5, 6] ..... -0.3 V to 3.9 V ( $V_{CC(max)}$  + 0.3 V)

DC input voltage [5, 6] ..... -0.3 V to 3.9 V ( $V_{CC(max)}$  + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ [7]
CY62167EV30LL	Industrial/ Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial/ Automotive-A)			Unit
			Min	Typ [8]	Max	
$V_{OH}$	Output HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1$ mA		2.0	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0$ mA		2.4	V
$V_{OL}$	Output LOW voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1$ mA		—	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1$ mA		0.4	V
$V_{IH}$	Input HIGH voltage	$2.2 \leq V_{CC} \leq 2.7$	1.8	—	$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$	2.2	—	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW voltage	$2.2 \leq V_{CC} \leq 2.7$	-0.3	—	0.6	V
		$2.7 \leq V_{CC} \leq 3.6$ For VFBGA package	-0.3	—	0.8	V
		$2.7 \leq V_{CC} \leq 3.6$ For TSOP I package	-0.3	—	0.7 [9]	V
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	—	+1	μA
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , Output disabled	-1	—	+1	μA
$I_{CC}$	$V_{CC}$ operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$		—	mA
		$f = 1$ MHz	$I_{OUT} = 0$ mA CMOS levels		2.2	mA
$I_{SB1}$ [10]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{max}$ (address and data only), $f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), $V_{CC} = V_{CC(max)}$	—	1.5	12	μA
$I_{SB2}$ [10]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or	$V_{CC} = V_{CC(max)}$ Temperature = 25 °C		3.0 [11]	μA
		$(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$	$V_{CC} = 3.0$ V, Temperature = 40 °C		3.5 [11]	μA
			$V_{CC} = V_{CC(max)}$ Temperature = 85 °C		12	μA

### Notes

- $V_{IL(min)}$  = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75$  V for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
- Under DC conditions the device meets a  $V_{IL}$  of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V. This is applicable to TSOP I package only.
- Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) and  $\overline{BYTE}$  must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating
- This parameter is guaranteed by design.

## Capacitance

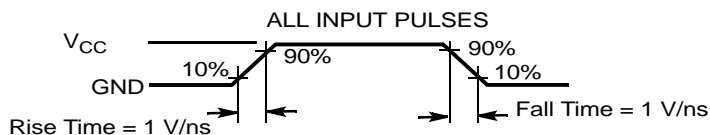
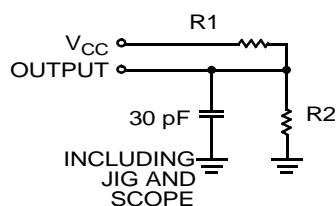
Parameter <sup>[12]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

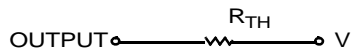
Parameter <sup>[12]</sup>	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	60	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		16	4.3	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.2 V to 2.7 V	2.7 V to 3.6 V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Note

12. Tested initially and after any design or process changes that may affect these parameters.

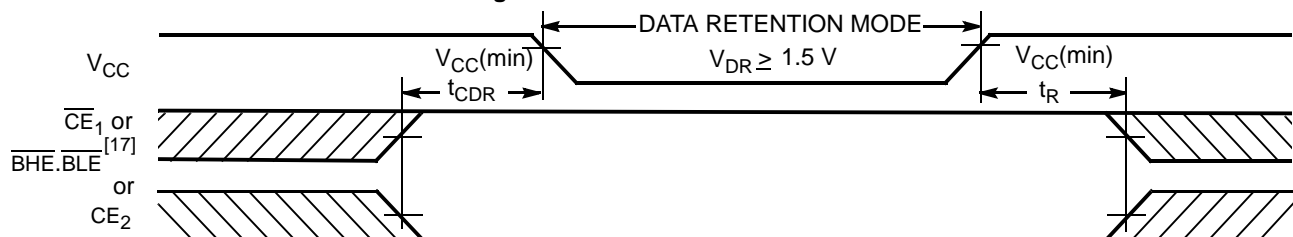
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions			Min	Typ <sup>[13]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention				1.5	–	–	V
$I_{CCDR}^{[14]}$	Data retention current	$V_{CC} = 1.5 \text{ V to } 3.0 \text{ V},$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}$	Industrial	48-pin TSOP I	–	–	8	$\mu\text{A}$
		$V_{CC} = 1.5 \text{ V},$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}$	Industrial	Other packages	–	–	10	$\mu\text{A}$
		$V_{CC} = 1.5 \text{ V},$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V or } CE_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V},$ $V_{IN} \geq V_{CC} - 0.2 \text{ V or } V_{IN} \leq 0.2 \text{ V}$	Automotive-A	All packages	–	–	10	$\mu\text{A}$
$t_{CDR}^{[15]}$	Chip deselect to data retention time				0	–	–	–
$t_R^{[16]}$	Operation recovery time				45	–	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^\circ\text{C}$ .
14. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ), byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) and  $\overline{BYTE}$  must be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(min)} \geq 100 \mu\text{s}$ .
17.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

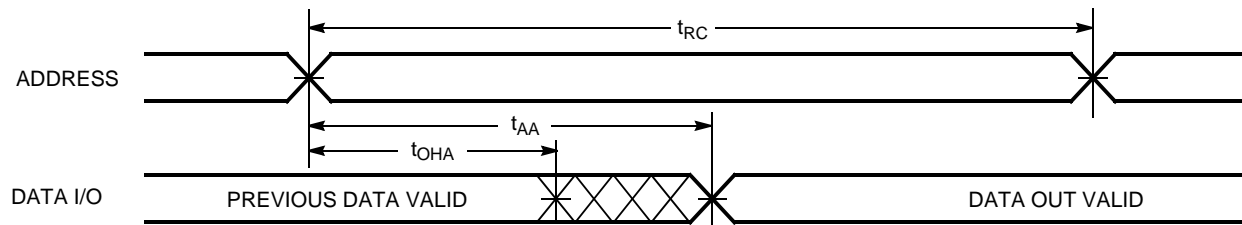
Parameter <sup>[18, 19]</sup>	Description	45 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[20]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[20, 21]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[20]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High Z <sup>[20, 21]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down	–	45	ns
t <sub>DBE</sub>	BLE / BHE LOW to data valid	–	45	ns
t <sub>LZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z <sup>[20]</sup>	10	–	ns
t <sub>HZBE</sub>	BLE / BHE HIGH to High Z <sup>[20, 21]</sup>	–	18	ns
Write Cycle <sup>[22, 23]</sup>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>BW</sub>	BLE / BHE LOW to write end	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[20, 21]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[20]</sup>	10	–	ns

### Notes

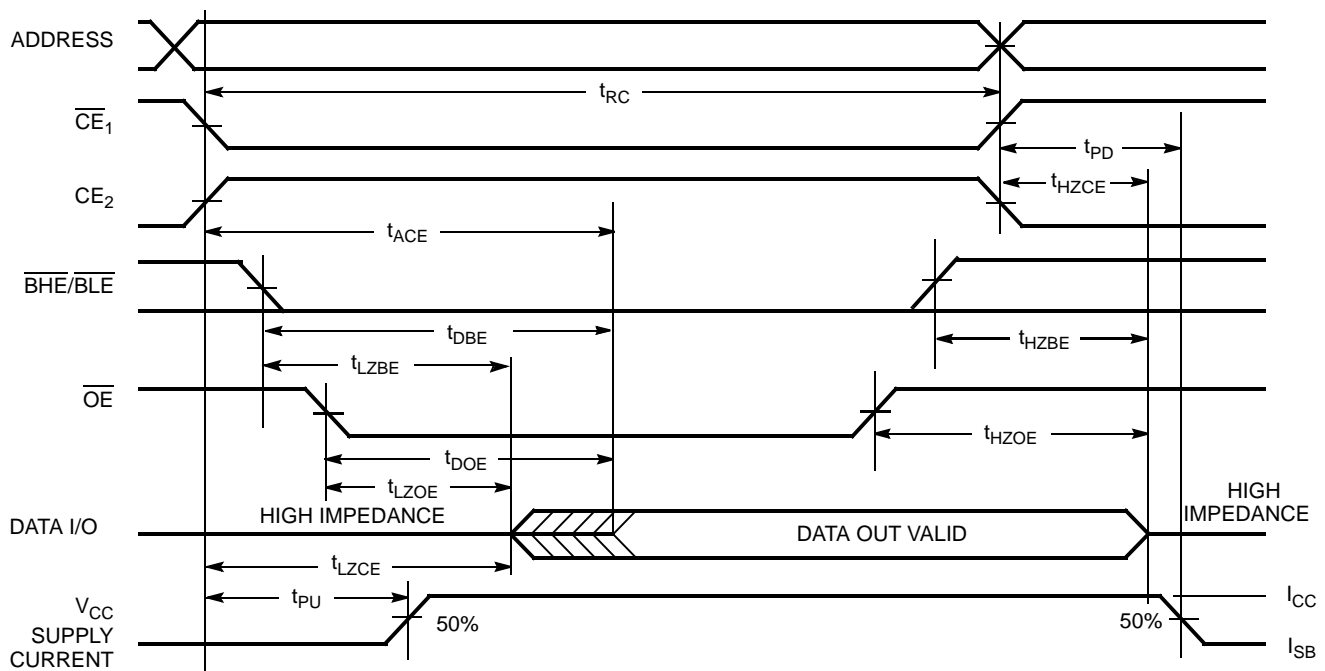
18. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in Figure 3 on page 5.
19. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
20. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
21.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
22. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , BHE or BLE or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
23. The minimum pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1 (Address Transition Controlled)** [24, 25]



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [25, 26]

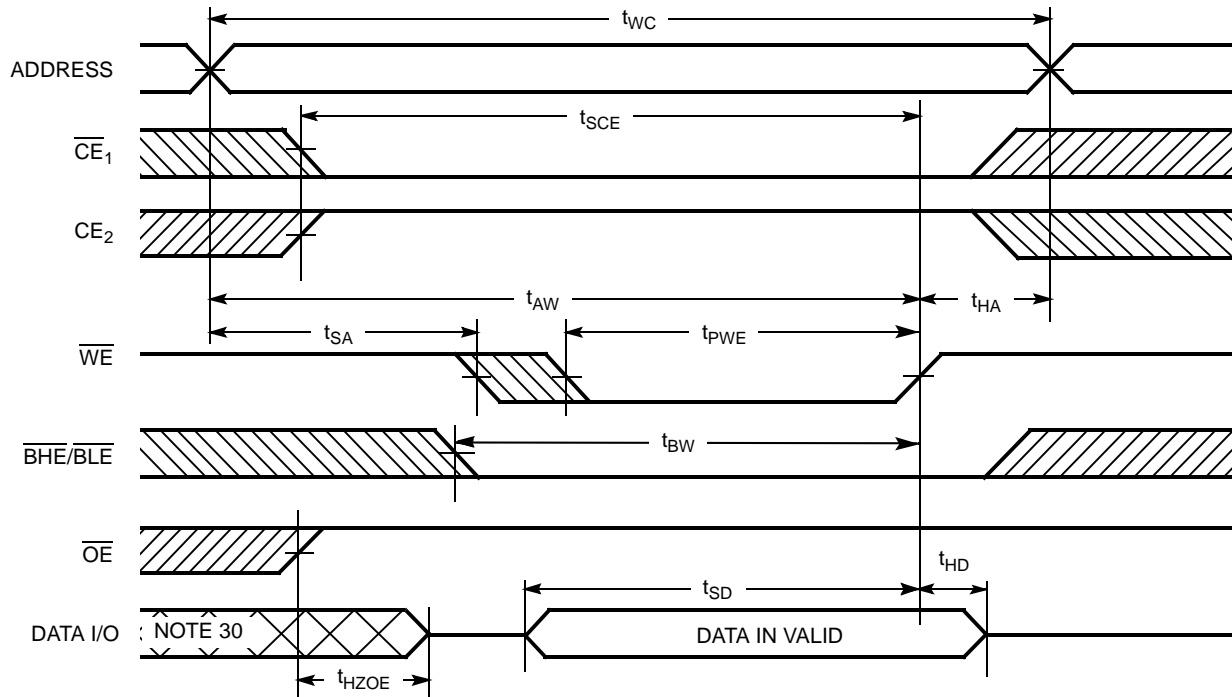


### Notes

24. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .

25.  $\overline{WE}$  is HIGH for read cycle.

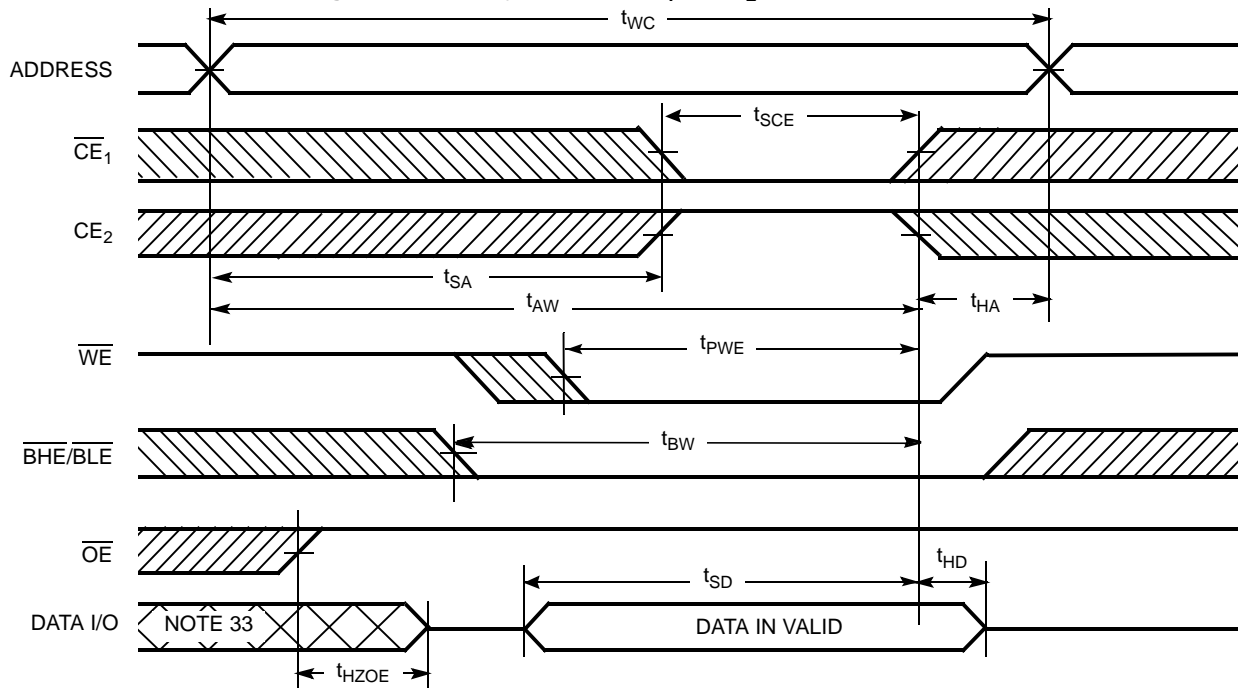
26. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [27, 28, 29]**

**Notes**

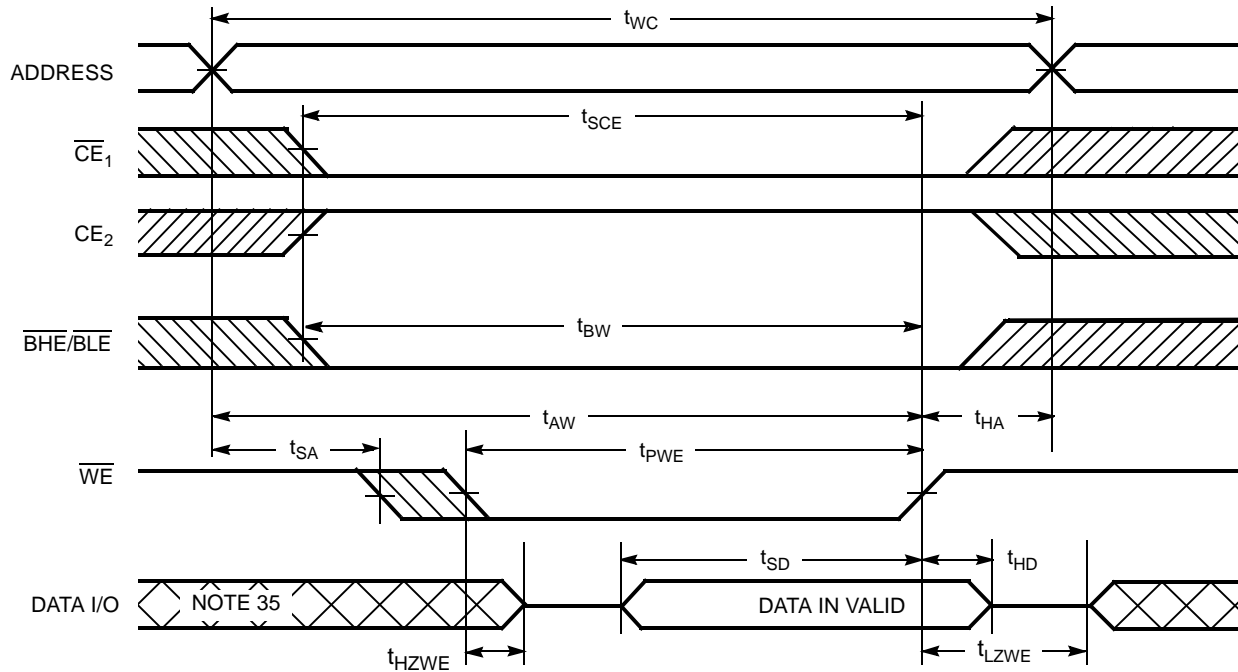
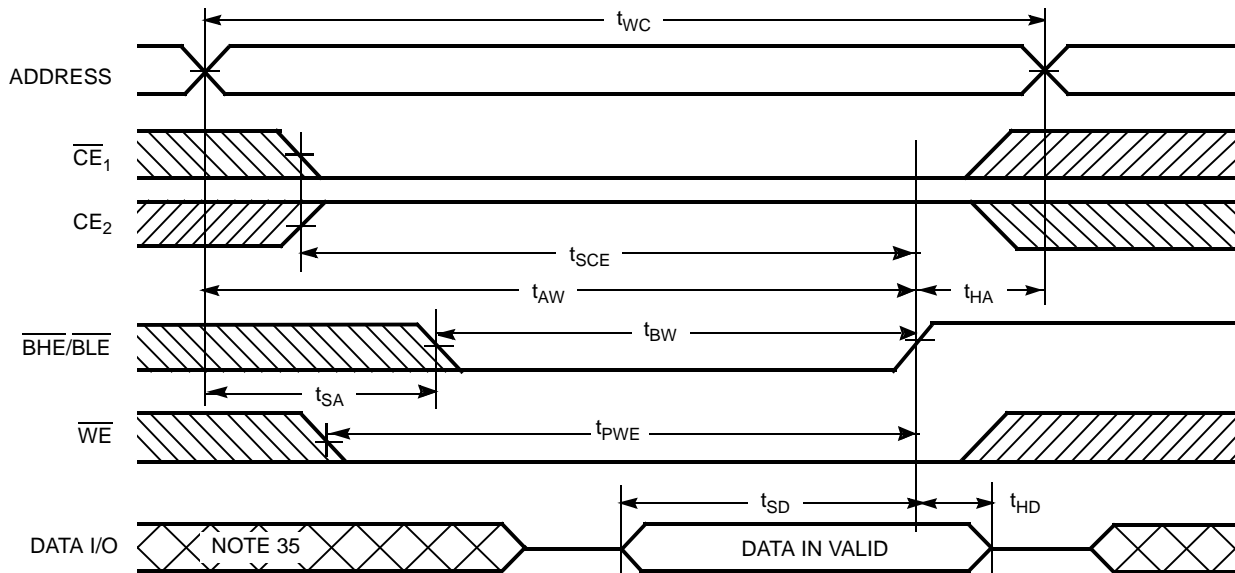
27. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
28. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
29. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.
30. During this period the I/Os are in output state. Do not apply input signals.



**Switching Waveforms** (continued)

**Figure 8. Write Cycle No. 2 ( $\overline{CE_1}$  or  $CE_2$  Controlled)** [31, 32]

**Notes**

31. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE_1} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. If  $\overline{CE_1}$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
33. During this period the I/Os are in output state. Do not apply input signals.

**Switching Waveforms (continued)**
**Figure 9. Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) [34]**

**Figure 10. Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  controlled,  $\overline{OE}$  LOW) [34]**

**Notes**

34. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.  
 35. During this period the I/Os are in output state. Do not apply input signals.

## Truth Table

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	$X^{[36]}$	X	X	$X^{[36]}$	$X^{[36]}$	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
$X^{[36]}$	L	X	X	$X^{[36]}$	$X^{[36]}$	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
$X^{[36]}$	$X^{[36]}$	X	X	H	H	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )

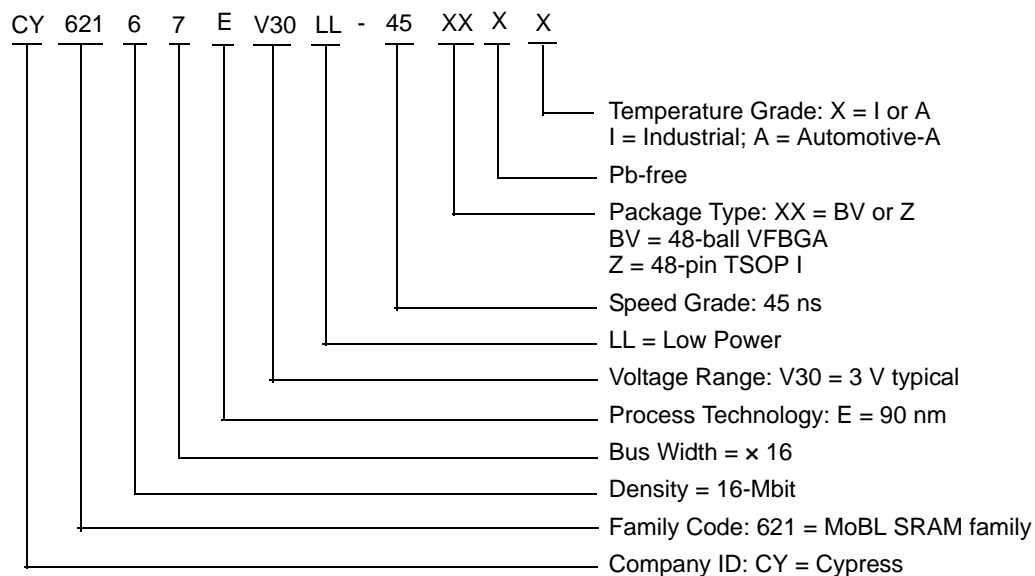
### Note

36. The 'X' (Don't care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

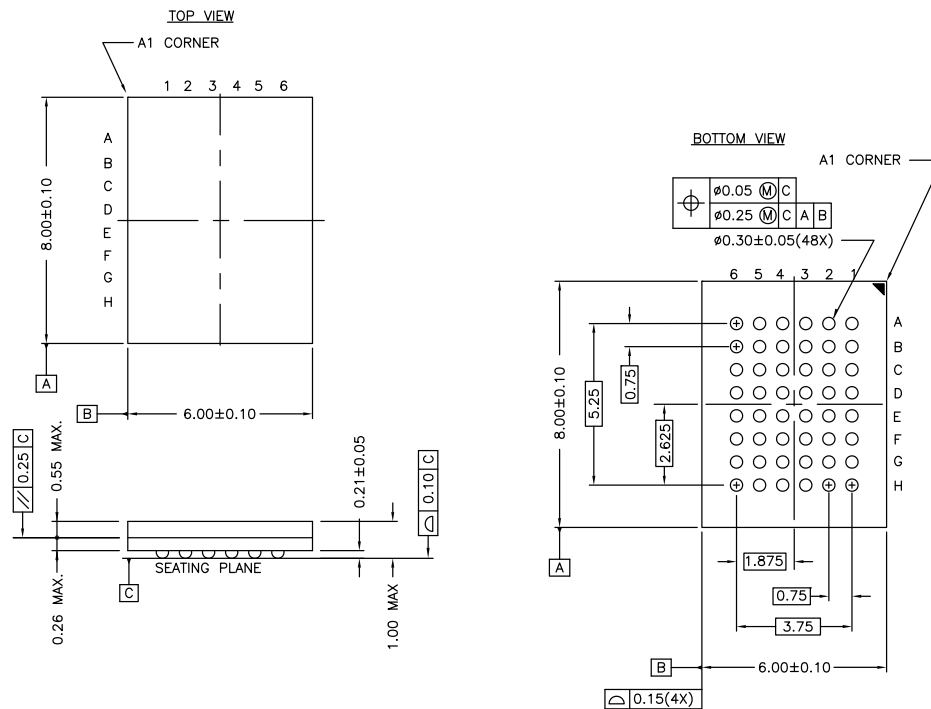
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BVI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Package Code: BV48	Industrial
	CY62167EV30LL-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
	CY62167EV30LL-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Automotive-A
	CY62167EV30LL-45ZXA	51-85183	48-pin TSOP I (Pb-free)	

## Ordering Code Definitions



## Package Diagrams

**Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150**

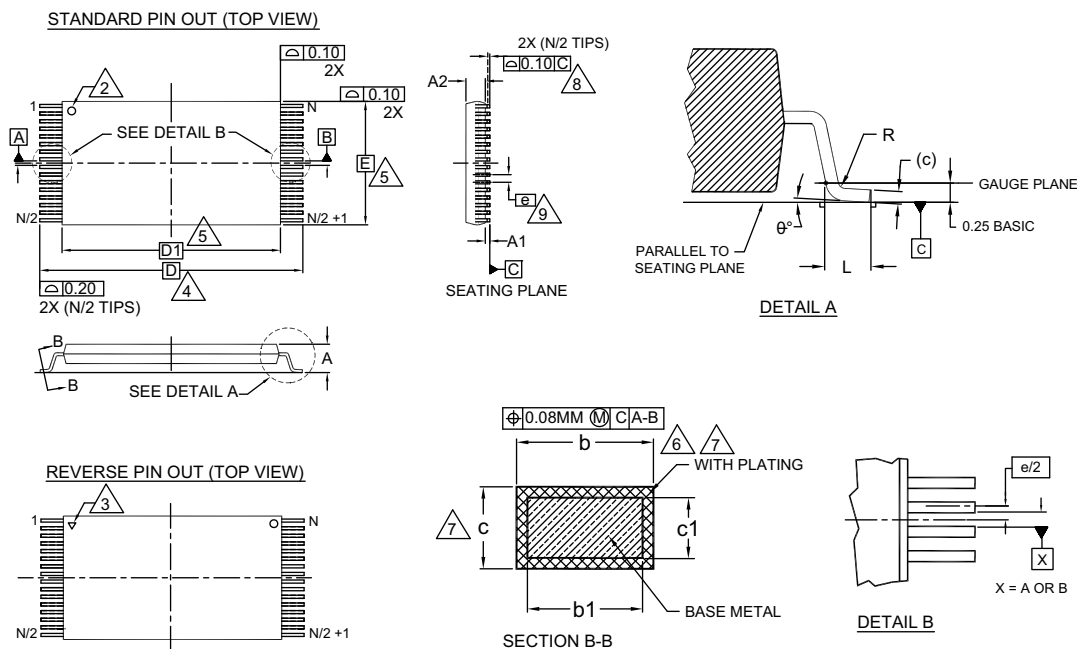


NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

## Package Diagrams (continued)

**Figure 12. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183**



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE  $-C-$ . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F

## Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62167EV30 MoBL®, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 38-05446				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	202600	AJU	01/23/2004	New data sheet.
*A	463674	NXR	See ECN	Changed status from Advance Information to Preliminary Removed 'L' bin and 35 ns speed bin from product offering Modified Data sheet to include x8 configurability. Changed ball E3 in FBGA pinout from DNU to NC Changed the $I_{SB2(Typ)}$ value from 1.3 $\mu A$ to 1.5 $\mu A$ Changed the $I_{CC(Max)}$ value from 40 mA to 25 mA Changed Vcc stabilization time in footnote #9 from 100 $\mu s$ to 200 $\mu s$ Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics ( $t_R$ ) from 100 $\mu s$ to $t_{RC}$ ns Changed $t_{OHA}$ , $t_{LZCE}$ , $t_{LZBE}$ , and $t_{LZWE}$ from 6 ns to 10 ns Changed $t_{LZOE}$ from 3 ns to 5 ns. Changed $t_{HZOE}$ , $t_{HZCE}$ , $t_{HZBE}$ , and $t_{HZWE}$ from 15 ns to 18 ns Changed $t_{SCE}$ , $t_{AW}$ , and $t_{BW}$ from 40 ns to 35 ns Changed $t_{PE}$ from 30 ns to 35 ns Changed $t_{SD}$ from 20 ns to 25 ns Updated 48-ball FBGA Package Information. Updated the Ordering Information table
*B	469169	NSI	See ECN	Minor Change: Moved to external web
*C	1130323	VKN	See ECN	Changed status from Preliminary to Final. Changed $I_{CC}$ max spec from 2.8 mA to 4.0 mA for $f = 1\text{MHz}$ Changed $I_{CC}$ typ spec from 22 mA to 25 mA for $f = f_{max}$ Changed $I_{CC}$ max spec from 25 mA to 30 mA for $f = f_{max}$ Added $V_{IL}$ spec for TSOP I package and footnote# 9 Added footnote# 10 related to $I_{SB2}$ and $I_{CCDR}$ Changed $I_{SB1}$ and $I_{SB2}$ spec from 8.5 $\mu A$ to 12 $\mu A$ Changed $I_{CCDR}$ spec from 8 $\mu A$ to 10 $\mu A$ Added footnote# 15 related to AC timing parameters
*D	1323984	VKN / AESA	See ECN	Modified $I_{CCDR}$ spec for TSOP I package Added 48-ball VFBGA (6 × 7 × 1mm) package Added footnote# 1 related to VFBGA (6 × 7 × 1mm) package Updated Ordering Information table
*E	2678799	VKN / PYRS	03/25/2009	Added Automotive-A information
*F	2720234	VKN / AESA	06/17/2009	Included -45BVXA part in the Ordering information table
*G	2880574	VKN	02/18/2010	Modified $I_{CCDR}$ spec from 8 $\mu A$ to 10 $\mu A$ for Auto-A grade. Added <a href="#">Contents</a> . Updated all package diagrams. Updated links in <a href="#">Sales</a> , <a href="#">Solutions</a> , and <a href="#">Legal Information</a> .
*H	2934396	VKN	06/03/10	Added footnote #25 related to chip enable. Updated template.
*I	3006301	RAME	08/12/2010	Included BHE and BLE in $I_{SB1}$ , $I_{SB2}$ , and $I_{CCDR}$ test conditions to reflect Byte power down feature. Removed 48-ball VFBGA (6 × 7 × 1 mm) package related information. Added Acronyms and Ordering code definition. Format updates to match template.



**Document History Page** (continued)

Document Title: CY62167EV30 MoBL®, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 38-05446				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*J	3295175	RAME	06/29/2011	Updated <a href="#">Package Diagrams</a> . Added <a href="#">Document Conventions</a> . Removed reference to AN1064 SRAM system guidelines. Added I <sub>SB1</sub> to footnotes <a href="#">10</a> and <a href="#">14</a> . Added byte enables to footnote <a href="#">36</a> and referenced to Truth table.
*K	3411301	TAVA	10/17/2011	Updated <a href="#">Switching Waveforms</a> . Updated <a href="#">Package Diagrams</a> . Updated to new template.
*L	3667939	TAVA	07/09/2012	Updated <a href="#">Ordering Information</a> (No change in part numbers, updated details in Package Type column only). Updated <a href="#">Package Diagrams</a> (Spec 51-85150 (Updated figure caption only, no change in revision)).
*M	4102969	VINI	08/23/2013	Updated <a href="#">Switching Characteristics</a> : Updated Note 19. Updated <a href="#">Package Diagrams</a> : spec 51-85150 – Changed revision from *G to *H. Updated to new template. Completing Sunset Review.
*N	4574264	VINI	11/19/2014	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, <a href="#">click here</a> .” at the end. Updated <a href="#">Maximum Ratings</a> : Referred Notes 5 and 6 in “Supply voltage to ground potential”. Updated <a href="#">Switching Characteristics</a> : Added Note 23 and referred the same note in “Write Cycle”.
*O	4715413	VINI	04/07/2015	Updated <a href="#">Electrical Characteristics</a> : Updated details in “Test Conditions” column corresponding to I <sub>SB2</sub> parameter and added corresponding values. Added Note 11 and referred the same note in maximum values of I <sub>SB2</sub> parameter corresponding to Test Conditions “V <sub>CC</sub> = V <sub>CC(max)</sub> , Temperature = 25 °C” and “V <sub>CC</sub> = 3.0 V, Temperature = 40 °C”.
*P	5734005	VINI	05/11/2017	Updated <a href="#">Package Diagrams</a> : spec 51-85183 – Changed revision from *D to *F. Updated to new template.

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