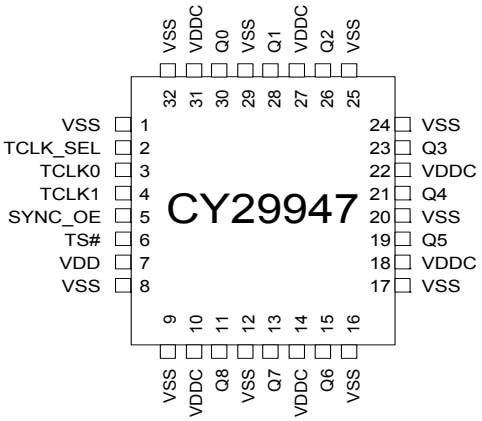
Contents

Pinouts

Figure 1. 32-pin TQFP pinout



Pin Definitions

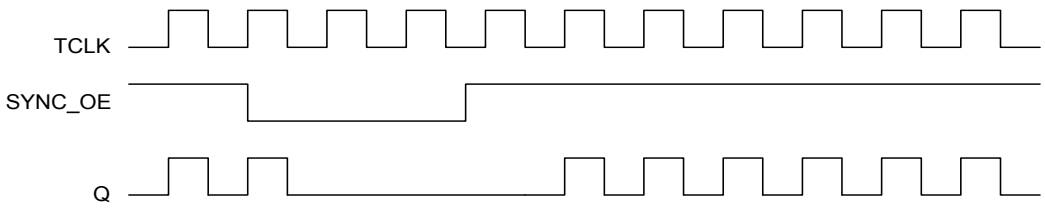
Pin	Name	PWR	I/O [1]	Description
3	TCLK0		I, PU	**Test Clock Input**
4	TCLK1		I, PU	**Test Clock Input**
2	TCLK_SEL		I, PU	**Test Clock Select Input**. When LOW, TCLK0 is selected. When asserted HIGH, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	**Clock Outputs**
5	SYNC_OE		I, PU	**Output Enable Input**. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	**Three-state Control Input**. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			**3.3 V or 2.5 V Power Supply for Output Clock Buffers**
7	VDD			**3.3 V or 2.5 V Power Supply**
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			**Common Ground**

Note
1. PD = internal pull-down, PU = internal pull-up.

Output Enable/Disable

The CY29947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in Figure 2.

Figure 2. SYNC_OE Timing Diagram



Maximum Ratings

Exceeding maximum ratings [2] may shorten the useful life of the device. User guidelines are not tested.

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3 V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3 V

Storage Temperature: ..... –65 °C to + 150 °C

Operating Temperature: ..... –40 °C to +85 °C

Maximum ESD protection ..... 2 kV

Maximum Power Supply: ..... 5.5 V

Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters

$V_{DD} = V_{DDC}$ = 3.3 V ± 10% or 2.5 V ± 5%, Over the specified temperature range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		V_{SS}	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}	V
I_{IL}	Input Low Current[3]		–	–	–100	µA
I_{IH}	Input High Current[3]		–	–	10	µA
V_{OL}	Output Low Voltage[4]	I_{OL} = 20 mA	–	–	0.4	V
V_{OH}	Output High Voltage[4]	I_{OH} = –20 mA, V_{DD} = 3.3 V	2.5	–	–	V
		I_{OH} = –20 mA, V_{DD} = 2.5 V	1.8	–	–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3 V, Outputs @ 100 MHz, CL = 30 pF	–	120	–	mA
		V_{DD} = 3.3 V, Outputs @ 160 MHz, CL = 30 pF	–	200	–	
		V_{DD} = 2.5 V, Outputs @ 100 MHz, CL = 30 pF	–	85	–	
		V_{DD} = 2.5 V, Outputs @ 160 MHz, CL = 30 pF	–	140	–	
Zout	Output Impedance	V_{DD} = 3.3 V	12	15	18	Ω
		V_{DD} = 2.5 V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

Notes

2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
5. These parameters are guaranteed by design and are not tested.

AC Parameters

V_{DD} = V_{DDC} = 3.3 V ± 10% or 2.5 V ± 5%, Over the specified temperature range

Parameter [6]	Description	Conditions	Min	Typ	Max	Unit
Fmax	Input Frequency[7]	V_{DD} = 3.3 V	–	–	200	MHz
		V_{DD} = 2.5 V	–	–	170	
Tpd	TCLK To Q Delay[7]	V_{DD} = 3.3 V	4.75	–	9.25	ns
		V_{DD} = 2.5 V	6.50	–	10.50	
FoutDC	Output Duty Cycle[7, 8]	Measured at V_{DD}/2	45	–	55	%
tpZL, tpZH	Output Enable Time (all outputs)		2	–	10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2	–	10	ns
Tskew	Output-to-Output Skew[7, 9]		–	150	250	ps
Tskew(pp)	Part-to-Part Skew[10]		–	–	2.0	ns
Ts	Set-up Time[7, 11]	SYNC_OE to TCLK	0.0	–	–	ps
Th	Hold Time[7, 11]	TCLK to SYNC_OE	1.0	–	–	ps
Tr/Tf	Output Clocks Rise/Fall Time[9]	0.8 V to 2.0 V, V_{DD} = 3.3 V	0.20	–	1.0	ns
		0.6 V to 1.8 V, V_{DD} = 2.5 V	0.20	–	1.3	

Notes
6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50 Ω transmission lines.
8. 50% input duty cycle.
9. See Figure 3 on page 7.
10. Part-to-Part skew at a given temperature and voltage.
11. Set-up and hold times are relative to the falling edge of the input clock.

Figure 3. LVCMOS_CLK CY29947 Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

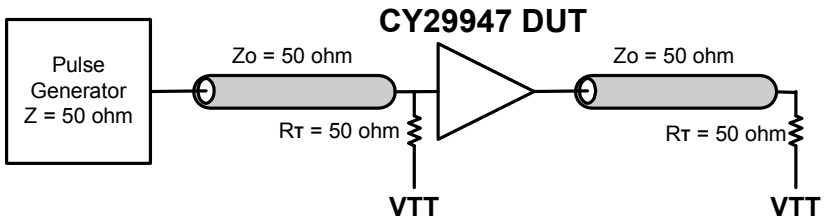


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

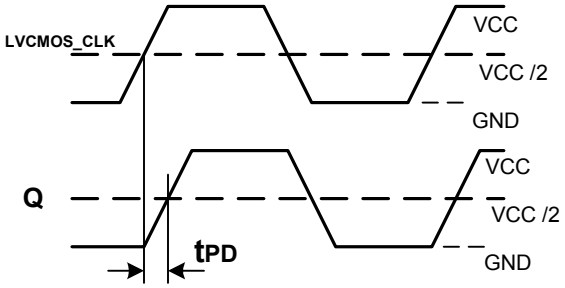


Figure 5. Output Duty Cycle (FoutDC)

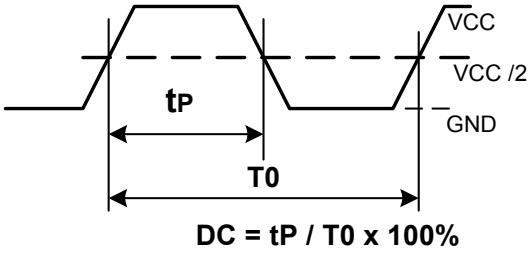
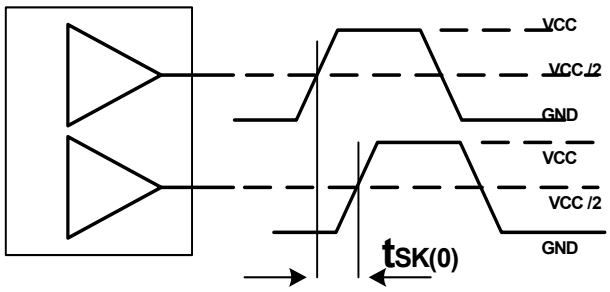


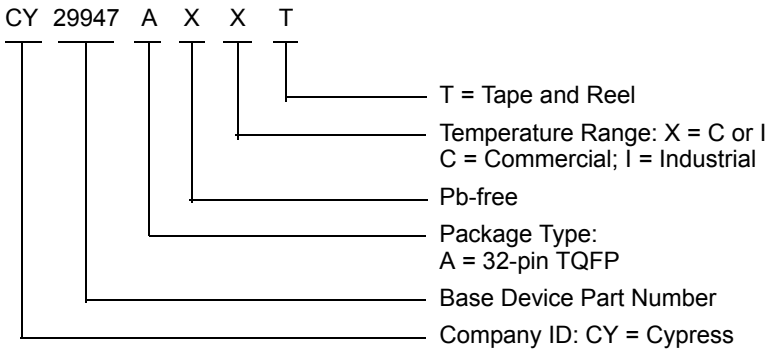
Figure 6. Output-to-Output Skew tsk(0)



Ordering Information

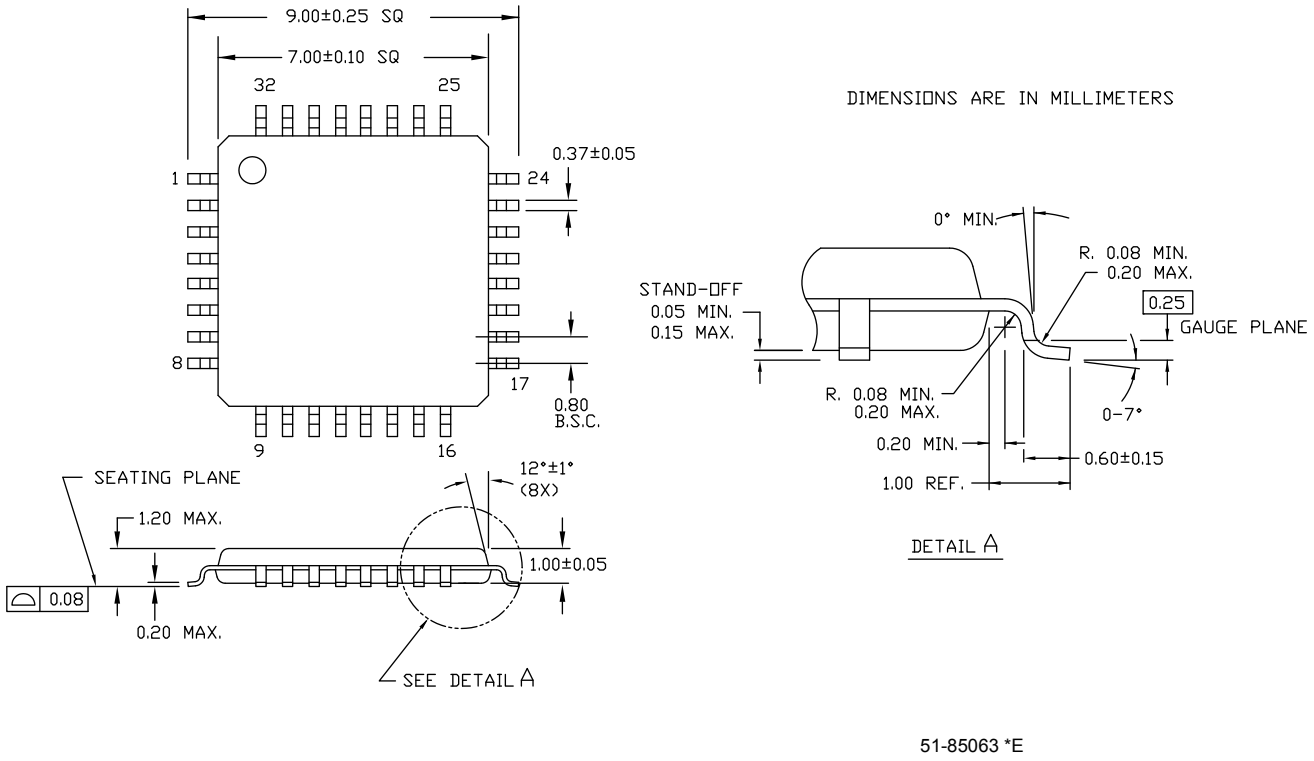
Part Number	Package Type	Production Flow
CY29947AXI	32-pin TQFP	Industrial, –40 °C to +85 °C
CY29947AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to +85 °C

Ordering Code Definitions



Package Drawing and Dimension

Figure 7. 32-pin TQFP (7 × 7 × 1.0 mm) Package Outline, 51-85063



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
I/O	Input/Output
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase Locked Loop
TQFP	Thin Quad Flat Pack
VCO	Voltage-Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kV	kilovolt
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Revision History

Document Title: CY29947, 2.5 V or 3.3 V, 200 MHz, 1:9 Clock Distribution Buffer Document Number: 38-07287				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111098	02/07/02	BRK	New data sheet
*A	116781	08/14/02	HWT	Added Commercial Temperature Range in the ordering information
*B	118462	09/09/02	HWT	Corrected the Package Drawing and Dimension in page 6 from 32 LQFP to 32 TQFP
*C	122879	12/22/02	RBI	Added power up requirements to Maximum Ratings
*D	2899714	03/26/10	BASH	Removed inactive parts from the ordering table. Replaced with active parts. Updated package diagram
*E	3163585	02/05/2011	CXQ	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*F	4311272	03/17/2014	CINM	Updated Package Drawing and Dimension: spec 51-85063 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*G	4586288	12/03/2014	CINM	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Ordering Information: Removed the prune part numbers CY29947AXC and CY29947AXCT.
*H	5270507	05/13/2016	PSR	Added Thermal Resistance. Updated Package Drawing and Dimension: spec 51-85063 – Changed revision from *D to *E. Updated to new template.

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