Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Block Mode, V_{CC} = 5 V, 25°C

Table 3. D.C. OPERATING CHARACTERISTICS, CAT93C56, Die Rev. G – New Product

(V_{CC} = +1.8 V to +5.5 V, T_A=−40°C to +125°C unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1 MHz, V_{CC} = 5.0 V			1	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1 MHz, V_{CC} = 5.0 V			500	μA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = GND	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		4	
I_{SB2}	Power Supply Current (Standby) (x16 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = Float or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, CS = GND	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V		−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V		2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 4.5 V		0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 4.5 V		V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = −400 μA		2.4		V
V_{OL2}	Output Low Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA			0.2	V
V_{OH2}	Output High Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OH} = −100 μA		V_{CC} − 0.2		V

Table 4. D.C. OPERATING CHARACTERISTICS, CAT93C56/57, Die Rev. E – Mature Product (CAT93C56, Rev. E – NOT RECOMMENDED FOR NEW DESIGNS) (V_{CC} = +1.8 V to +5.5 V, T_A=−40°C to +125°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1 MHz, V_{CC} = 5.0 V		3	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1 MHz, V_{CC} = 5.0 V		500	μA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = GND		10	μA
I_{SB2}	Power Supply Current (Standby) (x16 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = Float or V_{CC}		10	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, CS = GND		1	μA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V	−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 4.5 V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 4.5 V	V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA		0.2	V
V_{OH2}	Output High Voltage	1.8 V ≤ V_{CC} < 4.5 V, I_{OH} = −100 μA	V_{CC} − 0.2		V

Table 5. PIN CAPACITANCE (T_A = 25°C, f = 1 MHz, V_{CC} = 5 V)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT} (Note 4)	Output Capacitance (DO)	V_{OUT} = 0 V			5	pF
C_{IN} (Note 4)	Input Capacitance (CS, SK, DI, ORG)	V_{IN} = 0 V			5	pF

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 6. A.C. CHARACTERISTICS (Note 5)**, CAT93C56, Die Rev. G – New Product**
(V_{CC} = +1.8V to +5.5V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Limits		Units
		Min	Max	
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	μs
t_{PD0}	Output Delay to 0		0.25	μs
t_{HZ} (Note 6)	Output Delay to High−Z		100	ns
t_{EW}	Program/Erase Pulse Width		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		μs
t_{SKHI}	Minimum SK High Time	0.25		μs
t_{SKLOW}	Minimum SK Low Time	0.25		μs
t_{SV}	Output Delay to Status Valid		0.25	μs
SK_{MAX}	Maximum Clock Frequency	DC	2000	kHz

Table 7. A.C. CHARACTERISTICS (Note 5)**, CAT93C56/57, Die Rev. E – Mature Product**
(CAT93C56 Rev. E – NOT RECOMMENDED FOR NEW DESIGNS)

Symbol	Parameter	Limits						Units
		V_{CC} = 1.8 V – 5.5 V		V_{CC} = 2.5 V – 5.5 V		V_{CC} = 4.5 V – 5.5 V		
		Min	Max	Min	Max	Min	Max	
t_{CSS}	CS Setup Time	200		100		50		ns
t_{CSH}	CS Hold Time	0		0		0		ns
t_{DIS}	DI Setup Time	400		200		100		ns
t_{DIH}	DI Hold Time	400		200		100		ns
t_{PD1}	Output Delay to 1		1		0.5		0.25	μs
t_{PD0}	Output Delay to 0		1		0.5		0.25	μs
t_{HZ} (Note 6)	Output Delay to High−Z		400		200		100	ns
t_{EW}	Program/Erase Pulse Width		10		10		10	ms
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		μs
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		μs
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		μs
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	μs
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	kHz

Table 8. POWER−UP TIMING (Notes 6 and 7)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

5. Test conditions according to “A.C. Test Conditions” table.
6. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 9. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	0.2 V_{CC} to 0.7 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	0.5 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Output Load	Current Source I_{OLmax}/I_{OHmax}; CL=100 pF	

Device Operation

The CAT93C56/57 is a 2048−bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C56/57 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 10−bit instructions for 93C57 or seven 11−bit instructions for 93C56 control the reading, writing and erase operations of the device. When organized as X8, seven 11−bit instructions for 93C57 or seven 12−bit instructions for 93C56 control the reading, writing and erase operations of the device. The CAT93C56/57 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

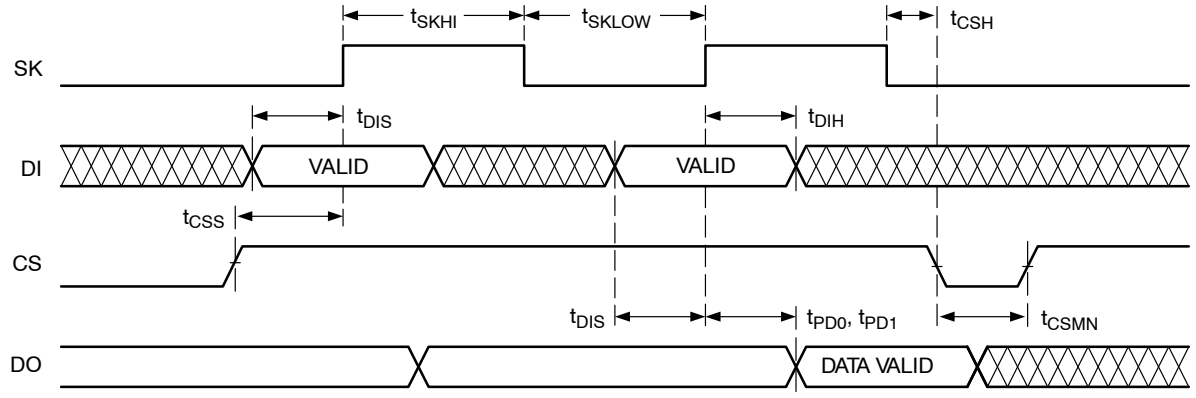


Figure 2. Synchronous Data Timing

The format for all instructions sent to the device is a logical “1” start bit, a 2−bit (or 4−bit) opcode, 7−bit address (CAT93C57) / 8−bit address (CAT93C56) (an additional bit when organized X8) and for write operations a 16−bit data field (8−bit for X8 organizations). The instruction format is shown in Instruction Set table.

Table 10. INSTRUCTION SET

Instruction	Device Type	Start Bit	Opcode	Address		Data		Comments
				x8	x16	x8	x16	
READ	93C56 (Note 8)	1	10	A8−A0	A7−A0			Read Address AN−A0
	93C57	1	10	A7−A0	A6−A0			
ERASE	93C56 (Note 8)	1	11	A8−A0	A7−A0			Clear Address AN−A0
	93C57	1	11	A7−A0	A6−A0			
WRITE	93C56 (Note 8)	1	01	A8−A0	A7−A0	D7−D0	D15−D0	Write Address AN−A0
	93C57	1	01	A7−A0	A6−A0	D7−D0	D15−D0	
EWEN	93C56 (Note 8)	1	00	11XXXXXXX	11XXXXXX			Write Enable
	93C57	1	00	11XXXXXX	11XXXXX			
EWDS	93C56 (Note 8)	1	00	00XXXXXXX	00XXXXXX			Write Disable
	93C57	1	00	00XXXXXX	00XXXXX			
ERAL	93C56 (Note 8)	1	00	10XXXXXXX	10XXXXXX			Clear All Addresses
	93C57	1	00	10XXXXXX	10XXXXX			
WRAL	93C56 (Note 8)	1	00	01XXXXXXX	01XXXXXX	D7−D0	D15−D0	Write All Addresses
	93C57	1	00	01XXXXXX	01XXXXX	D7−D0	D15−D0	

8. Address bit A8 for 256x8 organization and A7 for 128x16 organization are “Don’t Care” bits, but must be kept at either a “1” or “0” for READ, WRITE and ERASE commands.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C56/57 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAT93C56/57, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 3.

Erase/Write Enable and Disable

The CAT93C56/57 powers up in the write disable state. Any writing after power−up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C56/57 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

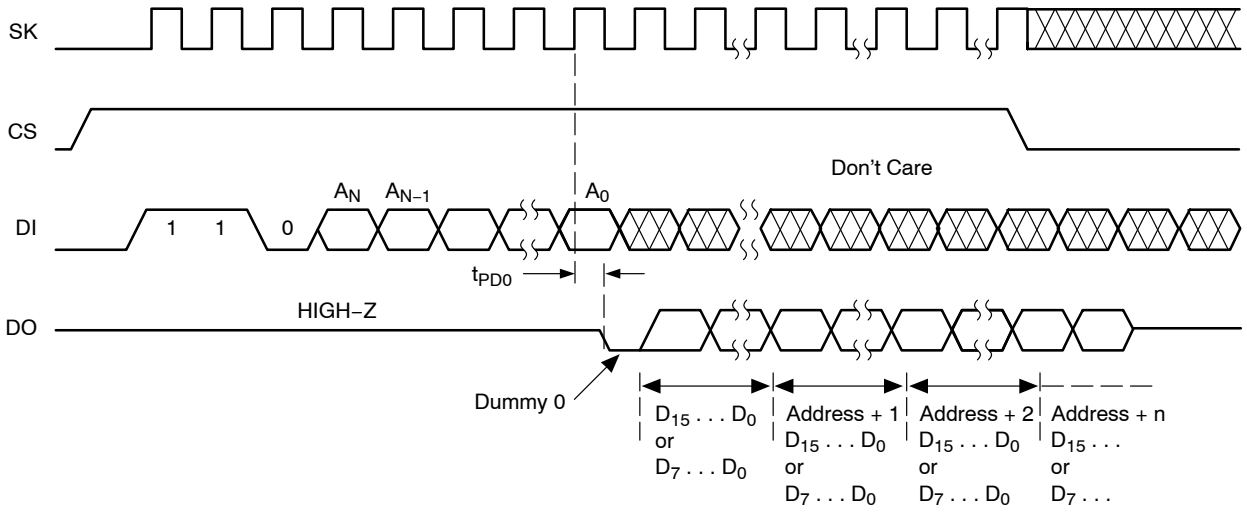


Figure 3. READ Instruction Timing

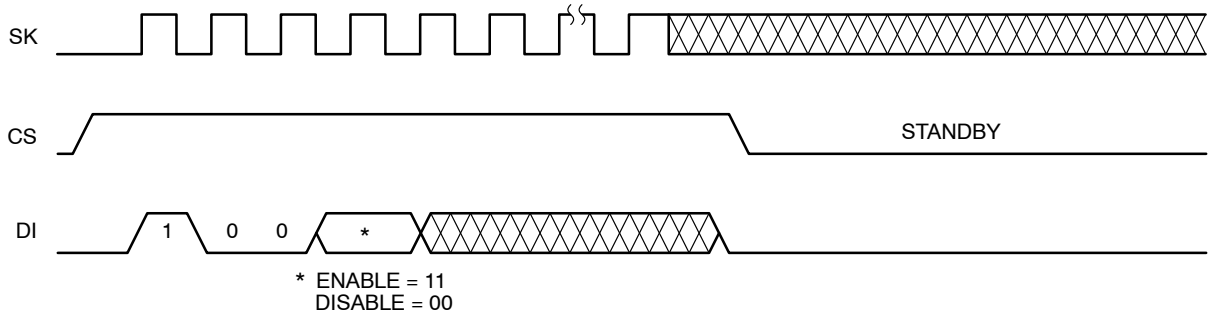


Figure 4. EWEN/EWDS Instruction Timing

Write

After receiving a WRITE command (Figure 5), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/57 can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 6). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SaK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/57 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

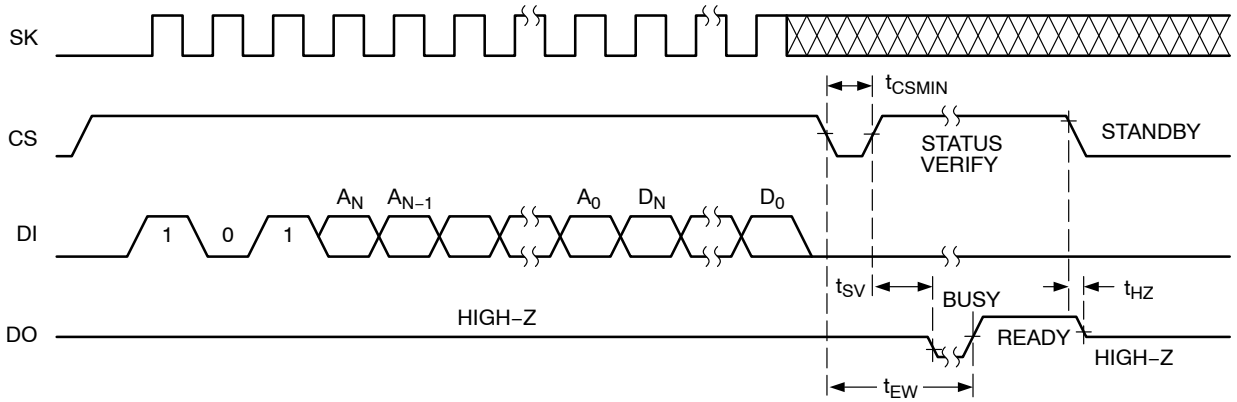


Figure 5. Write Instruction Timing

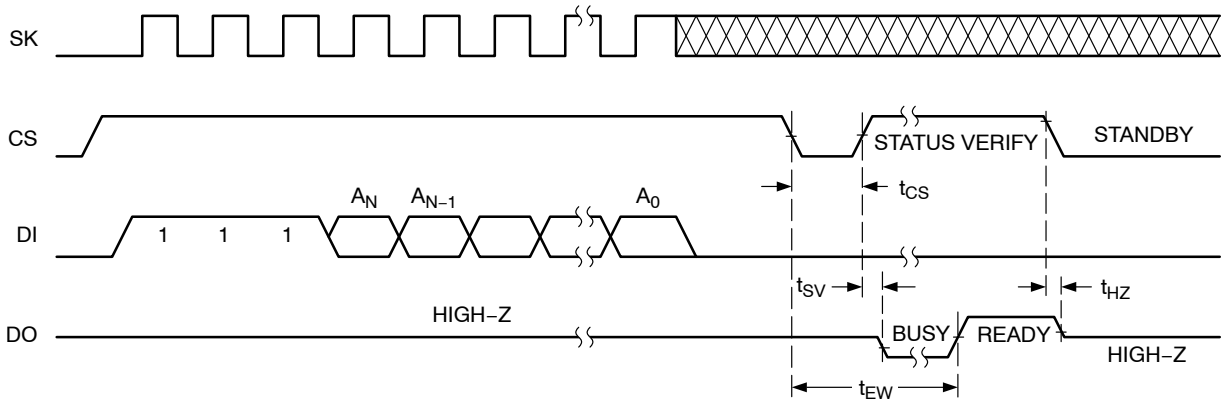


Figure 6. Erase Instruction Timing

Erase All

Upon receiving an ERAL command (Figure 7), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/57 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 8). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C56/57 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

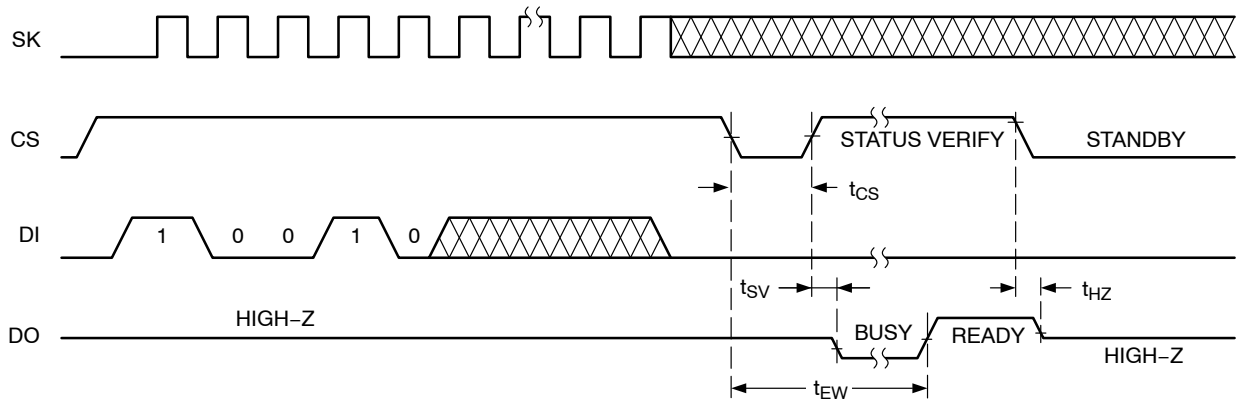


Figure 7. ERAL Instruction Timing

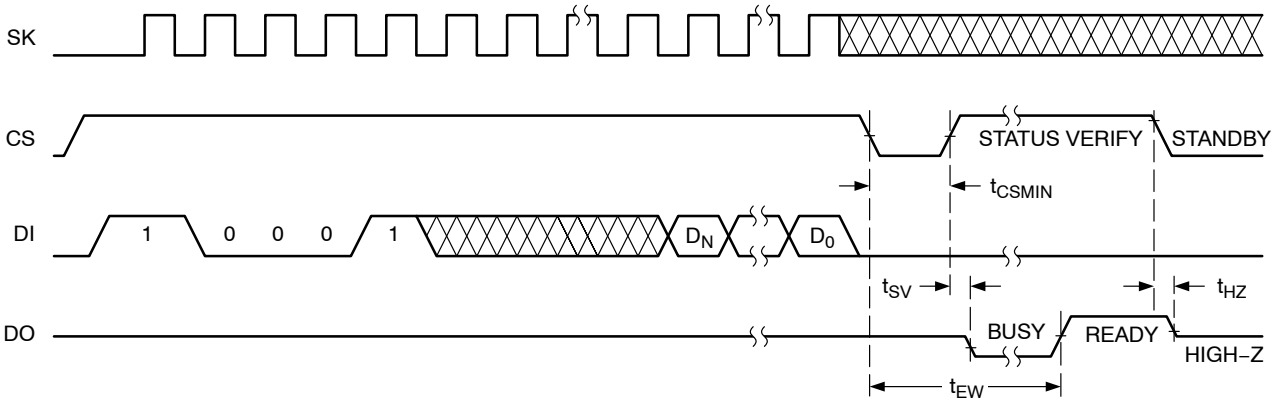
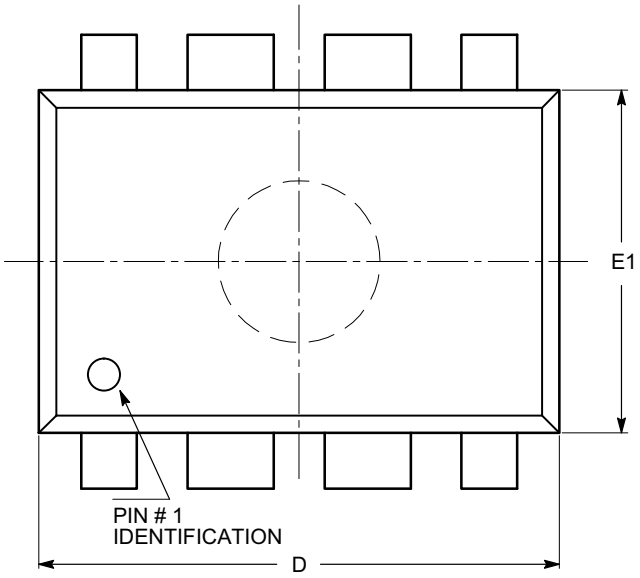


Figure 8. WRAL Instruction Timing

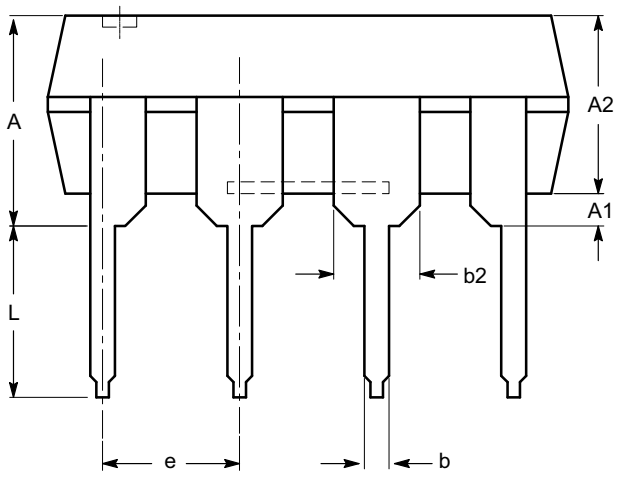
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

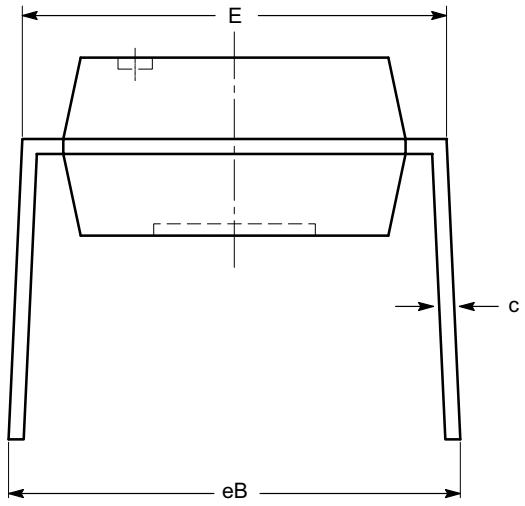


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

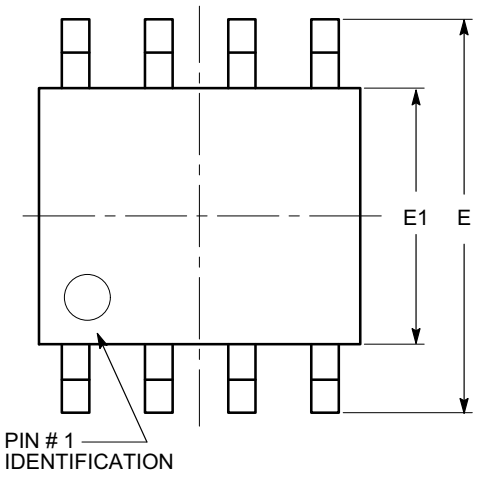


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

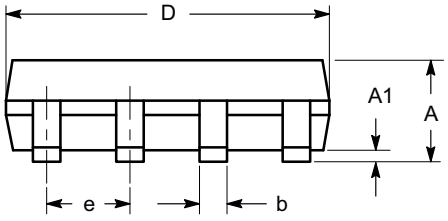
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

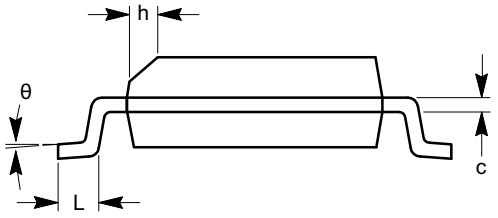


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

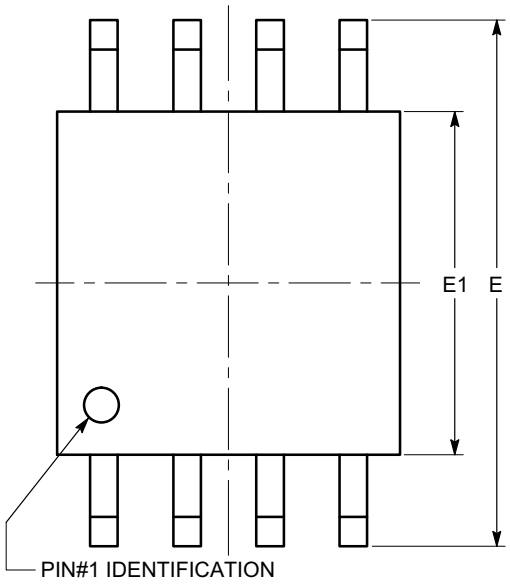


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

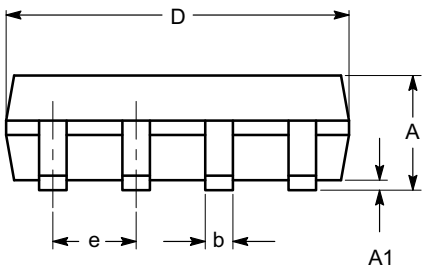
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE−01
ISSUE O

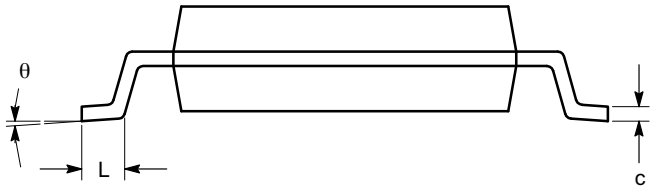


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e		1.27 BSC	
L	0.51		0.76
θ	0°		8°



SIDE VIEW

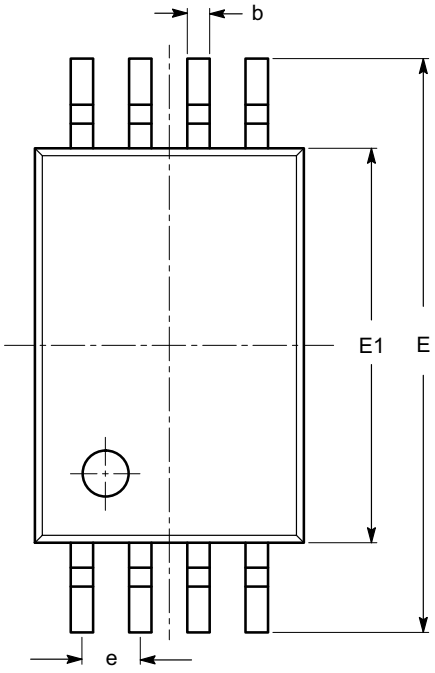


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

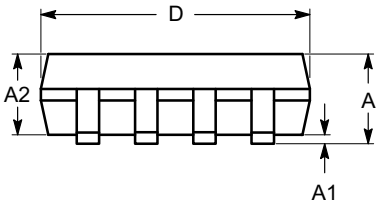
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

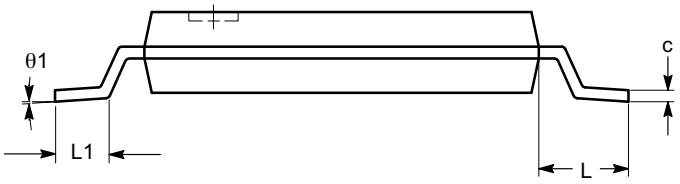


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

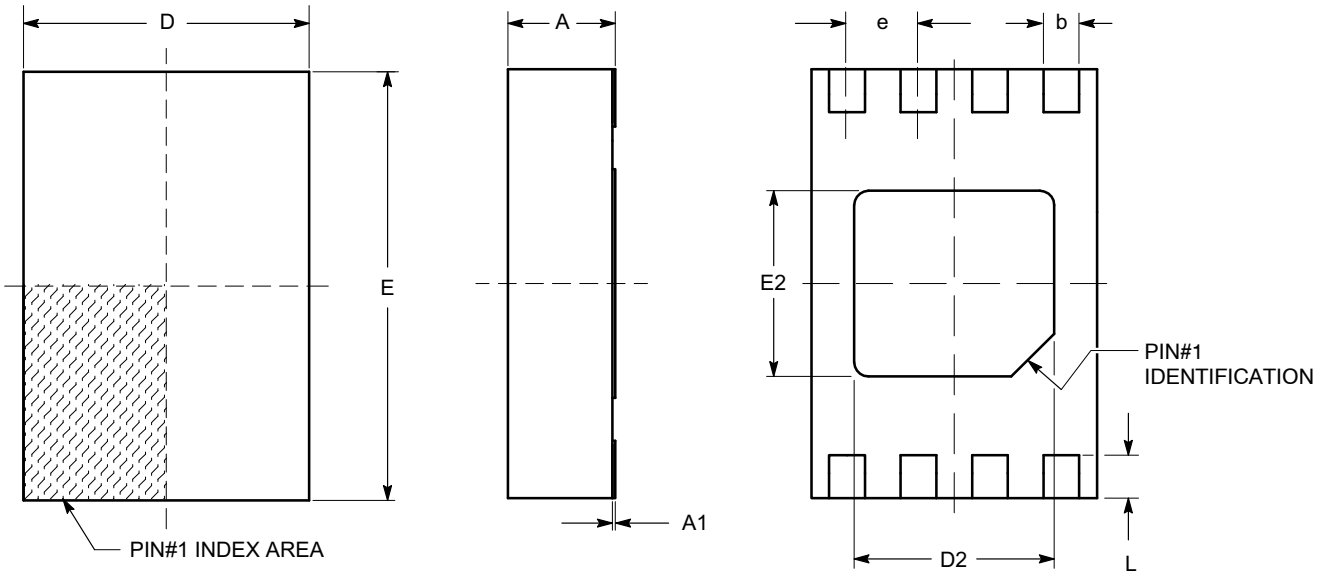


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

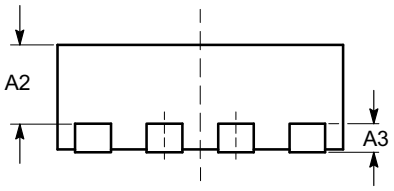
PACKAGE DIMENSIONS

TDFN8, 2x3
CASE 511AK−01
ISSUE A



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40

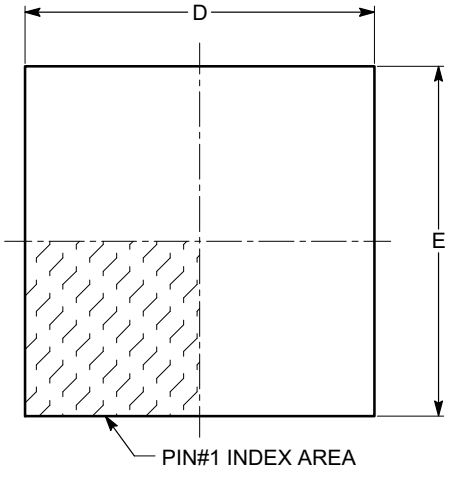


FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

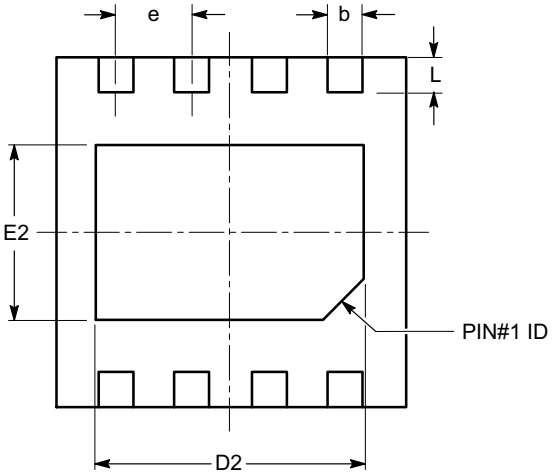
PACKAGE DIMENSIONS

TDFN8, 3x3
CASE 511AL−01
ISSUE A



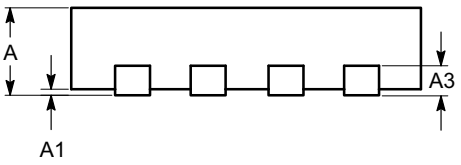
TOP VIEW

SIDE VIEW



BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.23	0.30	0.37
D	2.90	3.00	3.10
D2	2.20	−−−	2.50
E	2.90	3.00	3.10
E2	1.40	−−−	1.80
e		0.65 TYP	
L	0.20	0.30	0.40

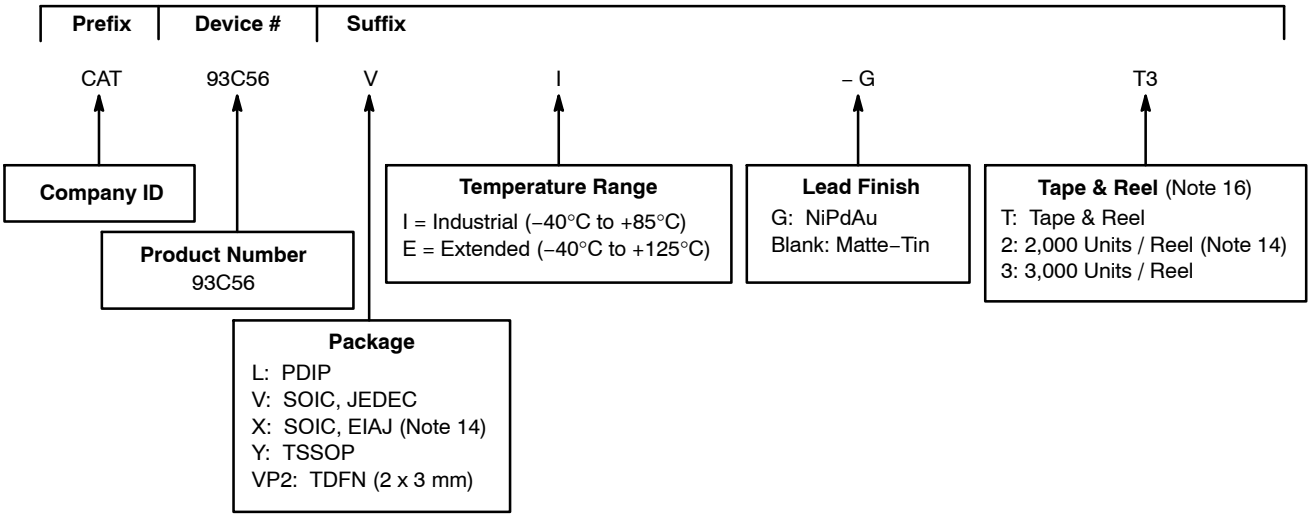


FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

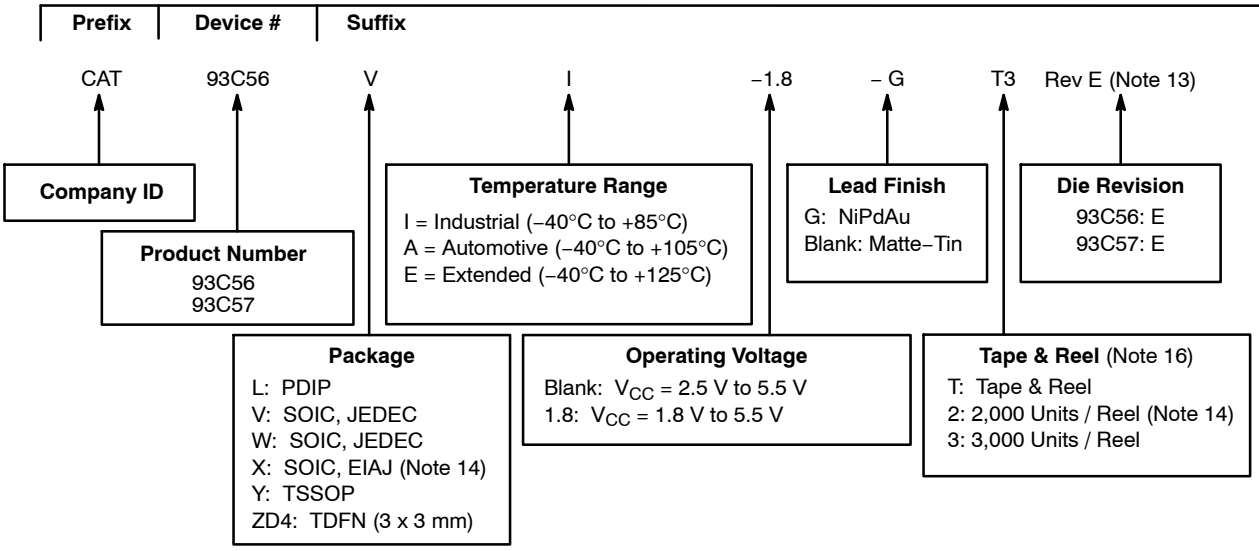
Example of Ordering Information

CAT93C56, Die Rev. G, New Product



9. The device used in the above example is a CAT93C56VI–GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).

CAT93C56/57, Die Rev. E, Mature Product
(CAT93C56, Rev. E – Not Recommended for New Designs)



10. All packages are RoHS–compliant (Lead–free, Halogen–free).
11. The standard lead finish is NiPdAu.
12. The device used in the above example is a CAT93C56VI–1.8–GT3 (SOIC green package, Industrial Temperature, 1.8 Volt to 5.5 Volt Operating Voltage, NiPdAu finish, Tape & Reel).
13. Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWE). For additional information, please contact your ON Semiconductor sales office.
14. For SOIC, EIAJ (X) package the standard lead finish is Matte–Tin. This package is available in 2,000 pcs/reel, i.e. CAT93C56XI–T2.
15. For additional package and temperature options, please contact your nearest ON Semiconductor sales office.
16. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

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Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

CAT93C56/D