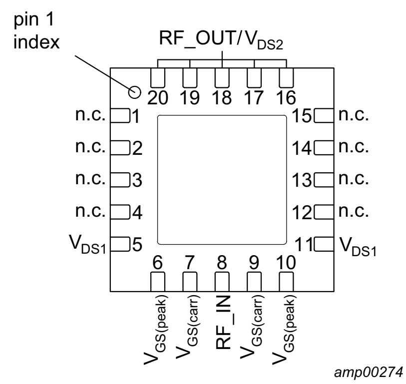
2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
V_{DS1}	5	drain-source voltage of driver stages
$V_{GS(peak)}$	6	gate-source voltage of peaking
$V_{GS(carr)}$	7	gate-source voltage of carrier
RF_IN	8	RF input
$V_{GS(carr)}$	9	gate-source voltage of carrier
$V_{GS(peak)}$	10	gate-source voltage of peaking
V_{DS1}	11	drain-source voltage of driver stages
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
n.c.	15	not connected
RF_OUT/V_{DS2}	16	RF output / drain-source voltage of final stages
RF_OUT/V_{DS2}	17	RF output / drain-source voltage of final stages
RF_OUT/V_{DS2}	18	RF output / drain-source voltage of final stages

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT/V_{DS2}	19	RF output / drain-source voltage of final stages
RF_OUT/V_{DS2}	20	RF output / drain-source voltage of final stages
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM9D2527-20AB	PQFN20	plastic thermal enhanced quad flat package; no leads; 20 terminals; body 8.0 x 8.0 x 2.1 mm	SOT1462-1

4. Block diagram

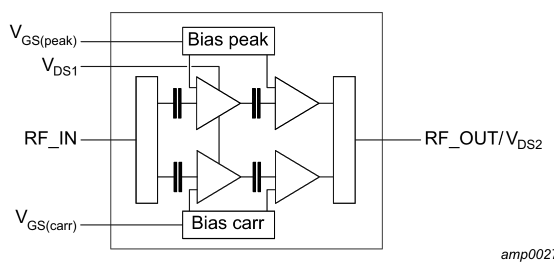


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	175	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; $P_{L(AV)}$ = 3 W	[1]	12	K/W
		T_{case} = 90 °C; $P_{L(AV)}$ = 1.25 W	[1]	17	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 8 dB.

7. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 37 mA	1.65	2.2	2.75	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA

Table 7. RF Characteristics
Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 37 mA (carrier); $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.5 V; P_L = 2 W; f = 2.7 GHz. Unless otherwise specified, measured in an Ampleon production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: CW						
G_p	power gain		26	27.2	29	dB
η_D	drain efficiency	P_L = 2 W	36	41	-	%
		P_L = $P_{L(3dB)}$	50	56	-	%
RL_{in}	input return loss		-	−19	−10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		43	43.6	-	dBm

8. Application information

Table 8. Typical performance

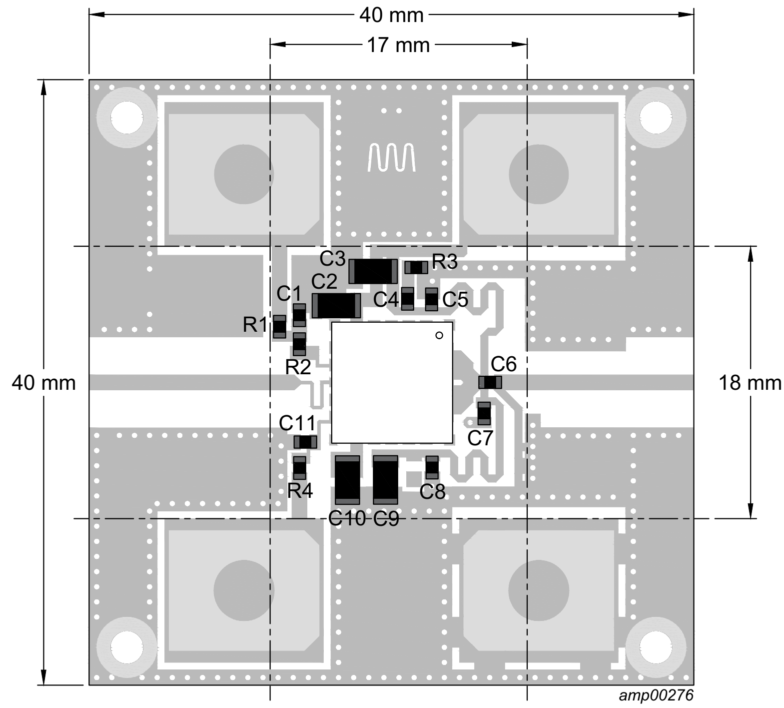
Test signal: 1-carrier W-CDMA;T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 43 mA (driver and final stages); test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF; unless otherwise specified, measured in an Ampleon 2620 MHz to 2690 MHz frequency band asymmetrical Doherty application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 2655 MHz [1]	-	43.4	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	f = 2655 MHz; at 3 dB compression point [2]	-	–14.5	-	°
η_D	drain efficiency	8 dB OBO ($P_{L(AV)}$ = 35.8 dBm); f = 2620 MHz	-	46.1	-	%
G_p	power gain	$P_{L(AV)}$ = 35.8 dBm; f = 2620 MHz	-	27.3	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 34.5 dBm set to obtain IMD3 = –30 dBc; 2-tone CW; f = 2655 MHz	-	265	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 35.8 dBm; f = 2620 MHz to 2170 MHz	-	0.2	-	dB
$ACPR_{5M}$	adjacent channel power ratio (5M)	$P_{L(AV)}$ = 35.8 dBm; f = 2655 MHz	-	–33.3	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 2655 MHz	-	0.04	-	dB/°C
K	Rollett stability factor	T_{case} = –40 °C; f = 0.15 GHz to 5 GHz [3]	-	>1.7	-	

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 μs).

[2] 25 ms CW power sweep measurement.

[3] S-parameters measured with load-pull jig.



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

Table 9. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C11	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: GRM31CR61H106KA12L
C2, C3, C9, C10	multilayer ceramic chip capacitor	1 μF, 6.3 V	TDK: C1608X5R0J106K080AB
C4	multilayer ceramic chip capacitor	100 pF	Murata: GQM1875C2E1R6BB12
C5, C8	multilayer ceramic chip capacitor	4.7 pF	Murata: GQM1875C2E5R6BB12
C6	multilayer ceramic chip capacitor	1.8 pF	Murata: GQM1875C2E7R5BB12
C7	multilayer ceramic chip capacitor	1.6 pF	Murata: GQM1875C2ER50BB12
J1	SMA Coaxial panel connector male		Hubner & Suhner: 13_SMA-50-0-2/111_N
J2	SMA Coaxial panel connector female		Hubner & Suhner: 13_SMA-50-0-2/111_N
R1	SMD resistor	820 Ω, ±1 %	Multicomp: MC805
R2	SMD resistor	5.1 Ω, ±1 %	Multicomp: MC805
R3, R4	SMD resistor	10 Ω, ±1 %	Multicomp: MC805
T1, T2, T3, T4	PCB Terminal	6.35 mm × 0.81 mm; 4.1 mm	TE connectivity

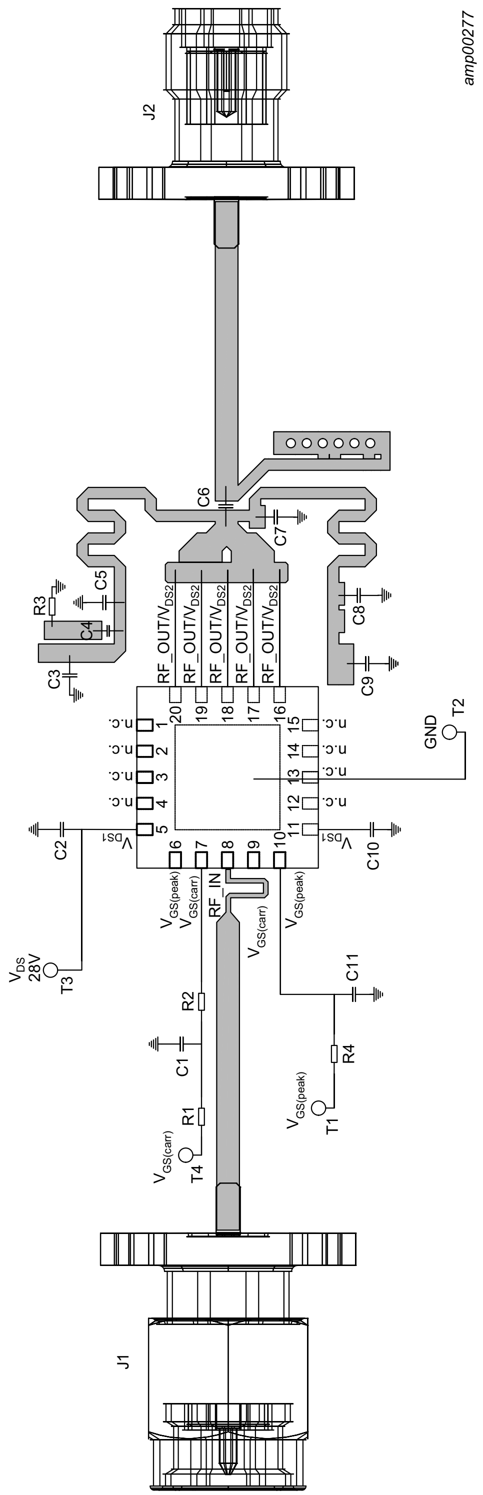


Fig 4. Electrical schematic

8.1 Ruggedness in a Doherty operation

The BLM9D2527-20AB is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 37 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_i corresponding to $P_{L(3dB)}$ under Z_S = 50 Ω load; f = 2700 MHz (CW); T_{case} = 25 °C.

8.2 Impedance information

Table 10. Typical impedance for optimum Doherty operation

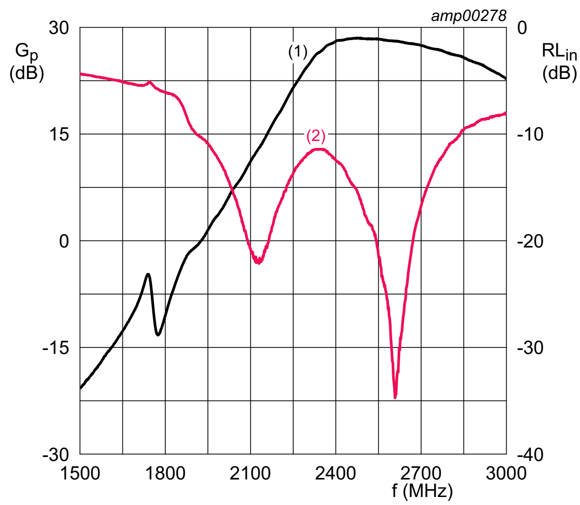
Measured load-pull data per section; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 35 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; t_p = 100 μs; δ = 10 %. Typical values.

	tuned for optimum Doherty operation				
f	Z_L	$G_{p(max)}$	P_L	η_{add} [1]	η_{add} [2]
(MHz)	(Ω)	(dB)	(dBm)	(%)	(%)
2450	4.97 – j0.76	28.60	43.80	51.00	51.30
2500	5.48 – j0.92	28.60	43.80	51.20	52.80
2500	5.97 – j1.02	28.40	43.90	53.30	52.20
2600	6.73 – j1.22	28.30	43.70	53.80	52.00
2650	7.20 – j1.31	28.20	43.70	54.70	52.10
2700	7.59 – j1.21	28.20	43.60	56.50	52.40
2750	7.93 – j1.04	28.00	43.50	56.60	50.30

[1] at 43 dBm (nearly 3 dB compression point).

[2] at 35 dBm (nearly 8 dB OBO point).

8.3 Graphs



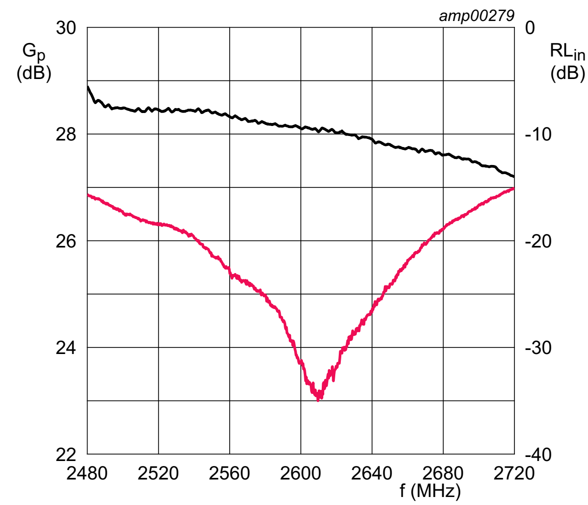
T_{case} = 25 °C; V_{DS} = 28 V; P_L = 1 W;
I_{Dq1} + I_{Dq2} = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

Test signal: CW.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 5. Wideband power gain and input return loss as function of frequency; typical values



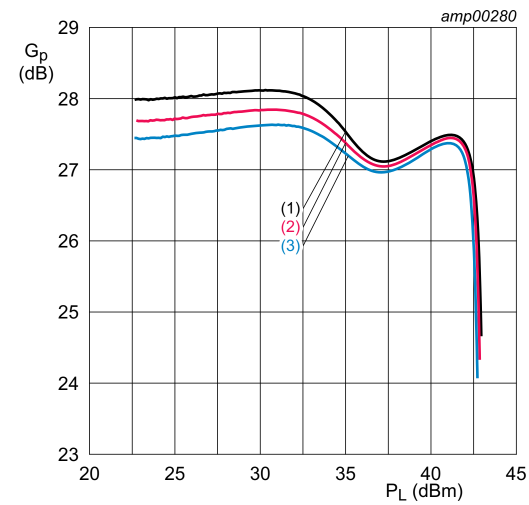
T_{case} = 25 °C; V_{DS} = 28 V; P_L = 1 W;
I_{Dq1} + I_{Dq2} = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

Test signal: CW.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 6. In-band power gain and input return loss as function of frequency; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

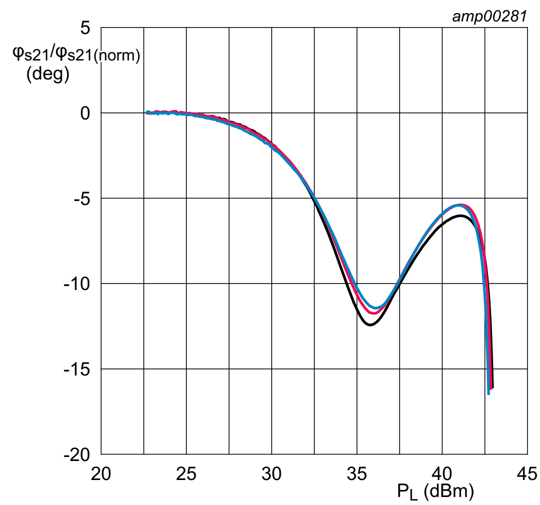
Test signal: CW.

(1) f = 2620 MHz

(2) f = 2655 MHz

(3) f = 2690 MHz

Fig 7. Power gain as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

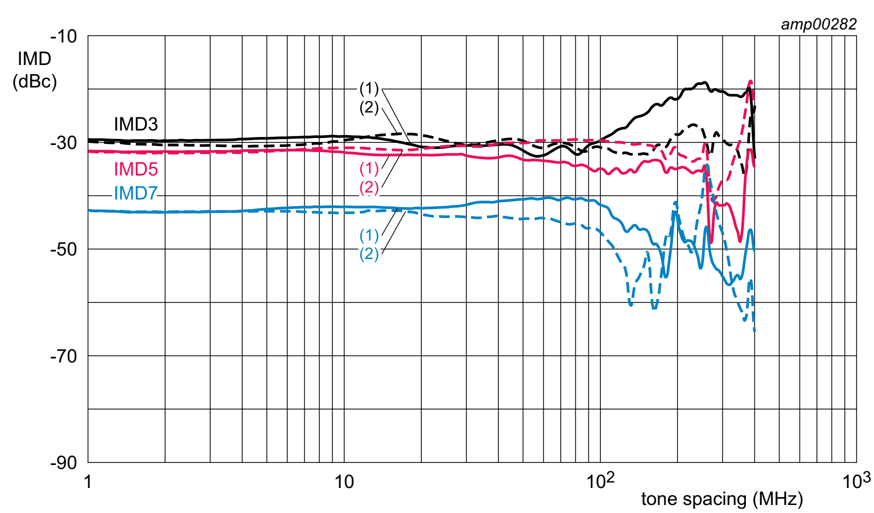
Test signal: CW.

(1) f = 2620 MHz

(2) f = 2655 MHz

(3) f = 2690 MHz

Fig 8. Normalized phase response as a function of output power; typical values



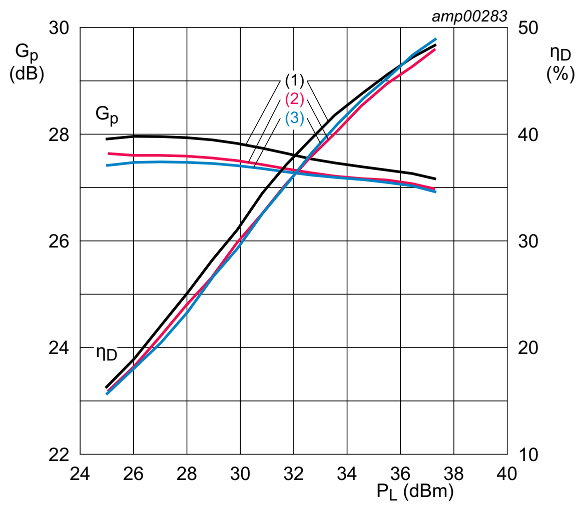
T_{case} = 25 °C; V_{DS} = 28 V; P_L = 34.5 dBm; I_{Dq1} + I_{Dq2} = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage); V_{GS} = 1.54 V (peaking stage).

Test signal: CW.

(1) IMD low

(2) IMD high

Fig 9. Intermodulation distortion as a function of tone spacing; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

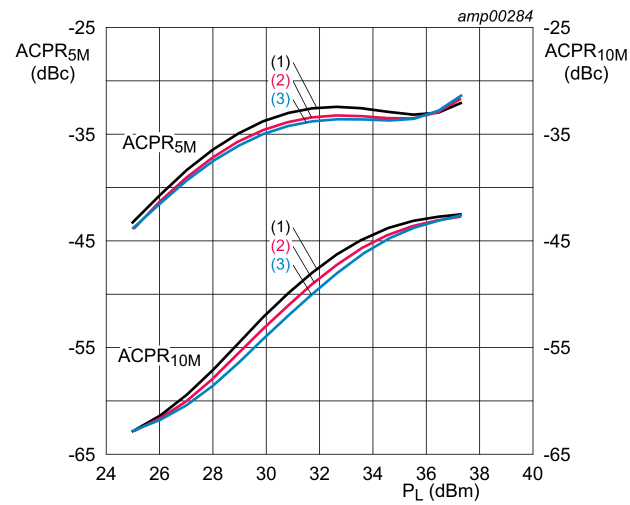
Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

(1) f = 2620 MHz

(2) f = 2655 MHz

(3) f = 2690 MHz

Fig 10. Power gain and drain efficiency as function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage);
V_{GS} = 1.54 V (peaking stage).

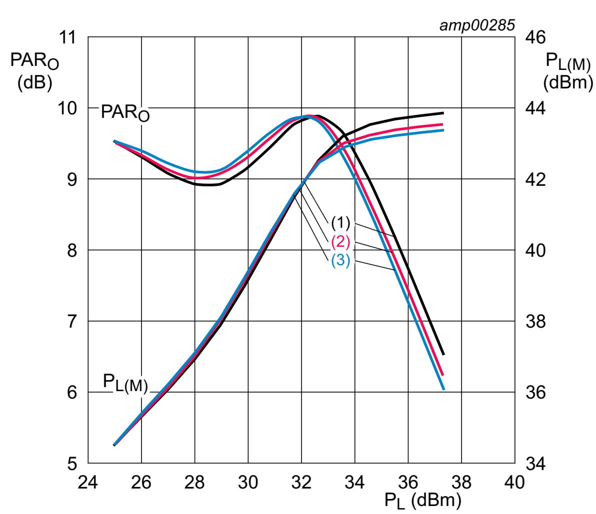
Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

(1) f = 2620 MHz

(2) f = 2655 MHz

(3) f = 2690 MHz

Fig 11. Adjacent channel power ratio as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V; $I_{Dq1} + I_{Dq2}$ = 43 mA (carrier and peaking stages);
V_{GS} = 2.29 V (carrier stage); V_{GS} = 1.54 V (peaking stage).

Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

(1) f = 2620 MHz

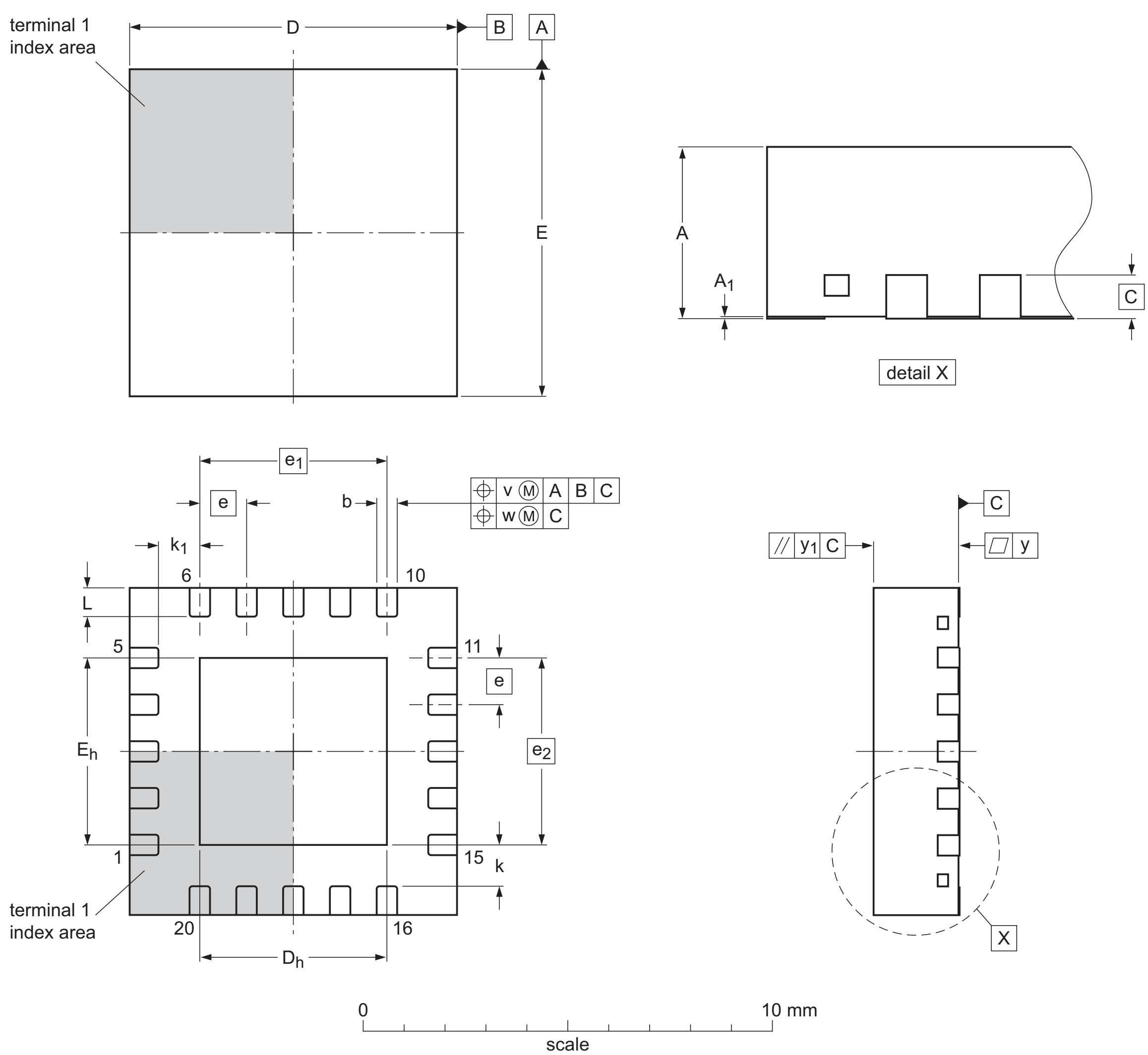
(2) f = 2655 MHz

(3) f = 2690 MHz

Fig 12. Output peak-to-average ratio and peak output power as function of output power; typical values

9. Package outline

PQFN20: plastic thermal enhanced quad flat package; no leads; 20 terminals; body 8.0 x 8.0 x 2.1 mm **SOT1462-1**



Dimensions

Unit		A(1)	A1	b	C	D(1)	Dh	E(1)	Eh	e	e1	e2	k	k1	L	v	w	y	y1
mm	max	2.20	0.05	0.60		8.1	4.72	8.1	4.72						0.8				
	nom	2.10		0.50	0.508	8.0	4.62	8.0	4.62	1.15	4.6	4.6			0.7	0.1	0.05	0.1	0.1
	min	2.00	0.00	0.40		7.9	4.52	7.9	4.52				0.99	0.99	0.6				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1462-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1462-1						~~15-10-12~~ 17-06-23

Fig 13. Package outline SOT1462-1 (PQFN20)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V, but fails after exposure to an ESD pulse of 1000 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
AM	Amplitude Modulation
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN9	Ninth Generation
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM9D2527-20AB v.1	20170629	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

15. Contents

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