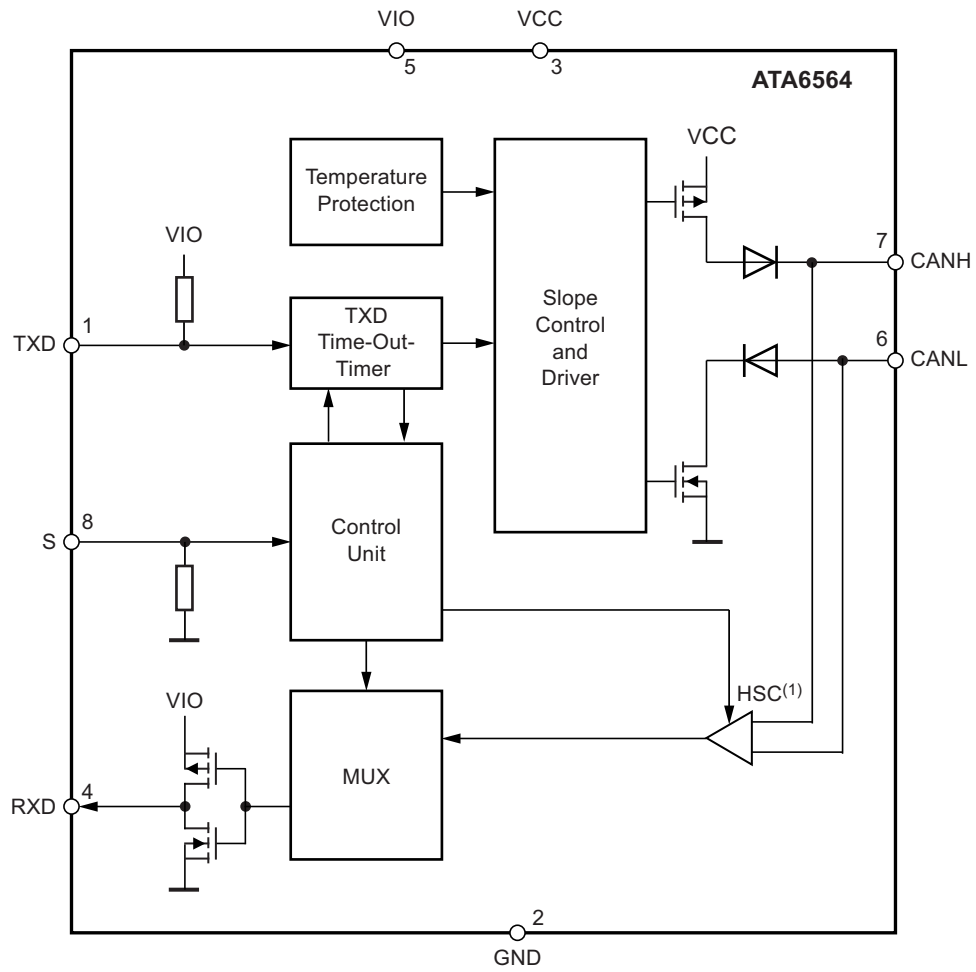
ATA6564 Family Members

Device	Grade 0	Grade 1	VDFN8	SOIC8	Description
ATA6564-GAQW0	x			x	Silent mode, VIO - pin for compatibility with 3,3V and 5V microcontroller
ATA6564-GBQW0	x		x		Silent mode, VIO - pin for compatibility with 3,3V and 5V microcontroller
ATA6564-GAQW1		x		x	Silent mode, VIO - pin for compatibility with 3,3V and 5V microcontroller
ATA6564-GBQW1		x	x		Silent mode, VIO - pin for compatibility with 3,3V and 5V microcontroller

Functional Block Diagram



Note 1: HSC: High-speed comparator.

1.0 DEVICE OVERVIEW

The ATA6564 is a stand-alone high-speed CAN transceiver compliant with the ISO 11898-2, ISO 11898-2: 2016 and SAE J2962-2 CAN standards. It provides very low current consumption in Silent mode.

1.1 Operating Modes

The ATA6564 supports two operating modes: Silent and Normal. These modes can be selected via the S pin. See Figure 1-1 and Table 1-1 for a description of the operating modes.

FIGURE 1-1: OPERATING MODES

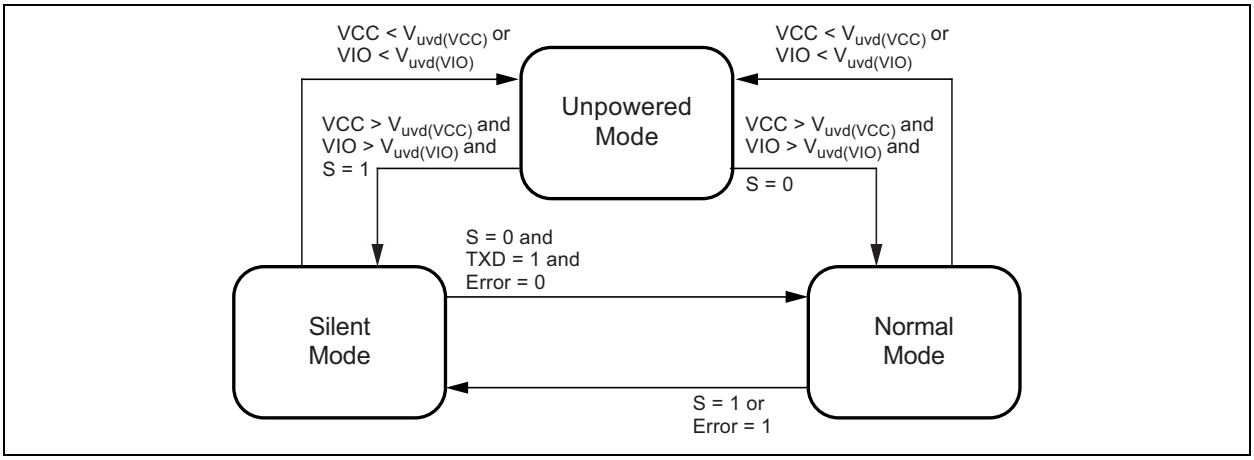


TABLE 1-1: OPERATING MODES

Mode	Inputs		Outputs	
	S	Pin TXD	CAN Driver	Pin RXD
Unpowered	x(2)	x(2)	Recessive	Recessive
Silent	HIGH	x(2)	Recessive	Active(1)
Normal	LOW	LOW	Dominant	LOW
	LOW	HIGH	Recessive	HIGH

Note 1: LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.
2: Irrelevant

1.1.1 NORMAL MODE

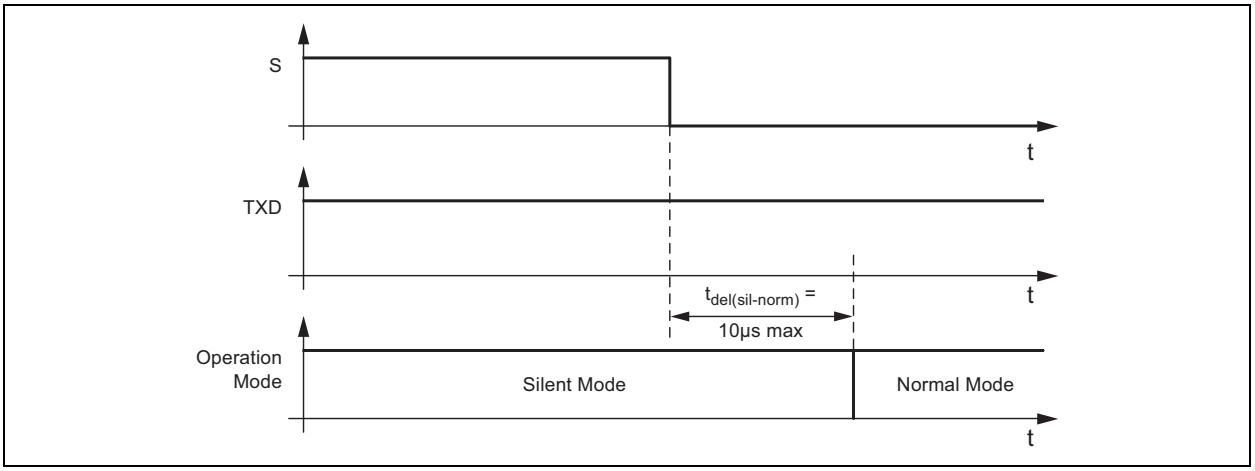
A low level on the S pin together with a high level on pin TXD selects the Normal mode. In this mode the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see **Section "Functional Block Diagram"**). The output driver stage is active and drives data from the TXD input to the CAN bus. The high-speed comparator (HSC) converts the analog data on the bus lines into digital data which is output to pin RXD. The bus biasing is set to $V_{VCC}/2$ and the undervoltage monitoring of VCC is active.

The slope of the output signals on the bus lines is controlled and optimized in a way that ensures the lowest possible electromagnetic emission (EME).

To switch the device in normal operating mode, set the S pin to low and the TXD pin to high (see Table 1-1 and Figure 1-2). The S pin provides a pull-down resistor to GND, thus ensuring a defined level if the pin is open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

FIGURE 1-2: SWITCHING FROM SILENT MODE TO NORMAL MODE



1.1.2 SILENT MODE

A high level on the S pin selects Silent mode. This receive-only mode can be used to test the connection of the bus medium. In Silent mode the ATA6564 can still receive data from the bus, but the transmitter is disabled and therefore no data can be sent to the CAN bus. The bus pins are released to recessive state. All other IC functions, including the high-speed comparator (HSC), continue to operate as they do in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

1.2 Fail-safe Features

1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to LOW. If the LOW state on the TXD pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin is set to high. If the low state on the TXD pin was longer than $t_{to(dom)TXD}$, then the TXD pin has to be set to high longer 4 µs in order to reset the TXD dominant time-out timer.

1.2.2 INTERNAL PULL-UP/PULL-DOWN STRUCTURE AT THE TXD AND S INPUT PINS

The TXD pin has an internal pull-up resistor to VIO and the S pin an internal pull-down resistor to GND. This ensures a safe, defined state in case one or all of these pins are left floating.

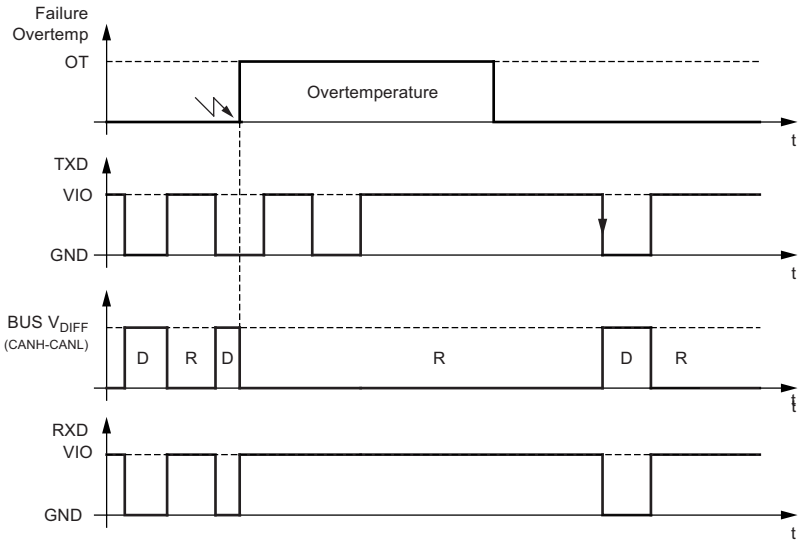
1.2.3 UNDERVOLTAGE DETECTION ON PINS VCC AND VIO

If V_{VCC} or V_{VIO} drop below their respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd(VIO)}$ (see Section TABLE 2-1:, Electrical Characteristics), the transceiver switches off and disengages from the bus until V_{VCC} and V_{VIO} have recovered. The logic state of the S pin is ignored until the VCC voltage or the VIO voltage has recovered.

1.2.4 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, T_{Jsd}, the output drivers are disabled until the junction temperature drops below T_{Jsd} and pin TXD is at high level again. This ensures that output driver oscillations due to temperature drift are avoided.

FIGURE 1-3: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION



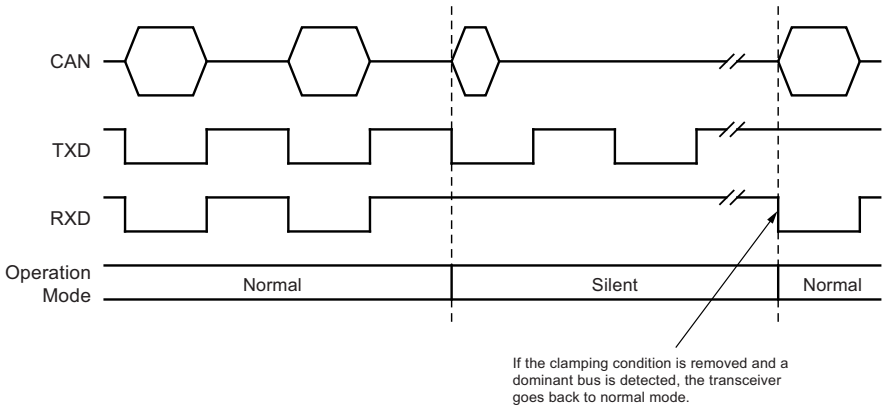
1.2.5 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches off the bus transmitter.

1.2.6 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD line is clamped to HIGH (e.g., recessive). That is, if the RXD pin cannot signalize a dominant bus condition because it is e.g, shorted to VCC, the transmitter within ATA6564 is disabled to avoid possible data collisions on the bus. In Normal and Silent mode, the device permanently compares the state of the high-speed comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than t_{RC_det} without the RXD pin doing the same, a recessive clamping situation is detected and the device is forced into Silent mode. This Fail-safe mode is released by either entering Unpowered mode or if the RXD pin is showing a dominant (e.g., LOW) level again.

FIGURE 1-4: RXD RECESSIVE CLAMPING DETECTION



1.3 Pin Descriptions

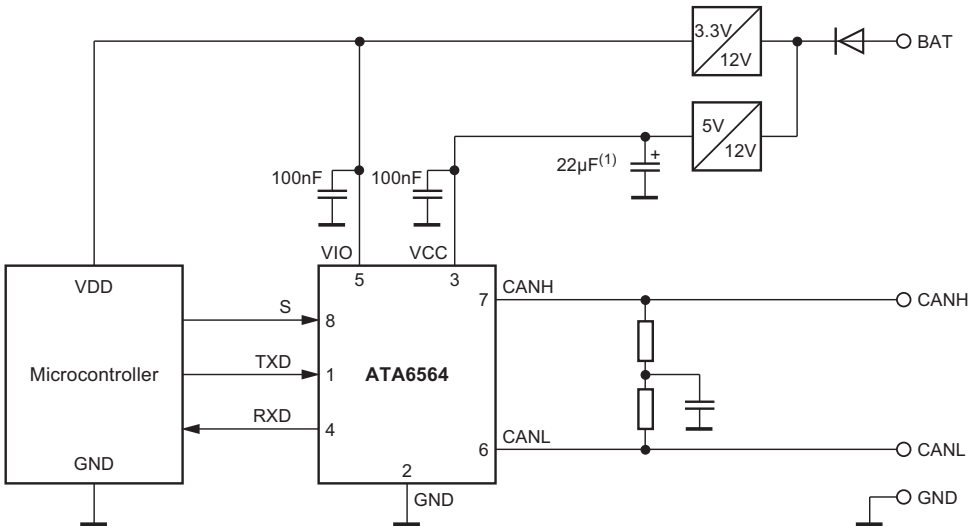
The descriptions of the pins are listed in Table 1-2.

TABLE 1-2: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	TXD	Transmit data input
2	GND	Ground supply
3	VCC	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	VIO	Supply voltage for I/O level adapter
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	S	Silent mode control input
9	EP(1)	Exposed Thermal Pad: Heat slug, internally connected to the GND pin.

Note 1: Only for the VDFN package.

1.4 Typical Application



(1) The size of this capacitor depends on the used external voltage regulator.

Note 1: For VDFN package: Heat slug must always be connected to GND.

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

DC Voltage at CANH and CANL ..... –27V to +42V
Transient Voltage on CANH and CANL (ISO 7637 part 2) ..... –150V to +100V
Max. differential bus voltage ..... –5V to +18V
DC voltage on all other pins ..... –0.3V to +5.5V
ESD on CANH and CANL pins (IEC 61000-4-2) ..... ±8 kV
ESD (HBM following STM 5.1 with 1.5 kΩ/100 pF) (Pins CANH, CANL to GND) ..... ±6 kV
Component Level ESD (HBM according to ANSI/ESD STM 5.1) JESD22-A114, AEC-Q 100 (002) ..... ±4 kV
CDM ESD STM 5.3.1 ..... ±750V
ESD machine model AEC-Q100-RevF(003) ..... ±200V
Virtual Junction Temperature ..... –40°C to +175°C
Storage Temperature ..... –55°C to +150°C

† Notice: Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C, Grade 0: T_{amb} = –40°C to +150°C, $T_{vJ} \leq 170°C$, V_{VCC}= 4.5V to 5.5V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF, unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	V_{VCC}	4.5	—	5.5	V	
Supply Current in Silent Mode	I_{VCC_sil}	1.9	2.5	3	mA	Silent Mode, $V_{TXD} = V_{VIO}$
Supply Current in Normal Mode	I_{VCC_rec} I_{VCC_dom} I_{VCC_short}	2 30	50	5 70 85	mA	Recessive, $V_{TXD} = V_{VIO}$ Dominant, V_{TXD} = 0V Short between CANH and CANL(**Note 1**)
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
I/O Level Adapter Supply, Pin VIO						
Supply Voltage on Pin VIO	V_{VIO}	2.8	—	5.5	V	
Supply Current on Pin VIO	I_{VIO_rec}	10	80	250	µA	Normal and Silent Mode recessive, $V_{TXD} = V_{VIO}$
	I_{VIO_dom}	50	350	500	µA	Normal and Silent Mode dominant, V_{TXD} = 0V
Undervoltage Detection Threshold on Pin VIO	$V_{uvd(VIO)}$	1.3	—	2.7	V	
Mode Control Input, Pin S						
High-Level Input Voltage	V_{IH}	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	0.3 × V_{VIO}	V	
Pull-Down Resistor to GND	R_{pd}	75	125	175	kΩ	$V_S = V_{VIO}$
Low-Level Leakage Current	I_L	–2	—	+2	µA	V_S = 0V
CAN Transmit Data Input, Pin TXD						
High-Level Input Voltage	V_{IH}	0.7 × V_{VIO}	—	V_{VIO} + 0.3	V	
Low-Level Input Voltage	V_{IL}	–0.3	—	0.3 × V_{VIO}	V	
Pull-up Resistor to VIO	R_{TXD}	20	35	50	kΩ	V_{TXD} = 0V
High-Level Leakage Current	I_{TDX}	–2	—	+2	µA	Normal Mode, $V_{TXD} = V_{VIO}$
Input Capacitance	C_{TXD}	—	5	10	pF	**Note 3**
CAN Receive Data Output, Pin RXD						
High-Level Output Current	I_{OH}	–8	—	-1	mA	$V_{RXD} = V_{VIO}$ – 0.4V, $V_{VIO} = V_{VCC}$
Low-Level Output Current	I_{OL}	2	—	12	mA	V_{RXD} = 0.4V, Bus Dominant
Bus Lines, Pins CANH and CANL						
Single Ended Dominant Output Voltage	$V_{O(dom)}$	 2.75 0.5	 3.5 1.5	 4.5 2.25	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 50Ω to 65Ω - pin CANH - pin CANL(**Note 1**)

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C, Grade 0: T_{amb} = –40°C to +150°C, $T_{vJ} \leq 170°C$, V_{VCC}= 4.5V to 5.5V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF, unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transmitter Voltage Symmetry	V_{Sym}	0.9	1	1.1	—	$V_{Sym} = (V_{CANH} + V_{CANL}) / V_{VCC}$ (**Note 3**)
Bus Differential Output Voltage	V_{Diff}	1.5	—	3	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 45Ω to 65Ω
		1.5	—	3.3	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 70Ω (**Note 3**)
		1.5	—	5	V	V_{TXD} = 0V, $t < t_{to(dom)TXD}$ R_L = 2240Ω (**Note 3**)
		–50	—	+50	mV	V_{VCC} = 4.75V to 5.25V $V_{TXD} = V_{VIO}$, receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	0.5 x V_{VCC}	3	V	Normal and Silent Mode, $V_{TXD} = V_{VIO}$, no load
Differential Receiver Threshold Voltage (HSC)	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal and Silent Mode, $V_{cm(CAN)}$ = –27V to +27V
Differential Receiver Hysteresis Voltage (HSC)	$V_{hys(RX)dif}$	50	120	200	mV	Normal and Silent Mode, $V_{cm(CAN)}$ = –27V to +27V
Dominant Output Current	$I_{IO(dom)}$	 –75 35	—	 –35 75	 mA mA	V_{TXD} = 0V, $t < t_{to(dom)TXD}$, V_{VCC} = 5V - pin CANH, V_{CANH} = –5V - pin CANL, V_{CANL} = +40V
Recessive Output Current	$I_{IO(rec)}$	–5	—	+5	mA	Normal and Silent Mode, $V_{TXD} = V_{VIO}$, no load, $V_{CANH} = V_{CANL}$ = –27V to +32V
Leakage Current	$I_{IO(leak)}$	–5	0	+5	µA	$V_{VCC} = V_{VIO}$ = 0V, $V_{CANH} = V_{CANL}$ = 5V
	$I_{IO(leak)}$	–5	0	+5	µA	VCC = VIO connected to GND with 47kΩ $V_{CANH} = V_{CANL}$ = 5V (**Note 3**)
Input Resistance	R_i	9	15	28	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	R_i	9	15	28	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Input Resistance Deviation	ΔR_i	–1	0	+1	%	Between CANH and CANL $V_{CANH} = V_{CANL}$ = 4V
	ΔR_i	–1	0	+1	%	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Differential Input Resistance	$R_{i(dif)}$	18	30	56	kΩ	$V_{CANH} = V_{CANL}$ = 4V
	$R_{i(dif)}$	18	30	56	kΩ	–2V ≤ V_{CANH} ≤ +7V, –2V ≤ V_{CANL} ≤ +7V (**Note 3**)
Common-Mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	f = 500 kHz, CANH and CANL referred to GND (**Note 3**)
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	f = 500 kHz, between CANH and CANL (**Note 3**)

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C, Grade 0: T_{amb} = –40°C to +150°C, $T_{vJ} \leq 170°C$, V_{VCC}= 4.5V to 5.5V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF, unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Bus Voltage Range for RECESSIVE State Detection	V_{Diff_rec}	–3	—	+0.5	V	Normal and Silent Mode (**Note 3**) –27V ≤ V_{CANH} ≤ +27V, –27V ≤ V_{CANL} ≤ +27V
Differential Bus Voltage Range for DOMINANT State Detection	V_{Diff_dom}	0.9	—	8	V	Normal and Silent Mode (**Note 3**) -27V ≤ V_{CANH} ≤ +27V, -27V ≤ V_{CANL} ≤ +27V
Transceiver Timing, Pins CANH, CANL, TXD, and RXD, see Figure Figure 2-1 and Figure 2-2						
Delay Time from TXD to Bus Dominant	$t_{d(TXD-busdom)}$	40	—	130	ns	Normal Mode (**Note 2**)
Delay Time from TXD to Bus Recessive	$t_{d(TXD-busrec)}$	40	—	130	ns	Normal Mode (**Note 2**)
Delay Time from Bus Dominant to RXD	$t_{d(busdom-RXD)}$	20	—	100	ns	Normal and Silent Mode (**Note 2**)
Delay Time from Bus Recessive to RXD	$t_{d(busrec-RXD)}$	20	—	100	ns	Normal and Silent Mode (**Note 2**)
Propagation Delay from TXD to RXD	$t_{PD(TXD-RXD)}$					Normal Mode R_L = 60Ω, C_L = 100 pF
		40	—	210	ns	Rising Edge at Pin TXD
		40	—	200	ns	Falling Edge at Pin TXD
	$t_{PD(TXD-RXD)}$					Normal Mode R_L = 150Ω, C_L = 100 pF
		—	—	300	ns	Rising Edge at Pin TXD (**Note 3**)
		—	—	300	ns	Falling Edge at Pin TXD (**Note 3**)
TXD Dominant Time-out Time	$t_{to(dom)TXD}$	0.8	—	3	ms	V_{TXD} = 0V, Normal Mode
Delay Time for Normal Mode to Silent Mode Transition	$t_{del(norm-sil)}$	—	—	10	µs	Rising at Pin S (**Note 3**)
Delay Time for Silent Mode to Normal Mode Transition	$t_{del(sil-norm)}$	—	—	10	µs	Falling at Pin S (**Note 3**)
Debouncing Time for Recessive Clamping State Detection	t_{RC_det}	—	90	—	ns	V(CANH-CANL) > 900 mV RXD = HIGH (**Note 3**)
Transceiver Timing for Higher Bit Rates, Pins CANH, CANL, TXD, and RXD, see Figure 2-1 and Figure 2-3, External Capacitor on the RXD Pin CRXD ≤ 20 pF						
Recessive Bit Time on Pin RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal Mode, $t_{Bit(TXD)}$ = 500 ns (**Note 1**) R_L = 60Ω, C_L = 100 pF
	$t_{Bit(RXD)}$	120	—	220	ns	Normal Mode, $t_{Bit(TXD)}$ = 200 ns R_L = 60Ω, C_L = 100 pF
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal Mode, $t_{Bit(TXD)}$ = 500 ns (**Note 1**) R_L = 60Ω, C_L = 100 pF
	$t_{Bit(Bus)}$	155	—	210	ns	Normal Mode, $t_{Bit(TXD)}$ = 200 ns R_L = 60Ω, C_L = 100 pF

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Grade 1: T_{amb} = –40°C to +125°C, Grade 0: T_{amb} = –40°C to +150°C, $T_{vJ} \leq 170°C$, V_{VCC}= 4.5V to 5.5V; V_{VIO} = 2.8V to 5.5V; R_L = 60Ω, C_L = 100 pF, unless otherwise specified. All voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Receiver Timing Symmetry	Δt_{Rec}	–65	—	+40	ns	Normal mode, $t_{Bit(TXD)}$ = 500ns $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ (**Note 1**) R_L = 60Ω, C_L = 100 pF
	Δt_{Rec}	–45	—	+15	ns	Normal mode, $t_{Bit(TXD)}$ = 200ns $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ R_L = 60Ω, C_L = 100 pF

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

TABLE 2-2: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
8-Pin SOIC						
Thermal Resistance Virtual Junction to Ambient	R_{thvJA}	—	145	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6564-GAQW1 (Grade 1)	T_{vJsd}	150	—	195	°C	
Thermal Shutdown of the Bus Drivers for ATA6564-GAQW0 (Grade 0)	T_{vJsd}	170	—	195	°C	
Thermal Shutdown Hysteresis	T_{vJsd_hys}	—	15	—	°C	
8-Pin VDFN						
Thermal Resistance Virtual Junction to Heat Slug	R_{thvJC}	—	10	—	K/W	
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is soldered to PCB according to JEDEC	R_{thvJA}	—	50	—	K/W	
Thermal Shutdown of the Bus Drivers for ATA6564-GBQW1 (Grade 1)	T_{vJsd}	150	—	195	°C	
Thermal Shutdown of the Bus Drivers for ATA6564-GBQW0 (Grade 0)	T_{vJsd}	170	—	195	°C	
Thermal Shutdown Hysteresis	T_{vJsd_hys}	—	15	—	°C	

FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6564 CAN TRANSCEIVER

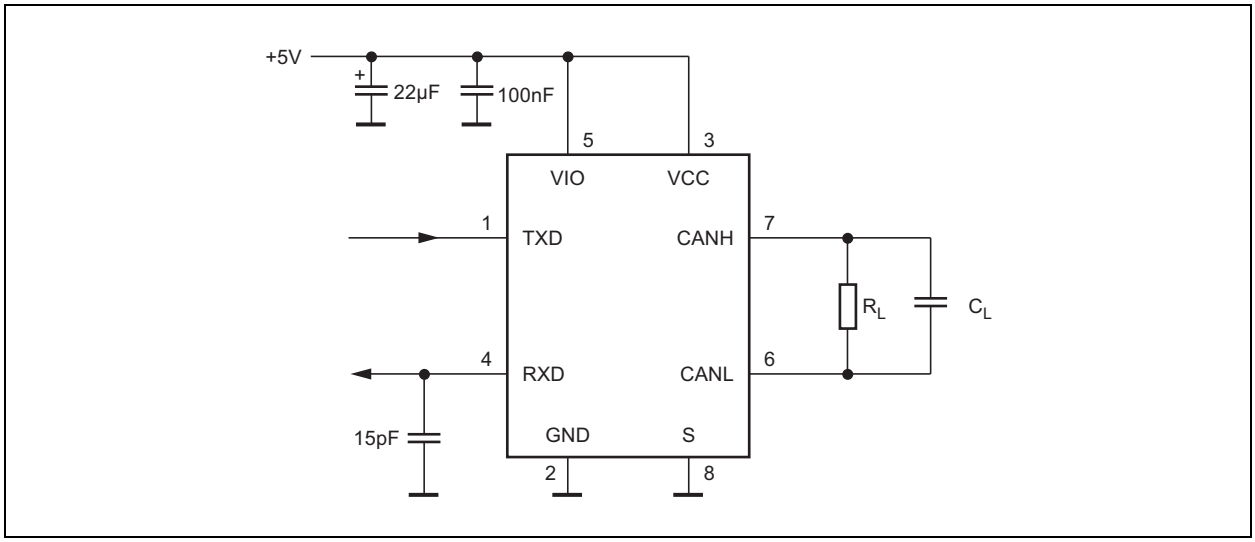


FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1

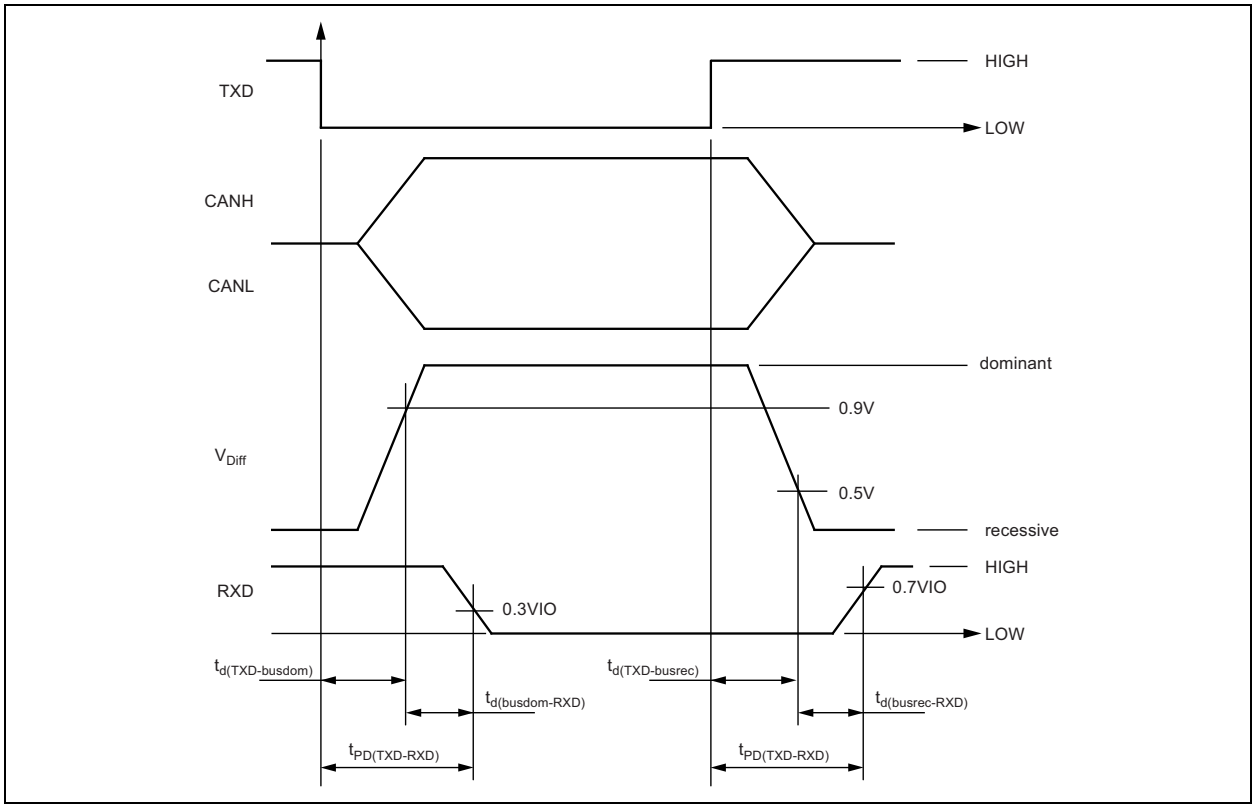
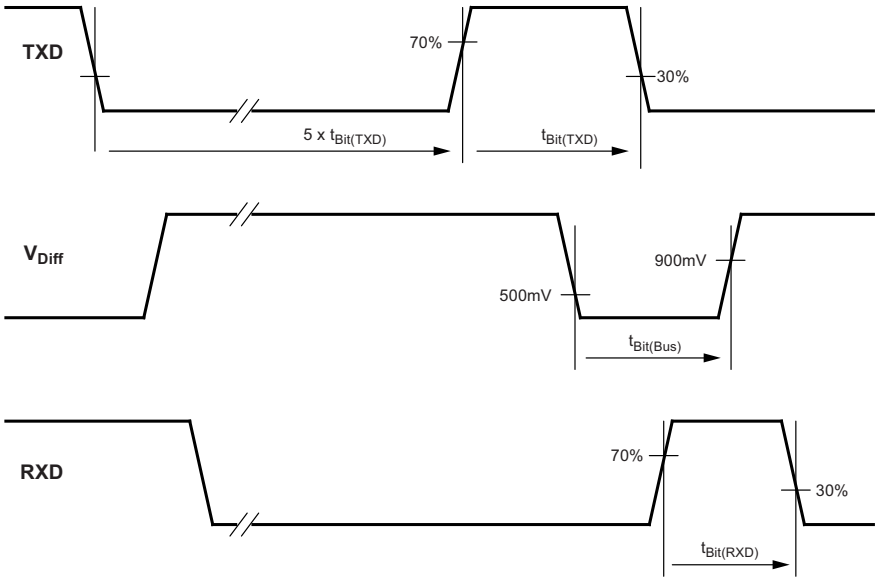


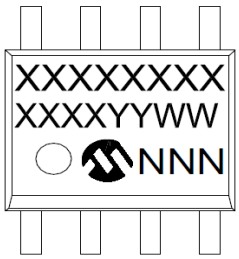
FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2



3.0 PACKAGING INFORMATION

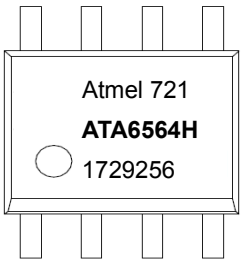
3.1 Package Marking Information

8-Lead SOIC

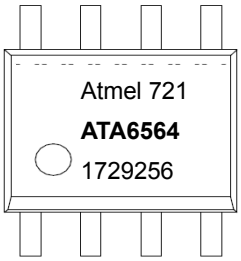


Example

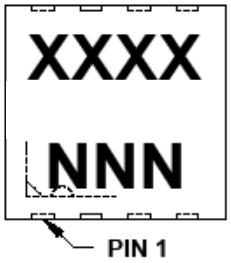
Grade 0



Grade 1

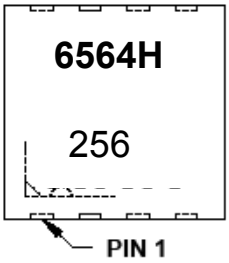


8-Lead VDFN 3 X 3 mm

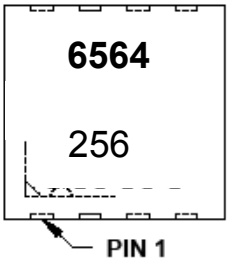


Example

Grade 0



Grade 1

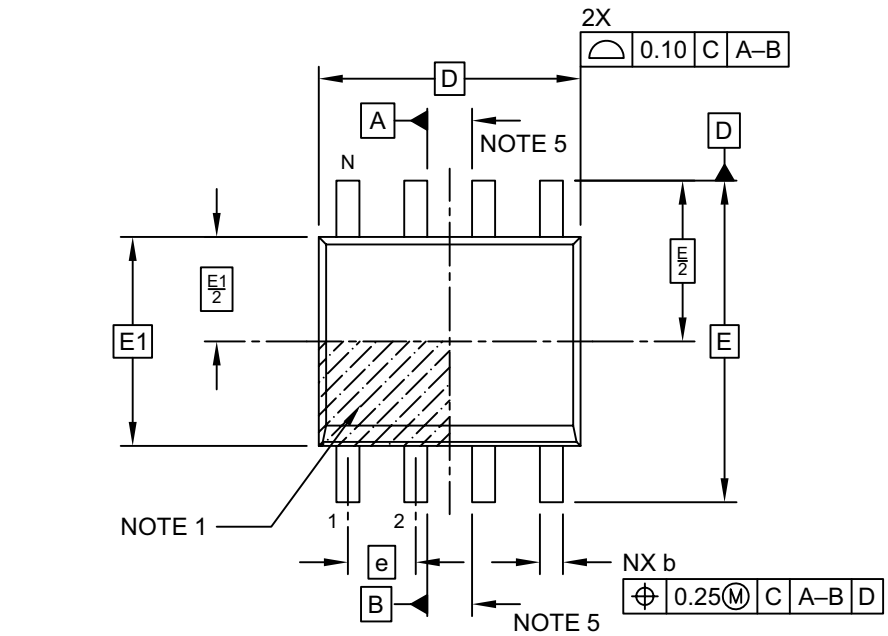


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

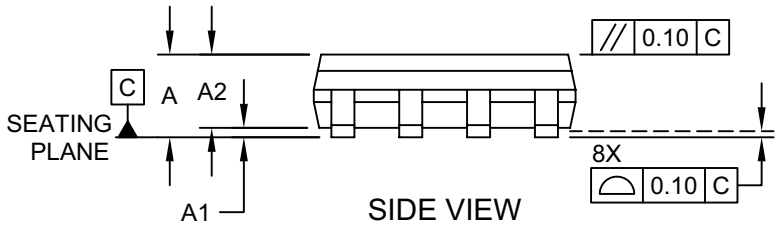
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

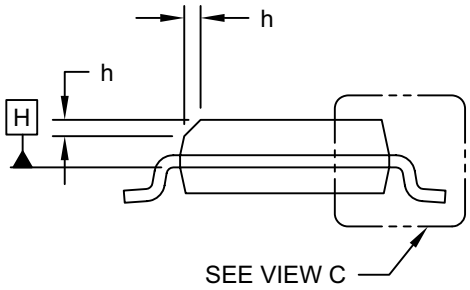
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



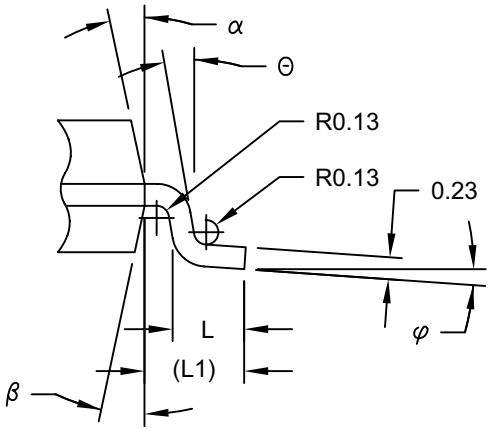
TOP VIEW



SIDE VIEW



VIEW A–A

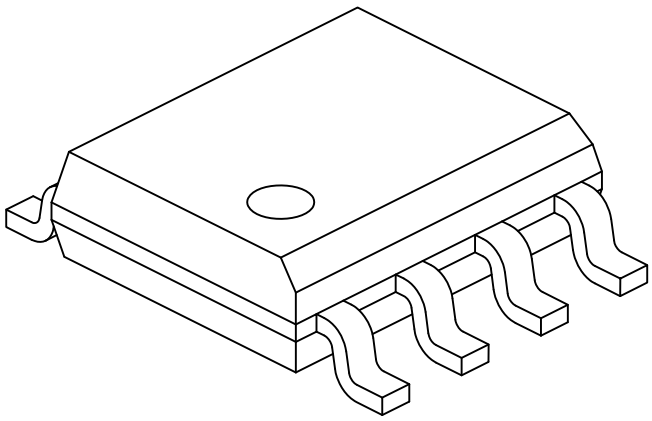


VIEW C

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

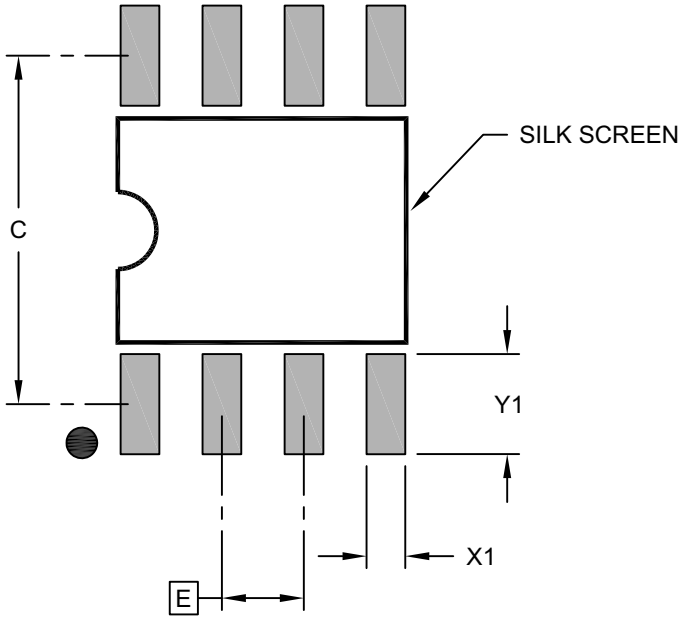
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

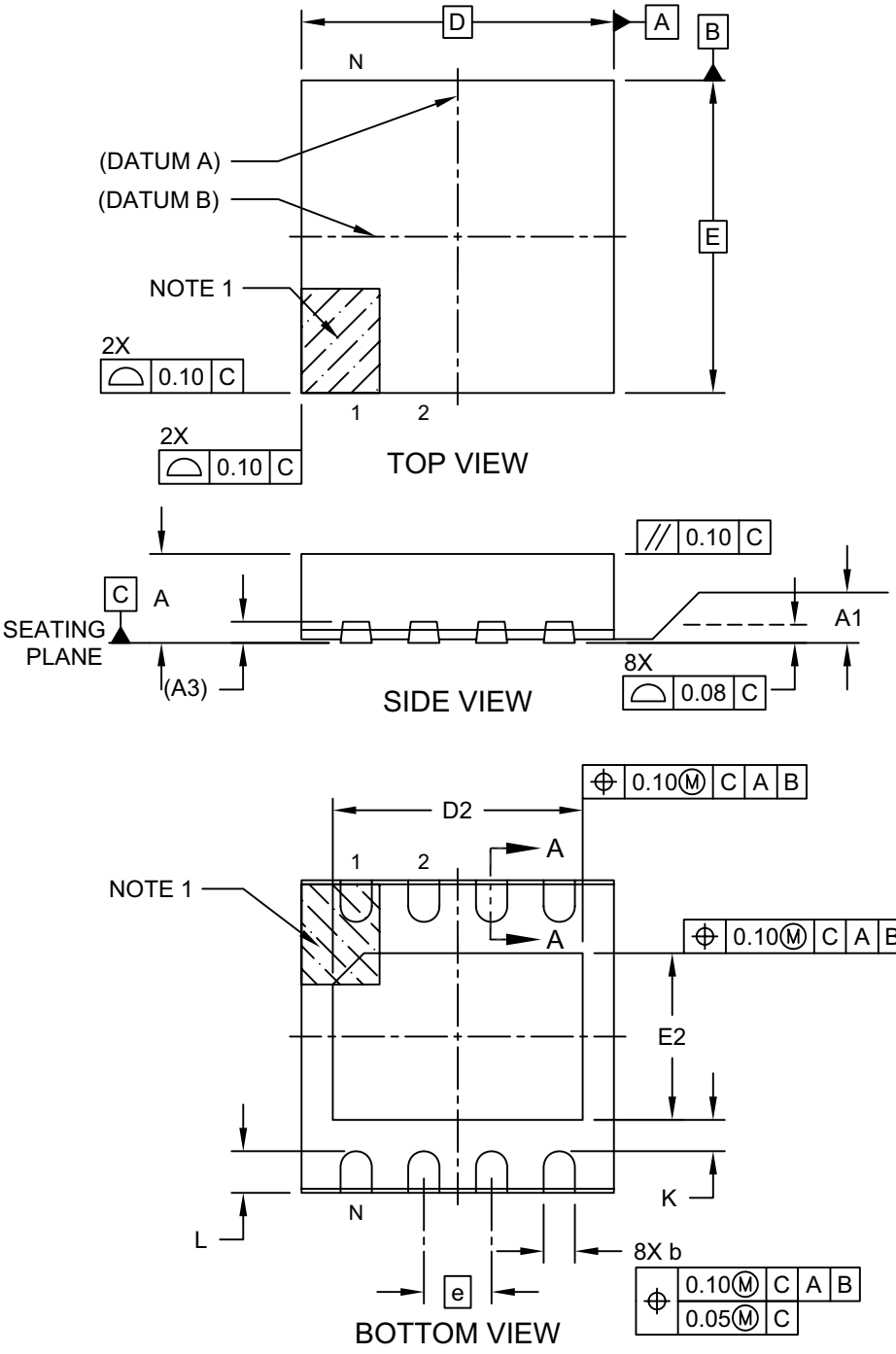
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

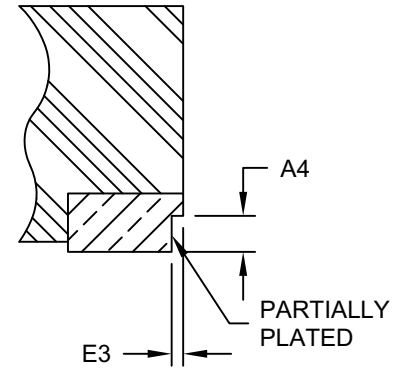
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



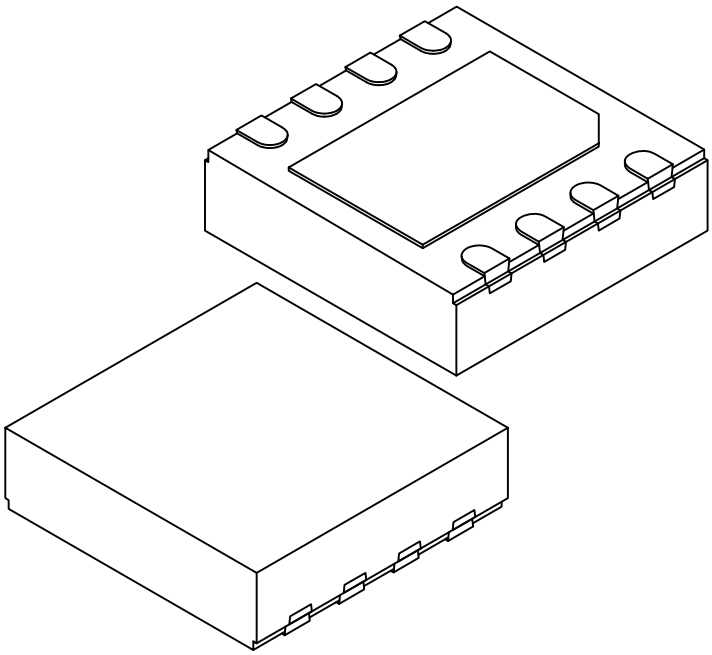
Microchip Technology Drawing C04-21358 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A–A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.30	2.40	2.50
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

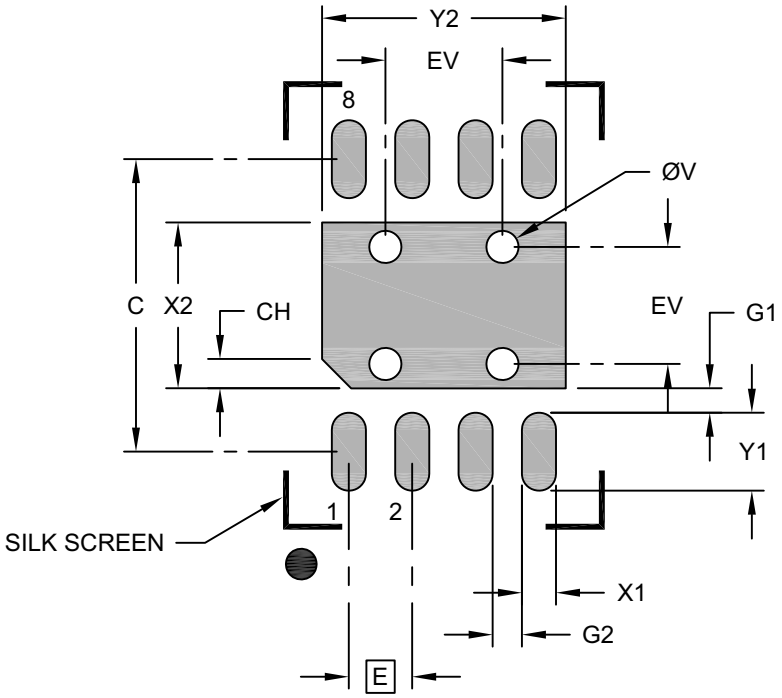
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21358 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (Q8B) - 3x3 mm Body [VDFN] With 2.40x1.60 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			2.50
Contact Pad Spacing	C		3.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Contact Pad to Contact Pad (X6)	G2	0.20		
Pin 1 Index Chamfer	CH	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23358 Rev B

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (August 2019)

The following is the list of modifications:

1. Updated **TABLE 2-2: "Temperature Specifications"**.
2. Added test conditions at several parameters in **TABLE 2-1: "Electrical Characteristics"**.

Revision B (July 2017)

The following is the list of modifications:

3. Added the new device ATA6564-GBQW0 and updated the related information across the document.
4. Updated **ATA6564 Family Members Table**.
5. Corrected **TABLE 2-1: Electrical Characteristics**.
6. Updated **TABLE 2-2: Temperature Specifications**.
7. Updated the VDFN8 package drawing and added a Grade 0 package example to **Section 3.1, Package Marking Information**.
8. Added a ATA6564-GBQW0 example to **"Product Identification System"** section.
9. Various typographical edits.

Revision A (June 2017)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	[X](1)	X	X
Device	Package	Tape and Reel Option	Package directives classification	Temperature Range

Device:	ATA6564:		High-speed CAN Transceiver with Silent Mode CAN FD Ready
Package:	GA GB	= =	8-Lead SOIC 8-Lead VDFN
Tape and Reel Option:	Q	=	330 mm diameter Tape and Reel
Package directives classification:	W	=	Package according to RoHS(2)
Temperature Range:	0 1	= =	Temperature Grade 0 (-40°C to +150°C) Temperature Grade 1 (-40°C to +125°C)

Examples:

a) ATA6564-GAQW0: ATA6564, 8-Lead SOIC, Tape and Reel, package according to RoHS, Temperature Grade 0

b) ATA6564-GBQW0: ATA6564, 8-Lead VDFN, Tape and Reel, package according to RoHS, Temperature Grade 0

c) ATA6564-GAQW1: ATA6564, 8-Lead SOIC, Tape and Reel, package according to RoHS, Temperature Grade 1

d) ATA6564-GBQW1: ATA6564, 8-Lead VDFN, Tape and Reel, package according to RoHS, Temperature Grade 1

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant, Maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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