(16) Digital Input Level: CMOS
(17) Power Supply:
- TVDD= 1.7 ~ 3.6V
- AVDD=3.0 ~ 5.5V
(18) Supporting 105°C Temperature (Exposed pad is connected to ground)
(19) Package: 32-pin QFN

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

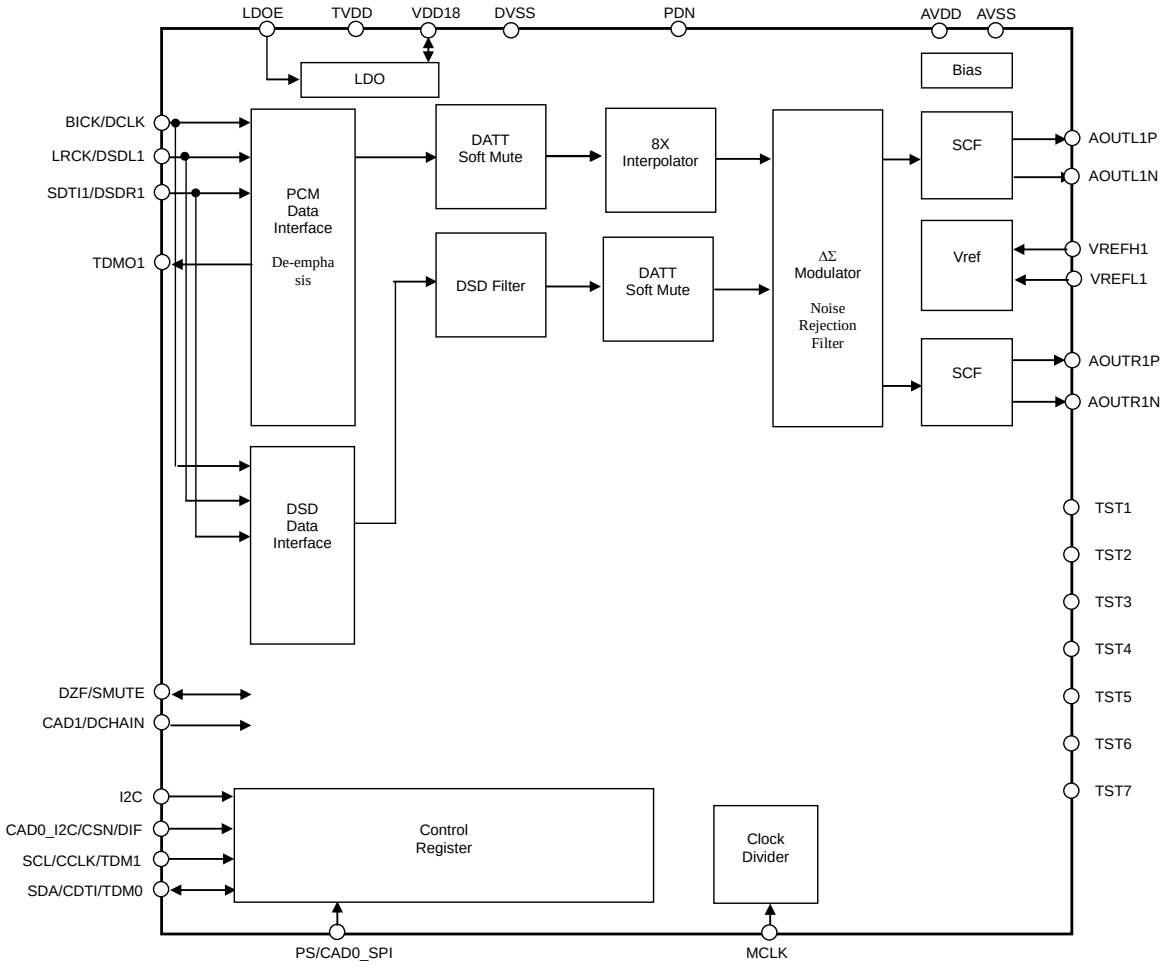


Figure 1. Block Diagram

■ Functions

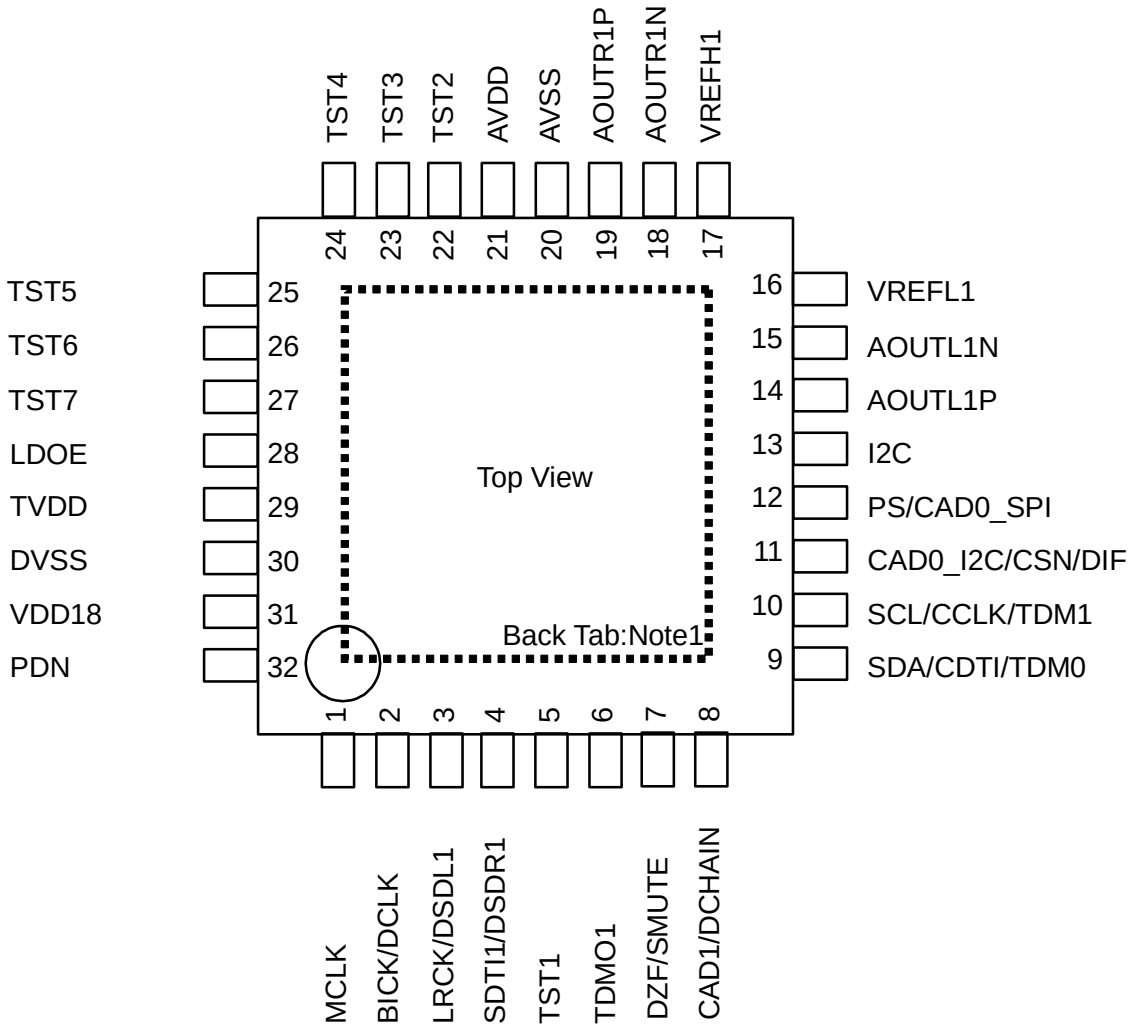
Block	Functions
PCM Data Interface	This block executes serial/parallel conversion of SDTI input audio data by synchronizing with LRCK and BICK.
DSD Data Interface	1-bit data that is input from DSDL1 and DSDR1 pins is received by synchronizing with DCLK.
DATT、Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis	Apply De-emphasis process to input data.
8x Interpolator	FIR filters that over sample 1fs rate data to 8fs rate.
ΔΣ Modulator	Output multi-bit data to SCF. This block consists of a third-order digital delta-sigma modulator.
Noise Rejection Filter	Attenuate out of band noise to prevent degradation of analog characteristics.
SCF	A primary switched capacitor filter that converts a multi-bit output of delta-sigma modulator to an analog signal.
LDO	Generate power for internal digital circuit (1.8V typ.).
Control Register	Keep register settings for each mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.

5. Pin Configurations and Functions

■ Ordering Guide

AK4452VN	–40 ~ +105°C (Exposed pad is connected to ground) –40 ~ +85°C (Exposed pad is open) 32-pin QFN
AKD4452	Evaluation Board for AK4452

■ Pin Configurations



Note 1. The exposed pad at back face of the package must be open or connected to the ground.

■ Pin Functions

No.	Pin Name	I/O	Function	PD Status
1	MCLK	I	External Master Clock Input Pin	Hi-Z
2	BICK	I	Audio Serial Data Clock Pin in PCM mode	Hi-Z
	DCLK	I	DSD Clock Pin in DSD mode	
3	LRCK	I	Input Channel Clock Pin in PCM mode	Hi-Z
	DSDL1	I	Audio Serial Data Input in DSD mode	
4	SDTI1	I	Audio Serial Data Input in PCM mode	Hi-Z
	DSDR1	I	Audio Serial Data Input in DSD mode	
5	TST1	I	Test Pin. This pin must be connected to DVSS	Hi-Z
6	TDMO1	O	Audio Serial Data Output in Daisy Chain mode	100kΩ Pull down
7	DZF	O	Zero Input Detect in I^{2}C Bus or 3-wire serial control mode	100kΩ Pull down
	SMUTE	I	Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases.	
8	CAD1	I	Chip Address 0 Pin in I^{2}C Bus or 3-wire serial control mode	Hi-Z
	DCHAIN	I	Daisy Chain Mode select pin in Parallel control mode.	
9	SDA	I/O	Control Data Input Pin in I^{2}C Bus serial control mode	Hi-Z
	CDTI	I	Control Data Input Pin in 3-wire serial control mode	
	TDM0	I	TDM Mode select pin in Parallel control mode.	
10	SCL	I	Control Data Clock Pin in I^{2}C Bus serial control mode	Hi-Z
	CCLK	I	Control Data Clock Pin in 3-wire serial control mode	
	TDM1	I	TDM Mode select pin in Parallel control mode.	
11	CAD0_I2C	I	Chip Address 0 Pin in I^{2}C Bus serial control mode	Hi-Z
	CSN	I	Chip Select Pin in 3-wire serial control mode	
	DIF	I	Audio Data Format Select in Parallel control mode. "L" : 32-bit MSB, "H" : 32-bit I^{2}S	
12	PS	I	(I2C pin = "H") Control Mode Select Pin "L": I^{2}C Bus serial control mode ,"H": Parallel control mode.	Hi-Z
	CAD0_SPI	I	(I2C pin = "L") Chip Address 0 Pin in 3-wire serial control mode	
13	I2C	I	Control Mode Select Pin "L": 3-wire serial control mode "H": I^{2}C Bus serial control mode or Parallel control mode.	Hi-Z
14	AOUTL1P	O	L ch Positive Analog Output 1 Pin	Hi-Z
15	AOUTL1N	O	L ch Negative Analog Output 1 Pin	Hi-Z
16	VREFL1	I	Negative Voltage Reference Input Pin, AVSS	Hi-Z
17	VREFH1	I	Positive Voltage Reference Input Pin, AVDD	Hi-Z
18	AOUTR1N	O	R ch Negative Analog Output 1 Pin	Hi-Z
19	AOUTR1P	O	R ch Positive Analog Output 1 Pin	Hi-Z
20	AVSS	-	Analog Ground Pin	—
21	AVDD	-	Analog Power Supply Pin, 3.0V~5.5V	—
22	TST2	I	Test Pin. This pin must be connected to AVSS.	Hi-Z
23	TST3	I	Test Pin. This pin must be connected to AVSS.	Hi-Z
24	TST4	I	Test Pin. This pin must be connected to AVSS.	Hi-Z
25	TST5	I	Test Pin. This pin must be connected to AVSS.	Hi-Z

No.	Pin Name	I/O	Function	PD Status
26	TST6	I	Test Pin. This pin must be connected to AVSS.	Hi-Z
27	TST7	I	Test Pin. This pin must be connected to AVSS.	Hi-Z
28	LDOE	I	Internal LDO Enable Pin. "L": Disable, "H": Enable	Hi-Z
29	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V	—
30	DVSS	-	Digital Ground Pin	—
31	VDD18	O	(LDOE pin = "H") LDO Output Pin This pin should be connected to DVSS with 1.0µF.	(Note 4)
		I	(LDOE pin = "L") 1.8V Power Input Pin	
32	PDN	I	Power-Down & Reset Pin When "L", the AK4452 is powered-down and the control registers are reset to default state.	Hi-Z

Note 2. All input pins except internal pull-up/down pins must not be allowed to float.
Note 3. PCM mode and DSD mode are controlled by registers. Daisy Chain mode is controlled by both registers and pins.
Note 4. This pin outputs DVSS when the LDOE pin = "H" and Hi-z when the LDOE pin = "L".

■ Handling of Unused Pin

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	AOUTL1P/N, AOUTR1P/N	These pins must be open.
Digital	TDMO1, DZF	This pin must be open.

6. Absolute Maximum Ratings

(AVSS =DVSS =0V; Note 5)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	TVDD	–0.3	4.0	V
	|AVSS – DVSS|	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (Power applied)					
When the back tab is connected to VSS		Ta	–40	105	°C
When the back tab is open		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 5. All voltages with respect to ground.
Note 6. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS =DVSS =0V; Note 5)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (LDOE pin= "L") (Note 7)	AVDD	3.0	5.0	5.5	V
	I/O buffer	TVDD	VDD18	1.8	3.6	V
	Digital (LDOE pin = "H")(Note 8)	VDD18	1.7	1.8	1.98	V
	I/O buffer	TVDD	3.0	3.3	3.6	V
Voltage Reference	"H" voltage reference	VREFH1	AVDD–0.5	-	AVDD	V
	"L" voltage reference	VREFL1	-	AVSS	-	V

Note 7. When the LDOE pin = "L" VDD18 must be powered up either at the same time or after TVDD is powered up. The power up sequence between AVDD and TVDD or AVDD and VDD18 is not critical.
Note 8. When LDOE pin = "H", the internal LDO supplies 1.8V (typ). The power up sequences between AVDD and TVDD, AVDD and VDD18 are not critical.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Electrical Characteristics

■ Analog Characteristics

(1) AVDD = 5.0V

(Ta=25°C: TVDD=3.3V, AVDD=5.0V: AVSS= DVSS=0V: VREFH1=AVDD, VREFL1= AVSS: fs=44.1kHz: BICK=64fs: Signal Frequency=1kHz: 24-bit Input Data: $R_L \geq 2k\Omega$: measurement bandwidth = 20Hz ~ 20kHz: External Circuit: (Figure 80), unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution			-	-	32	bit
Dynamic Characteristics (Note 9)						
THD+N	fs=44.1kHz	0dBFS	-	-107	-100	dB
	BW=20kHz	–60dBFS	-	-52	-	dB
	fs=96kHz	0dBFS	-	-104	-	dB
	BW=40kHz	–60dBFS	-	-48	-	dB
	fs=192kHz	0dBFS		-104	-	dB
	BW=40kHz	–60dBFS		-48	-	dB
	BW=80kHz	–60dBFS		-44	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 10)			110	115	-	dB
S/N (A-weighted) (Note 11)			110	115	-	dB
Interchannel Isolation (1kHz)			100	110	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0	0.3	dB
Gain Drift (Note 12)			-	20	-	ppm/°C
Output Voltage (Note 13)			±2.65	±2.8	±2.95	Vpp
Load Resistance (Note 14)			2	-	-	kΩ
Load Capacitance (Note 14)			-	-	30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")						
AVDD			-	8	11	mA
TVDD (fs = 44.1kHz)			-	3	4	mA
TVDD (fs = 96kHz)			-	5	7	mA
TVDD (fs = 192kHz)			-	7	10	mA
Power down (PDN pin = "L") (Note 15)						
AVDD+TVDD			-	1	100	μA

(2) AVDD = 3.3V

(Ta=25°C: TVDD=3.3V, AVDD=3.3V: AVSS= DVSS=0V: VREFH1=AVDD, VREFL1= AVSS: fs=44.1kHz: BICK=64fs: Signal Frequency=1kHz: 24-bit Input Data: $R_L \geq 2k\Omega$: measurement bandwidth = 20Hz ~ 20kHz: External Circuit: (Figure 80), unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Resolution					32	bit
Dynamic Characteristics		(Note 9)				
THD+N	fs=44.1kHz	0dBFS	-	-93	-86	dB
	BW=20kHz	–60dBFS	-	-48	-	dB
	fs=96kHz	0dBFS	-	-92	-	dB
	BW=40kHz	–60dBFS	-	-45	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	–60dBFS		-45	-	dB
	BW=80kHz	–60dBFS		-41	-	dB
Dynamic Range(–60dBFS with A-weighted)		(Note 10)	106	111	-	dB
S/N (A-weighted)		(Note 11)	106	111	-	dB
Inter channel Isolation (1kHz)			100	110	-	dB
DC Accuracy						
Inter channel Gain Mismatch				0	0.3	dB
Gain Drift		(Note 12)	-	20	-	ppm/°C
Output Voltage		(Note 13)	±1.66	±1.85	±2.04	Vpp
Load Resistance		(Note 14)	2			kΩ
Load Capacitance		(Note 14)			30	pF
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")						
AVDD			-	6	-	mA
TVDD (fs = 44.1kHz)			-	3	-	mA
TVDD (fs = 96kHz)			-	5	-	mA
TVDD (fs = 192kHz)			-	7	-	mA
Power down (PDN pin = "L")		(Note 15)				
AVDD+TVDD				1	100	μA

Note 9. Measured by Audio Precision, System Two. Averaging mode.

Note 10. Figure 80 External LPF Circuit Example 1. 100dB for 16-bit data.

Note 11. Figure 80 External LPF Circuit Example 1. S/N does not depend on input data size.

Note 12. The voltage on (VREFH1 – VREFL1) is held +5V externally.

Note 13. The full scale voltage when applying a 1kHz sine wave (0dB) in PCM mode, or when applying a 1kHz sine wave (25~75% duty) in DSD mode. Output voltage scales with the voltage of (VREFH1 – VREFL1).

DAC: AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFH1 – VREFL1)/5

Note 14. Regarding Load Resistance, AC load is 2kΩ (min) with a DC cut capacitor (Figure 80). DC load is 2 kΩ (min) without a DC cut capacitor (Figure 80). The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore the capacitive load must be minimized.

Note 15. In the power down mode. All other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.

■ Sharp Roll-Off Filter Characteristics

Sharp Roll-Off Filter Characteristics **(fs= 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF, SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Pass band Ripple		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	24.1			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	26.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		20.0	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 20.0kHz			-0.2		0.1	dB

Sharp Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF, SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Pass band Ripple		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	52.5			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	26.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		43.5	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 40.0kHz			-0.3		0.1	dB

Sharp Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF, SLOW bit = "0", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Pass band Ripple		PR	-0.0032		0.0032	dB
Stop band (Note 16)		SB	105			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	26.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		87.0	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 80.0kHz			-1		0.1	dB

Note 16. The pass band and stop band frequencies scale with fs. For example, PB=0.4535×fs, SB=0.546×fs.
Note 17. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24/32bit data of both channels to input register to the output of analog signal.
Note 18. The output level is assumed as 0dB when inputting a 1kHz 0dB sine wave.
*Digital filter characteristics are based on simulation results.

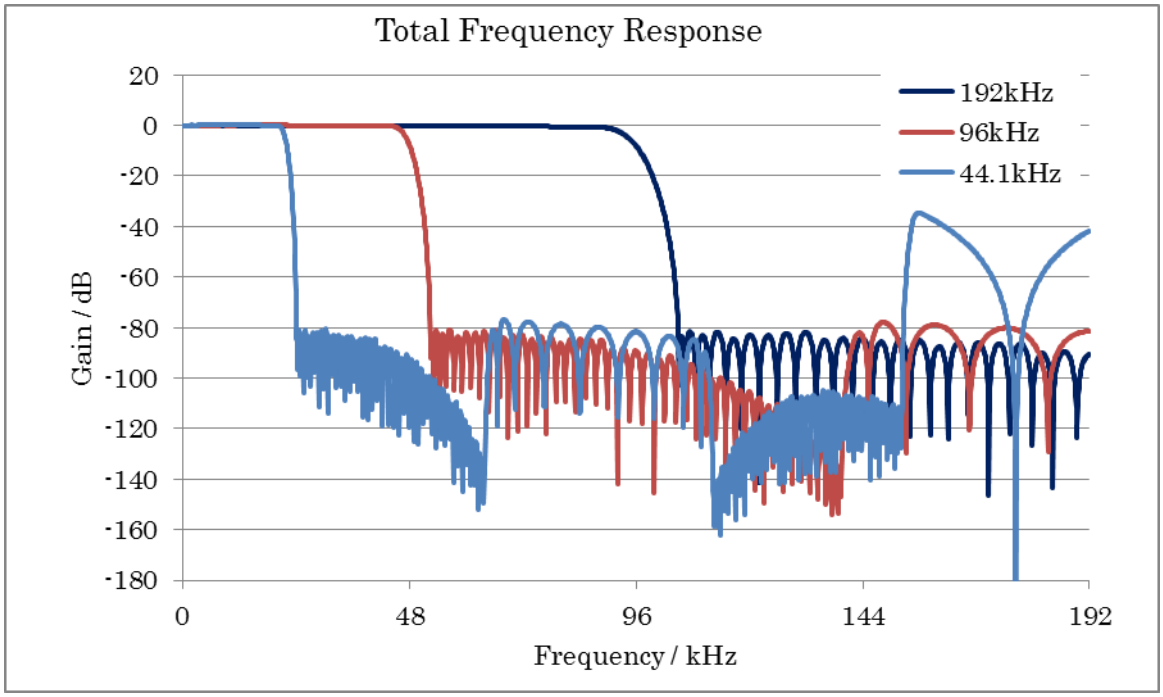


Figure 2. Sharp Roll-off Filter Frequency Response

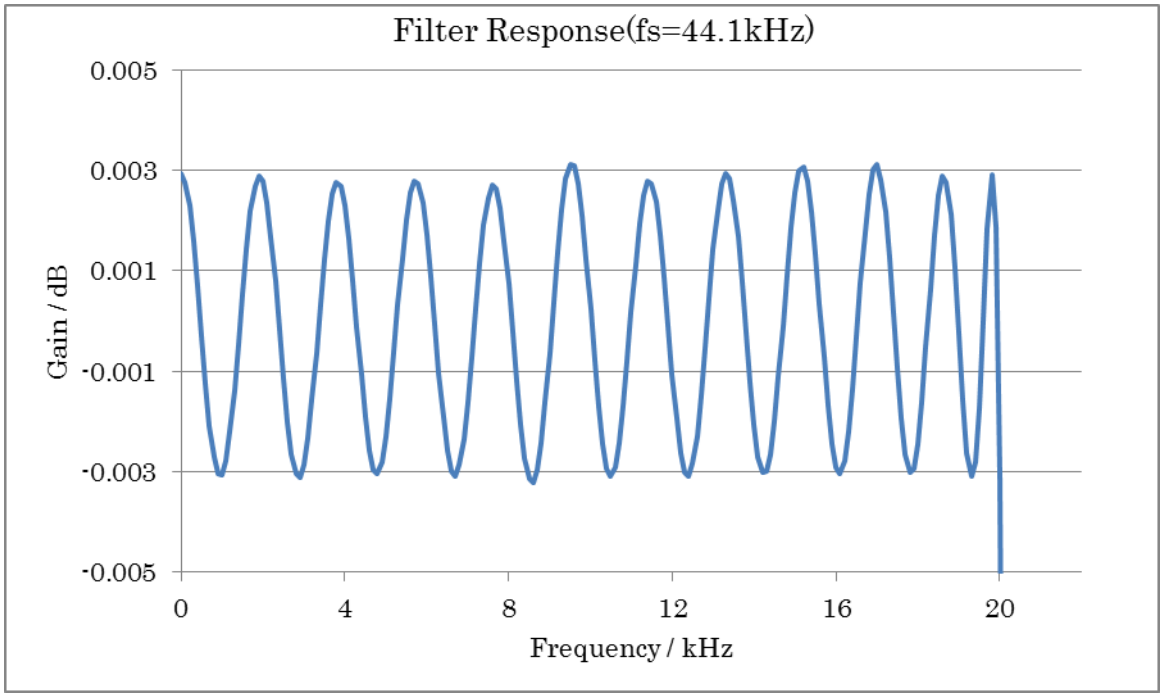


Figure 3. Sharp Roll-off Filter Passband Ripple

■ Slow Roll-Off Filter Characteristics

Slow Roll-Off Filter Characteristics **(fs = 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 19)	±0.05dB	PB	0		8.1	kHz
	−3.0dB	PB		18.2		kHz
Pass band Ripple		PR	-0.043		0.043	dB
Stop band (Note 19)		SB	39.2			kHz
Stop band Attenuation (Note 18)		SA	73			dB
Group Delay (Note 17)		GD	-	6.3	-	1/fs
Frequency Response (Note 18)	±0.05dB	-	0		8.1	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 20.0kHz			-5		0.1	dB

Slow Roll-Off Filter Characteristics **(fs = 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 19)	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Pass band Ripple		PR	-0.043		0.043	dB
Stop band (Note 19)		SB	85.3			kHz
Stop band Attenuation (Note 18)		SA	73			dB
Group Delay (Note 17)		GD	-	6.3	-	1/fs
Frequency Response (Note 18)	±0.05dB	PB	0		17.7	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 40.0kHz			-5		0.1	dB

Slow Roll-Off Filter Characteristics **(fs = 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="0")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 19)	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Pass band Ripple		PR	-0.043		0.043	dB
Stop band (Note 19)		SB	171			kHz
Stop band Attenuation (Note 18)		SA	73			dB
Group Delay (Note 17)		GD	-	6.3	-	1/fs
Frequency Response (Note 18)	±0.05dB	PB	0		35.5	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 80.0kHz			-5		0.1	dB

Note 19. The pass band and stop band frequencies scale with fs. For example, PB=0.185×fs, SB=0.888×fs.

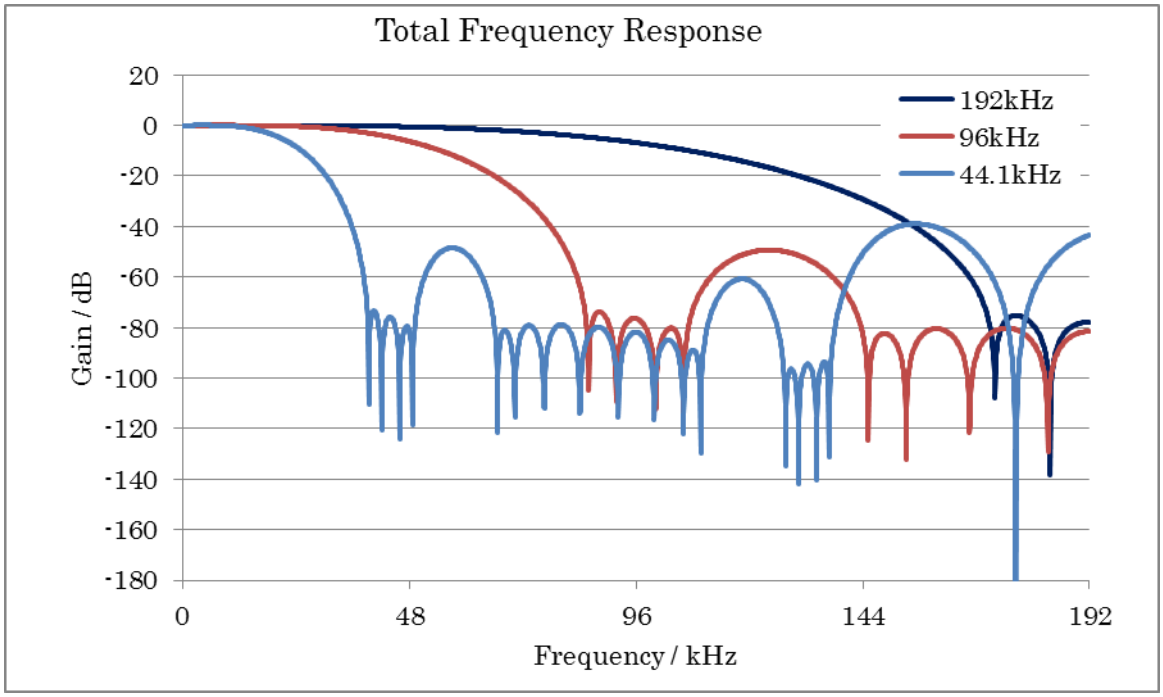


Figure 4. Slow Roll-off Filter Frequency Response

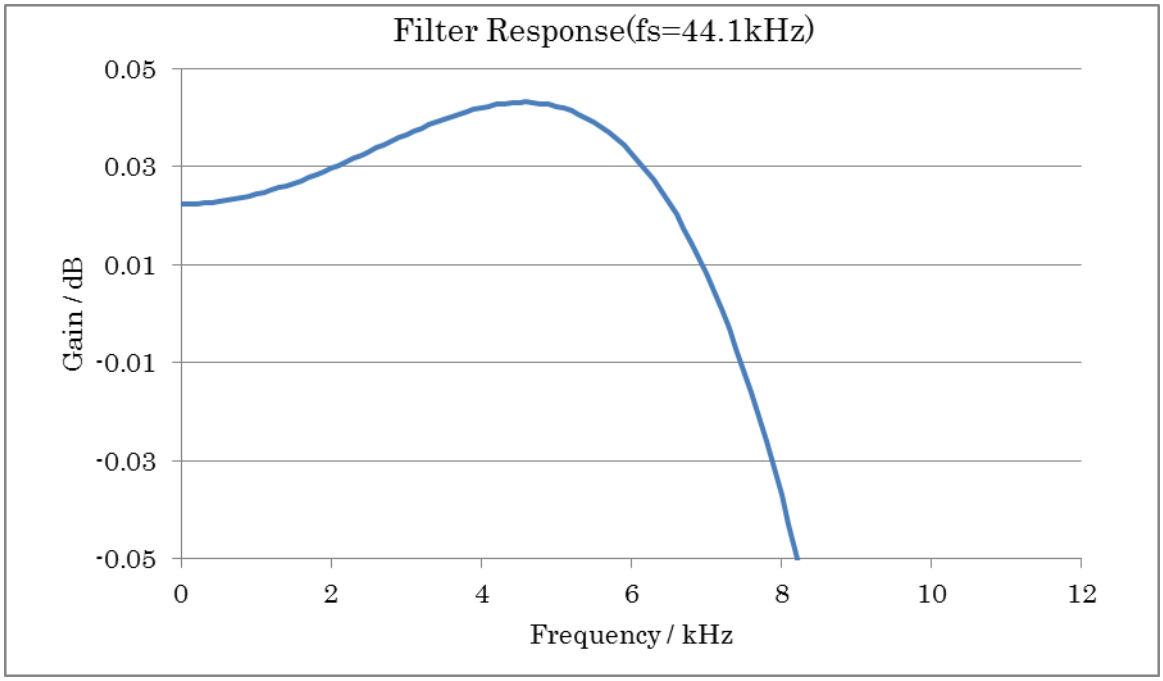


Figure 5. Slow Roll-off Filter Passband Ripple

■ Short Delay Sharp Roll-Off Filter Characteristics

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		20.0	kHz
	−3.0dB	PB		21.5		kHz
Pass band Ripple		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	24.1			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		20.0	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 20.0kHz			-0.2		0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Pass band Ripple		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	52.5			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		43.5	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 40.0kHz			-0.3		0.1	dB

Short Delay Sharp Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "0", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 16)	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Pass band Ripple		PR	-0.0031		0.0031	dB
Stop band (Note 16)		SB	105			kHz
Stop band Attenuation (Note 18)		SA	80			dB
Group Delay (Note 17)		GD	-	5.8	-	1/fs
Frequency Response (Note 18)	±0.07dB	-	0		87.0	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 80.0kHz			-1		0.1	dB

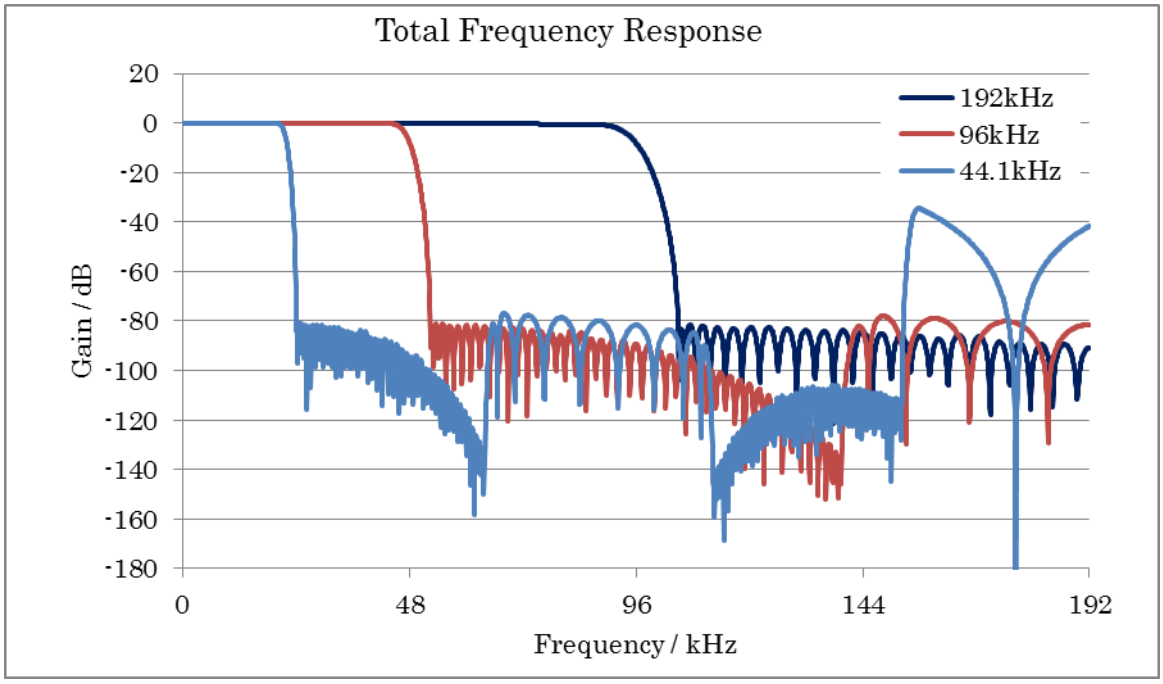


Figure 6. Short delay Sharp Roll-off Filter Frequency Response

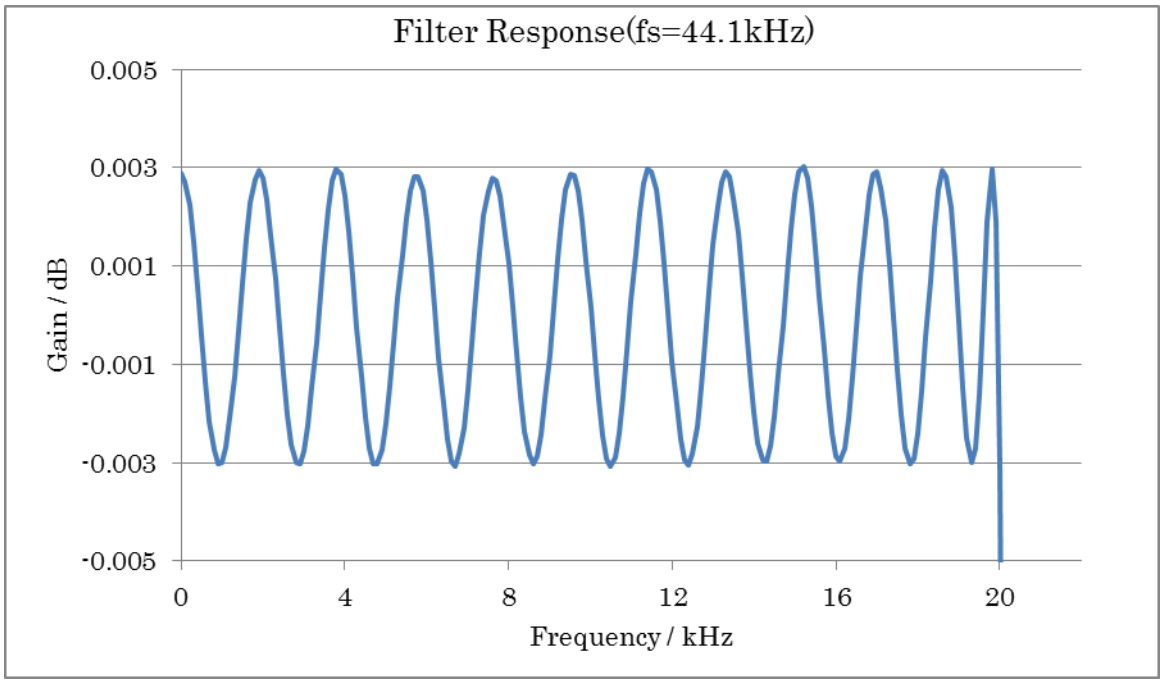


Figure 7. Short delay Sharp Roll-off Filter Passband Ripple

■ Short Delay Slow Roll-Off Filter Characteristics

Short Delay Slow Roll-Off Filter Characteristics **(fs= 44.1kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Normal Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		11.1	kHz
	–3.0dB	PB		19.4		kHz
Pass band Ripple		PR	-0.05		0.05	dB
Stop band (Note 20)		SB	38.1			kHz
Stop band Attenuation (Note 18)		SA	82			dB
Group Delay (Note 17)		GD	-	4.8	-	1/fs
Frequency Response (Note 18)	±0.05dB	-	0		11.1	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 20.0kHz			-5		0.1	dB

Short Delay Slow Roll-Off Filter Characteristics **(fs= 96kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Double Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		24.2	kHz
	–3.0dB	PB		42.1		kHz
Pass band Ripple		PR	-0.05		0.05	dB
Stop band (Note 20)		SB	83.0			kHz
Stop band Attenuation (Note 18)		SA	82			dB
Group Delay (Note 17)		GD	-	4.8	-	1/fs
Frequency Response (Note 18)	±0.05dB	-	0		24.2	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 40.0kHz			-5		0.1	dB

Short Delay Slow Roll-Off Filter Characteristics **(fs= 192kHz)**
(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V; Quad Speed Mode; DEM=OFF; SLOW bit = "1", SD bit="1")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter						
Pass band (Note 20)	±0.05dB	PB	0		48.4	kHz
	–3.0dB	PB		84.3		kHz
Pass band Ripple		PR	-0.05		0.05	dB
Stop band (Note 20)		SB	165.9			kHz
Stop band Attenuation (Note 18)		SA	82			dB
Group Delay (Note 17)		GD	-	4.8	-	1/fs
Frequency Response (Note 18)	±0.05dB	-	0		48.4	kHz
Digital Filter + SCF (Note 18)						
Frequency Response: 0 ~ 80.0kHz			-5		0.1	dB

Note 20. The pass band and stop band frequencies scale with fs. For example, PB=0.252×fs, SB=0.864×fs.

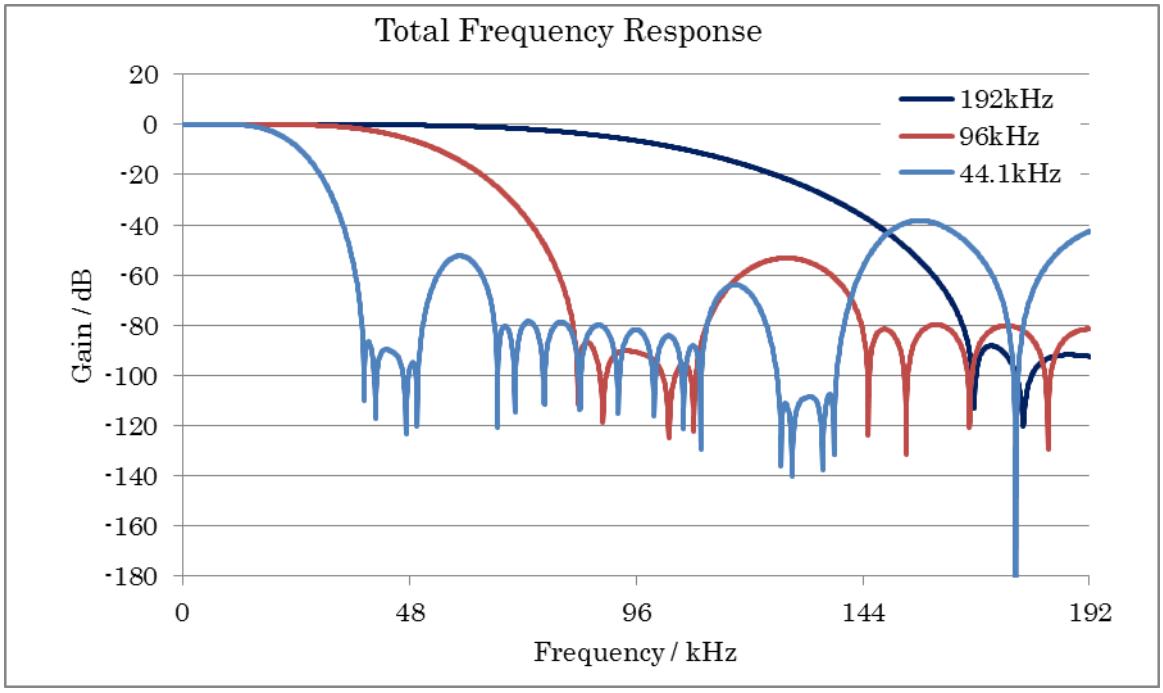


Figure 8. Short Delay Slow Roll-off Filter Frequency Response

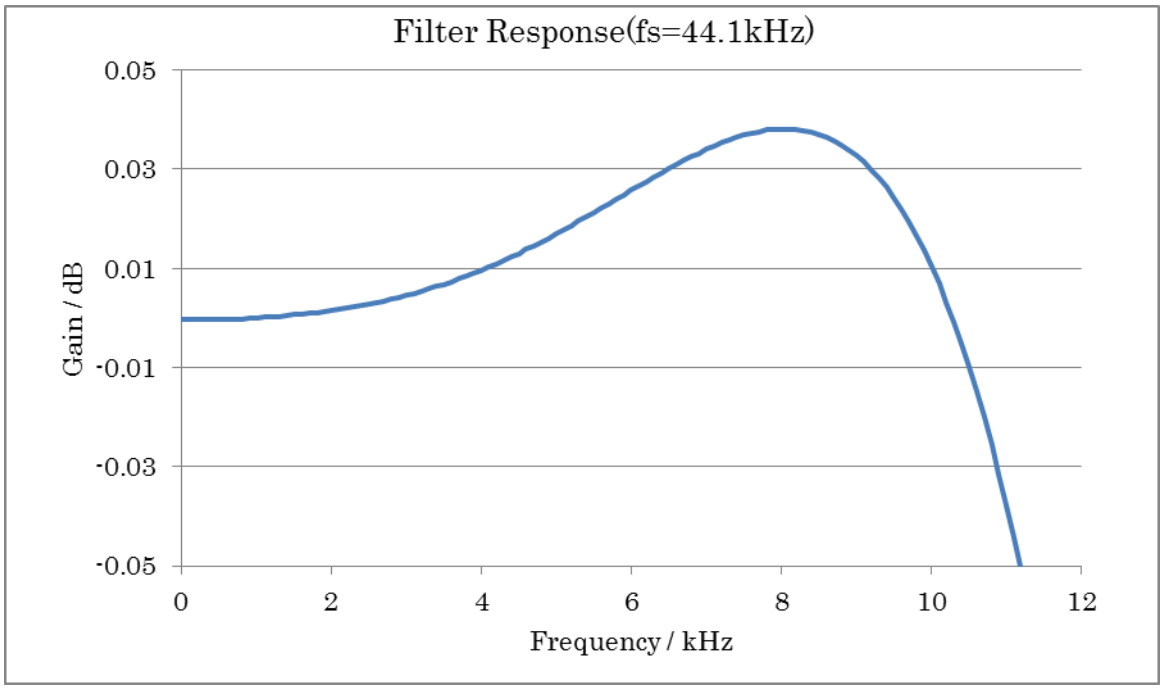


Figure 9. Short Delay Slow Roll-off Filter Passband Ripple

■ DSD Mode Characteristics

(1) DSDF bit= "0"

(Ta=-40 ~ 105°C: AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V: fs=44.1kHz: D/P bit= "1", DSDF bit= "0")

Parameter			Min.	Typ.	Max.	Unit
Digital Filter Response						
Frequency Response (Note 21)	DSDSEL[1:0]					
	"00"	20kHz 50kHz 100kHz		-0.8 -5.5 -19.9		dB
	"01""	40kHz 200kHz 400kHz		-0.8 -5.5 -19.9		dB
	"10"	80kHz 400kHz 800kHz		-0.8 -5.5 -19.9		dB

(2) DSDF bit= "1"

(Ta=-40 ~ 105°C: AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V: fs=44.1kHz: D/P bit="1", DSDF bit= "1")

Parameter			Min.	Typ.	Max.	Unit
Digital Filter Response						
Frequency Response (Note 21)	DSDSEL[1:0]					
	"00"	20kHz 100kHz 200kHz		-0.2 -6.3 -23.7		dB
	"01""	40kHz 200kHz 400kHz		-0.2 -6.3 -23.7		dB
	"10"	80kHz 400kHz 800kHz		-0.2 -6.3 -23.7		dB

Note 21. In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

Note 22. It is assumed that the output level is 0dB when the input signal is 1kHz and the duty range is between 25 ~ 75%.The output level is assumed as 0dB when applying a 1kHz sine wave in 25~ 75% duty.

*Digital filter characteristics are based on simulation results.

■ DC Characteristics

(Ta=-40 ~ 105°C; AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
TVDD=1.7 ~ 3.0V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
TVDD=3.0V ~ 3.6V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
High-Level Output Voltage (TDMO1, DZF pins: Iout=-100µA)	VOH	TVDD–0.5	-	-	V
Low-Level Output Voltage					
(excpt SDA pin : Iout= 100µA)	VOL	-	-	0.5	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.7V ≤ TVDD ≤ 2.0V: Iout= 3mA)	VOL	-		20%TVDD	V
Input Leakage Current	Iin	-	-	±10	µA

■ Switching Characteristics

(Ta=-40 ~ 105°C: AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V, C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
Frequency	fCLK	2.048		49.152	MHz
Duty Cycle	dCLK	45		55	%
Minimum Pulse Width	tCLKH	9.155			ns
	tCLKL	9.155			ns
LRCK Frequency (Note 23)					
Normal Mode (TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
Oct speed mode	fso		384		kHz
Hex speed mode	fsh		768		kHz
Duty Cycle	Duty	45		55	%
TDM128 mode (TDM1-0 bits = "01")					
Normal Speed Mode	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
Quad Speed Mode	fsq	108		216	kHz
High time	tLRH	1/128fs			nsec
Low time	tLRL	1/128fs			ns
TDM256 mode (TDM1-0 bits = "10")					
Normal Speed Mode High time	fsn	8		54	kHz
Double Speed Mode	fsd	54		108	kHz
High time	tLRH	1/256fs			nsec
Low time	tLRL	1/256fs			nsec
TDM512 mode (TDM1-0 bits = "11")					
Normal Speed Mode	fsn	8		54	kHz
High time	tLRH	1/512fs			nsec
Low time	tLRL	1/512fs			nsec
PCM Audio Interface Timing					
Normal Mode (TDM1-0 bits = "00")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			nsec
Double Speed Mode	tBCK	1/128fsd			nsec
Quad Speed Mode	tBCK	1/64fsq			nsec
Oct speed mode	tBCK	1/64fso			nsec
Hex speed mode	tBCK	1/64fsh			nsec
BICK Pulse Width Low	tBCKL	9			nsec
BICK Pulse Width High	tBCKH	9			nsec
BICK "↑" to LRCK Edge (Note 24)	tBLR	5			nsec
LRCK Edge to BICK "↑" (Note 24)	tLRB	5			nsec
SDTI1 Hold Time	tSDH	5			nsec
SDTI1 Setup Time	tSDS	5			nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
TDM128 mode (TDM1-0 bits = "01")					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			nsec
Double Speed Mode	tBCK	1/128fsd			nsec
Quad Speed Mode	tBCK	1/128fsq			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 24)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 24)	tLRB	14			nsec
SDTI1 Hold Time	tSDH	5			nsec
SDTI1 Setup Time	tSDS	5			nsec
TDM256 mode (TDM1-0 bits = "10")					
BICK Period					
Normal Speed Mode	tBCK	1/256fsn			nsec
Double Speed Mode (Note 25)	tBCK	1/256fsd			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 24)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 24)	tLRB	14			nsec
TDMO1 Setup time BICK "↑"	tBSS	5			nsec
TDMO1 Hold time BICK "↑"(Note 27)	tBSH	5			nsec
SDTI1 Hold Time	tSDH	5			nsec
SDTI1 Setup Time	tSDS	5			nsec
TDM512 mode (TDM1-0 bits = "11")					
BICK Period					
Normal Speed Mode (Note 26)	tBCK	1/512fsn			nsec
BICK Pulse Width Low	tBCKL	14			nsec
BICK Pulse Width High	tBCKH	14			nsec
BICK "↑" to LRCK Edge (Note 24)	tBLR	14			nsec
LRCK Edge to BICK "↑" (Note 24)	tLRB	14			nsec
TDMO1 Setup time BICK "↑"	tBSS	5			nsec
TDMO1 Hold time BICK "↑" (Note 27)	tBSH	5			nsec
SDTI1 Hold Time	tSDH	5			nsec
SDTI1 Setup Time	tSDS	5			nsec

Parameter	Symbol	Min.	Typ.	Max.	Unit
DSD Audio Interface Timing					
(64 mode, DSDSEL 1-0 bits = "00")					
DCLK Period	tDCK		1/64fs		nsec
DCLK Pulse Width Low	tDCKL	144			nsec
DCLK Pulse Width High	tDCKH	144			nsec
DCLK Edge to DSDL/R (Note 28)	tDDD	–20		20	nsec
(128 mode, DSDSEL 1-0 bits = "01")					
DCLK Period	tDCK		1/128fs		nsec
DCLK Pulse Width Low	tDCKL	72			nsec
DCLK Pulse Width High	tDCKH	72			nsec
DCLK Edge to DSDL/R (Note 28)	tDDD	–10		10	nsec
(256 mode, DSDSEL 1-0 bits = "10")					
DCLK Period	tDCK		1/256fs		nsec
DCLK Pulse Width Low	tDCKL	36			nsec
DCLK Pulse Width High	tDCKH	36			nsec
DCLK Edge to DSDL/R (Note 28)	tDDD	–5		5	nsec

Note 23. When the 1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK4452 should be reset by the PDN pin or RSTN bit.

Note 24. BICK rising edge must not occur at the same time as LRCK edge.

Note 25. fsd (max) = 96kHz when TVDD < 3.0V in Daisy Chain mode.

Note 26. fsn (max) = 48kHz when TVDD < 3.0V in Daisy Chain mode.

Note 27. tBSH (min) = 4 nsec when TVDD > 2.6V and the LDOE pin = "L".

Note 28. DSD data transmitting device must meet this time.
tDDD is defined from a falling edge of DCLK "↓" to a DSDL/R edge when DCKB bit = "0" and it is defined from a rising edge of DCLK "↑" to a DSDL/R edge when DCKB bit = "1"

(Ta=-40 ~ 105°C: AVDD=3.0 ~ 5.5V, TVDD=1.7 ~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			nsec
CCLK Pulse Width Low	tCCKL	80			nsec
Pulse Width High	tCCKH	80			nsec
CDTI Setup Time	tCDS	40			nsec
CDTI Hold Time	tCDH	40			nsec
CSN "H" Time	tCSW	150			nsec
CSN "↓" to CCLK "↑"	tCSS	50			nsec
CCLK "↑" to CSN "↑"	tCSH	50			nsec
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µsec
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µsec
Clock Low Time	tLOW	1.3		-	µsec
Clock High Time	tHIGH	0.6		-	µsec
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µsec
SDA Hold Time from SCL Falling (Note 29)	tHD:DAT	0		-	µsec
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µsec
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µsec
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µsec
Setup Time for Stop Condition	tSU:STO	0.6		-	µsec
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	nsec
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing (Note 30)					
PDN Accept Pulse Width	tAPD	150			nsec
PDN Reject Pulse Width	tRPD			30	nsec

Note 29. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 30.The AK4452 can be reset by bringing the PDN pin to "L".
Note 31. I^2C is a trademark of NXP B.V.

■ Timing Diagram

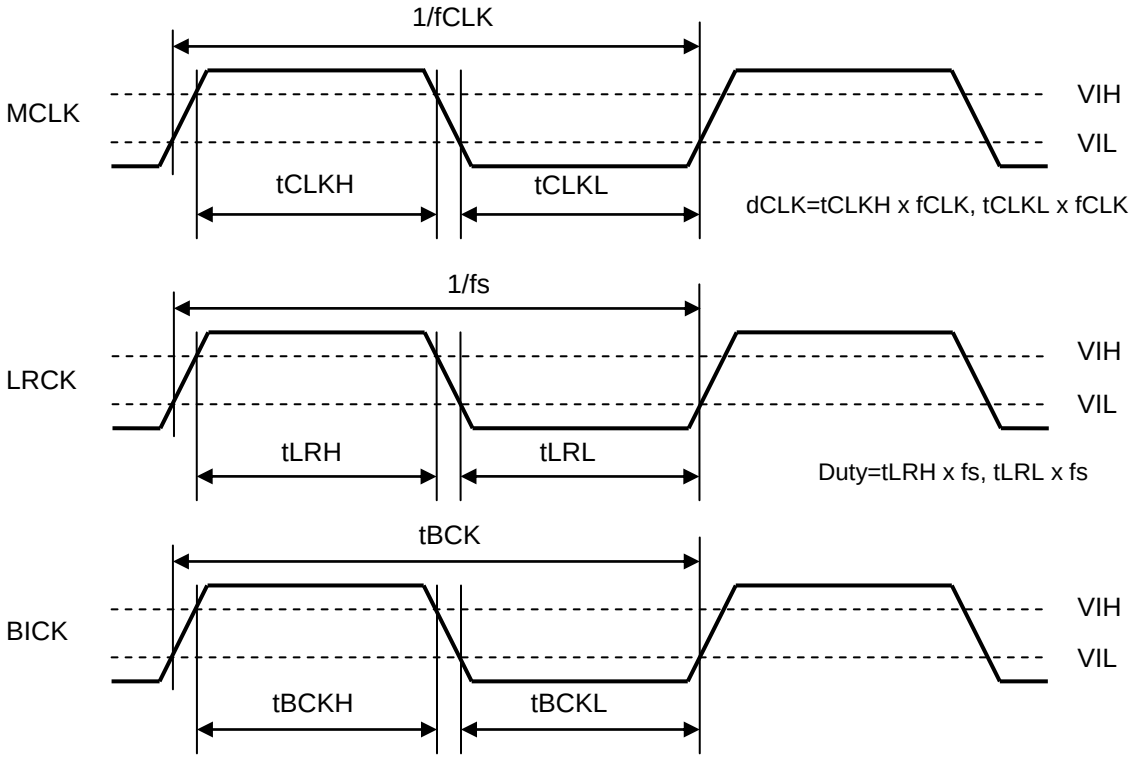


Figure 10. Clock Timing

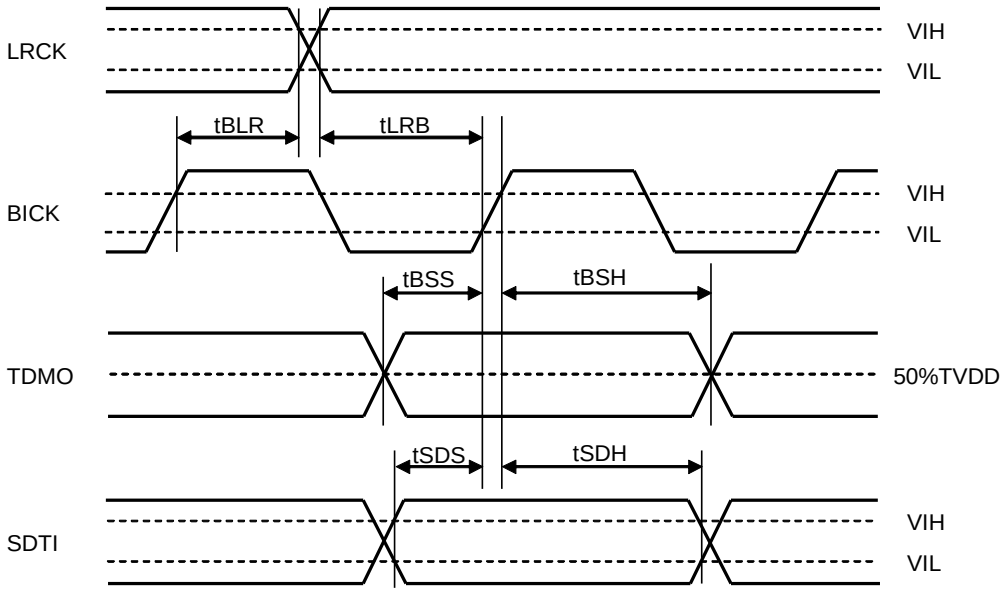


Figure 11. Audio Interface Timing (PCM Mode)

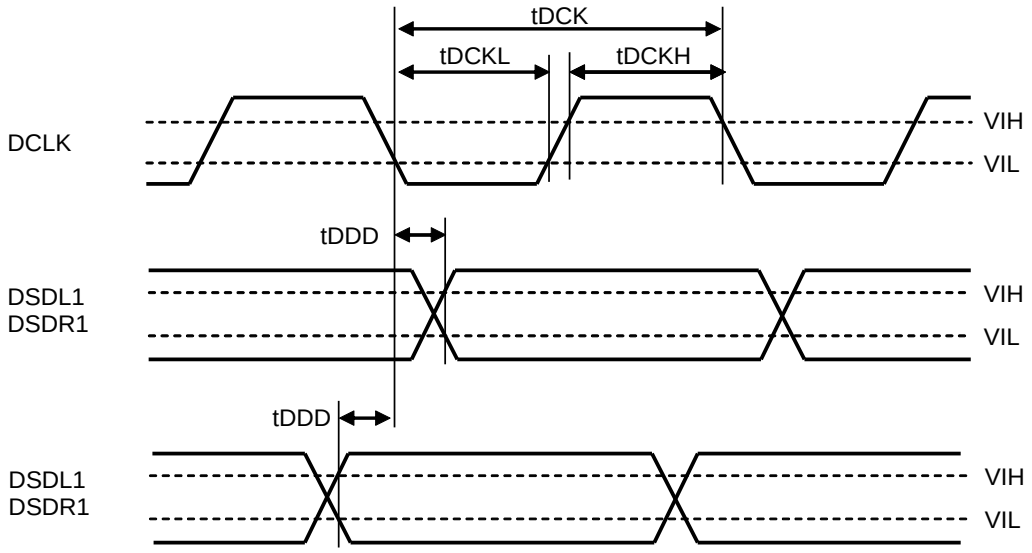


Figure 12. Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")

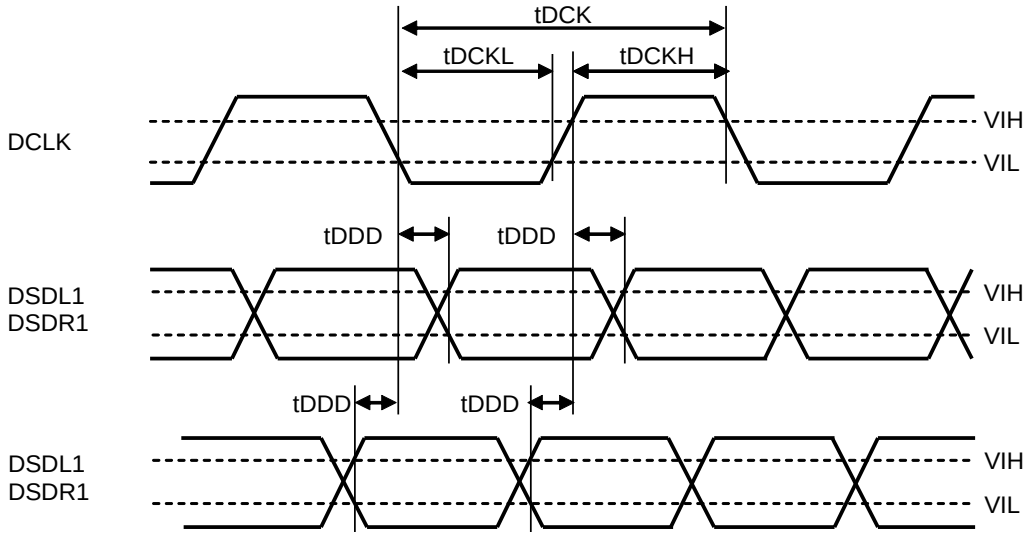


Figure 13. Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")

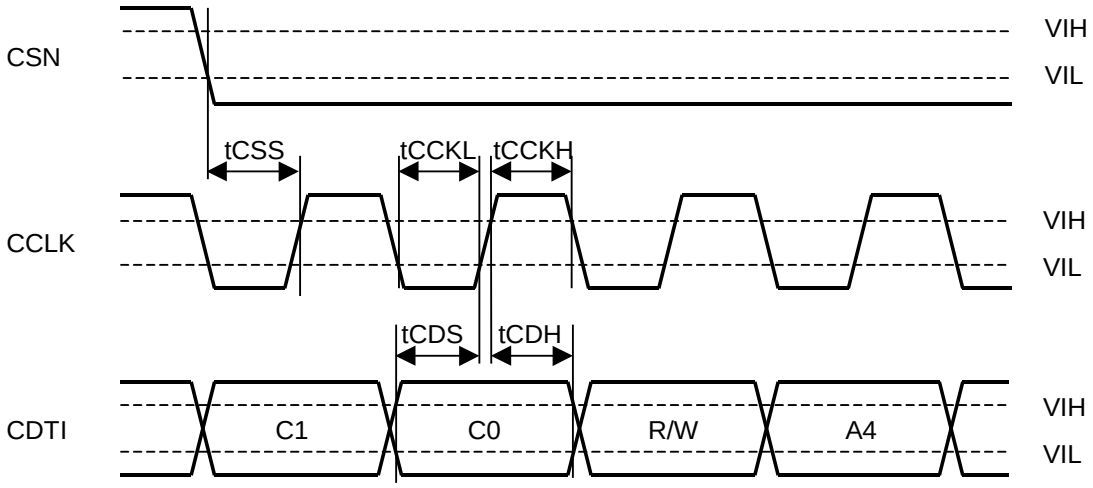


Figure 14. WRITE Command Input Timing (3-wire Serial Mode)

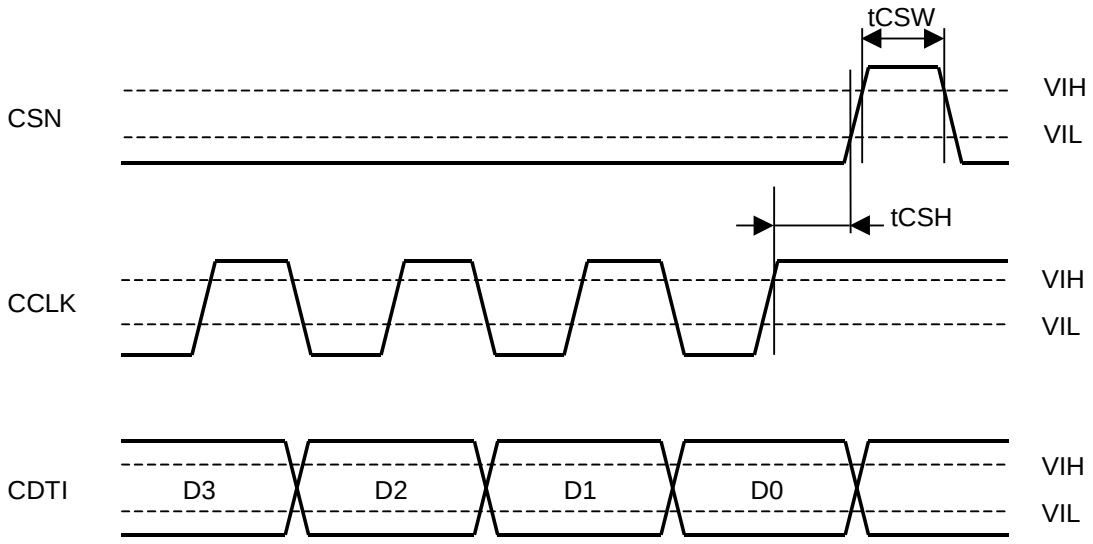


Figure 15. WRITE Data Input Timing (3-wire Serial Mode)

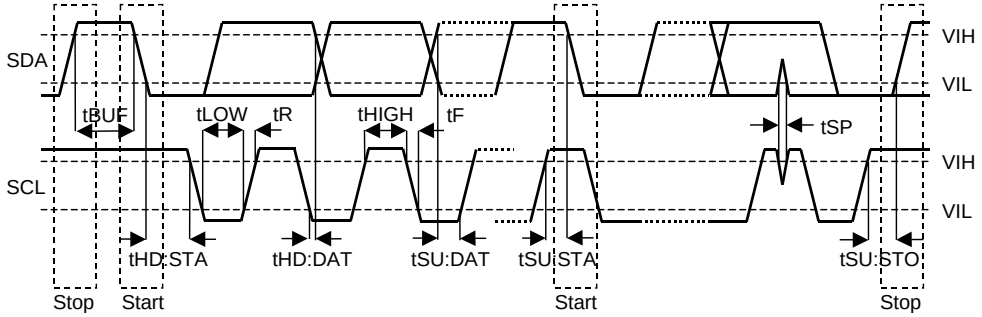


Figure 16. I^{2}C Bus mode Timing

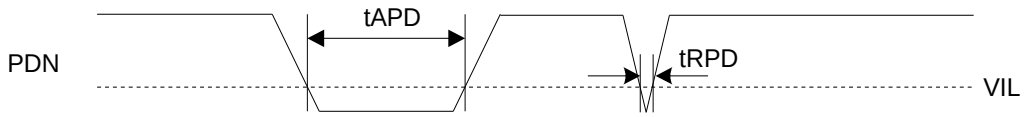


Figure 17. Power-down & Reset Timing

9. Functional Descriptions

■ D/A Conversion Mode (PCM mode, DSD mode)

The AK4452 can perform D/A conversion for either PCM data or DSD data. The DP bit controls PCM/DSD mode. When DSD mode, DSD data can be input from DCLK, DSDL and DSDR pins. When PCM mode, PCM data can be input from BICK, LRCK and SDTI pins. When PCM/DSD mode is changed by DP bit, the AK4452 should be reset by RSTN bit. It takes about 2/fs to 3/fs to change the mode. Only PCM data is supported in parallel mode.

DP bit	Interface
0	PCM
1	DSD

Table 1. PCM/DSD Mode Control

■ System Clock

[1] PCM Mode

The external clocks, which are required to operate the AK4452, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta - sigma modulator.

There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by the DFS0, DFS1 (Table 2) bits. The frequency of MCLK at each sampling speed is set automatically. When reset is released (PDN pin = "↑"), the AK4452 is in Manual Setting Mode. In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 5) and the internal master clock attains the appropriate frequency (Table 6, Table 7), so it is not necessary to set DFS bits.

1. Manual Setting Mode (ACKS bit = "0")

MCLK frequency is detected automatically and the sampling rate is set by DFS2-0 bits (Table 2). The MCLK frequency corresponding to each sampling speed should be provided externally (Table 3, Table 4).
The AK4452 is set to Manual Setting Mode at power-up (PDN pin = "L" →"H"). When DFS2-0 bits are changed, the AK4452 should be reset by RSTN bit.

DFS2	DFS1	DFS0	Sampling Rate (fs)		
0	0	0	Normal Speed Mode	8kHz ~ 54kHz	(default)
0	0	1	Double Speed Mode	54kHz ~ 108kHz	
0	1	0	Quad Speed Mode	120kHz ~ 216kHz	
0	1	1	Reserved	(*)	
1	0	0	Oct Speed Mode	384kHz	
1	0	1	Hex Speed Mode	768kHz	
1	1	0	Reserved	(* Shift to 384kHz)	
1	1	1	Reserved	(* Shift to 768kHz)	

Table 2. Sampling Speed (Manual Setting Mode)

LRCK	MCLK(MHz)						Sampling
Fs	16fs	32fs	48fs	64fs	96fs	128fs	Speed
32.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	N/A	22.5792	Quad
192.0kHz	N/A	N/A	N/A	N/A	N/A	24.5760	Quad
384kHz	N/A	12.288	18.432	24.576	36.864	49.152	Oct
768kHz	12.288	24.576	36.864	49.152	N/A	N/A	Hex

Table 3. System Clock Example (Manual Setting Mode)

LRCK	MCLK(MHz)							Sampling
fs	192fs	256fs	384fs	512fs	768fs	1024fs	1152fs	Speed
32.0kHz	N/A	8.1920	12.2880	16.3840	24.5760	36.8640	36.8640	Normal
44.1kHz	N/A	11.2896	16.9344	22.5792	33.8688	N/A	N/A	
48.0kHz	N/A	12.2880	18.4320	24.5760	36.8640	N/A	N/A	
88.2kHz	N/A	22.5792	33.8688	45.1584	N/A	N/A	N/A	Double
96.0kHz	N/A	24.5760	36.8640	49.152	N/A	N/A	N/A	
176.4kHz	33.8688	45.1584	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	36.8640	49.152	N/A	N/A	N/A	N/A	N/A	Quad
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 4. System Clock Example (Manual Setting Mode)

2. Auto Setting Mode (ACKS bit = "1")

MCLK frequency and the sampling speed are detected automatically (Table 5) and DFS2-0 bits are ignored. The MCLK frequency corresponding to each sampling speed should be provided externally (Table 6, Table 7).

MCLK		Sampling Speed
1152fs		Normal (fs≤32kHz)
512fs/256fs	768fs/384fs	Normal
256fs	384fs	Double
128fs	192fs	Quad
64fs	96fs	Oct
32fs	48fs	Hex

Table 5. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)					Sampling Speed
fs	32fs	48fs	64fs	96fs	128fs	
32.0kHz	N/A	N/A	N/A	N/A	N/A	Normal
44.1kHz	N/A	N/A	N/A	N/A	N/A	
48.0kHz	N/A	N/A	N/A	N/A	N/A	
88.2kHz	N/A	N/A	N/A	N/A	N/A	Double
96.0kHz	N/A	N/A	N/A	N/A	N/A	
176.4kHz	N/A	N/A	N/A	N/A	22.5792	Quad
192.0kHz	N/A	N/A	N/A	N/A	24.5760	Quad
384kHz	N/A	N/A	24.576	36.864	N/A	Oct
768kHz	24.576	36.864	N/A	N/A	N/A	Hex

Table 6. System Clock Example (Auto Setting Mode)

LRCK	MCLK(MHz)						Sampling Speed
fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	N/A	(8.1920*)	(12.2880*)	16.3840	24.5760	36.8640	Normal (Double*)
44.1kHz	N/A	(11.2896*)	(16.9344*)	22.5792	33.8688	N/A	
48.0kHz	N/A	(12.2880*)	(18.4320*)	24.5760	36.8640	N/A	
88.2kHz	N/A	22.5792	33.8688	N/A	N/A	N/A	Double
96.0kHz	N/A	24.5760	36.8640	N/A	N/A	N/A	
176.4kHz	33.8688	N/A	N/A	N/A	N/A	N/A	Quad
192.0kHz	36.8640	N/A	N/A	N/A	N/A	N/A	Quad
384kHz	N/A	N/A	N/A	N/A	N/A	N/A	Oct
768kHz	N/A	N/A	N/A	N/A	N/A	N/A	Hex

Table 7. System Clock Example (Auto Setting Mode)

MCLK= 256fs/384fs supports sampling rate of 8kHz~96kHz (Table 8). However, when the sampling rate is 8kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

ACKS bit	MCLK	DR,S/N
0	256fs/384fs/512fs/768fs	115dB
1	256fs/384fs	112dB
1	512fs/768fs	115dB

Table 8. Relationship of DR, S/N and MCLK frequency (fs = 44.1kHz)

[2] DSD mode (Serial Control mode only)

The AK4452 is capable to playback DSD data. The external clocks, which are required to operate the AK4452, are MCLK and DCLK. MCLK should be synchronized with DCLK but the phase is not critical. The frequency of MCLK is set by DCKS bit. (Table 9)

After exiting reset (PDN pin = "L" → "H", RSTN bit= "0" → "1") upon power-up, the AK4452 is in power-down state until MCLK and DCLK are input.

DCKS bit	MCLK Frequency	DCLK Frequency	
0	512fs	64fs/128fs/256fs	(default)
1	768fs	64fs/128fs/256fs	

Table 9. System Clock (DSD Mode)

The AK4452 supports 64fs, 128fs and 256fs data stream (fs= 32kHz, 44.1kHz, 48kHz). DSDSEL1-0 bits control this setting. (Table 10)

DSDSEL1	DSDSEL0	DSD data stream			
		fs=32kHz	fs=44.1kHz	fs=48kHz	
0	0	2.048MHz	2.8224MHz	3.072MHz	(default)
0	1	4.096MHz	5.6448MHz	6.144MHz	
1	0	8.192MHz	11.2896MHz	12.288MHz	
1	1	Reserved (8.192MHz)	Reserved (11.2896MHz)	Reserved (12.288MHz)	

Table 10. DSD Data Stream Select

DSDD bit selects DSD playback mode (Table 11). When DSDD bit= "1", the output volume control is not available and the cut off filter value is fixed to 100kHz.

DSDD bit	Mode	
0	Full function	(default)
1	Volume pass	

Table 11. DSD Playback Mode Select

The cut off filter characteristic in DSD mode can be selected by DSDF bit. (Table 12)

DSDF bit	Cut Off Filter	
0	50kHz	(default)
1	100kHz	

Table 12. DSD Filter Select

■ Audio Interface Format

The AK4452 supports both PCM and DSD formats for digital input signal. Mode settings are available by the pins (TDM1-0 pins, DIF pin and DCHAIN pin) and registers (TDM1-0 bits, DIF2-0 bits, SDS2-0 bits and DCHAIN bit). The RSTN bit should be toggled in case these format setting bits are changed during operation.

[1] PCM Mode

Normal Mode (TDM1-0 bits="00")
Two channels audio data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 bits as shown in Table 13. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used in 16-bit and 20-bit MSB justified and Mode 6 can be used in 16-bit, 20-bit and 24-bit MSB justified formats by zeroing the unused LSBs.

TDM128 Mode (TDM1-0 bits="01")
Four channels audio data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Data is selected by SDS2-0 bits. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 13. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.

TDM256 Mode (TDM1-0 bits="10")
Eight channels audio data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Data is selected by SDS2-0 bits. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 13. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.

TDM512 Mode (TDM1-0 bits="11")
Sixteen channels audio data is shifted in via the SDTI1 pin using BICK and LRCK inputs. Data is selected by SDS2-0 bits. BICK is fixed to 512fs. Six data formats are supported and selected by the DIF2-0 bits as shown in Table 13. In all formats the serial data is MSB first, 2's compliment format and is latched on the rising edge of BICK.

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	SDTI Format	LRCK	BICK
Normal (Note 32)	0	0	0	0	0	0	16-bit LSB justified	H/L	≥32fs
	1			0	0	1	20-bit LSB justified	H/L	≥40fs
	2			0	1	0	24-bit MSB justified	H/L	≥48fs
	3			0	1	1	24-bit I^2S compatible	L/H	≥48fs
	4			1	0	0	24-bit LSB justified	H/L	≥48fs
	5			1	0	1	32-bit LSB justified	H/L	≥64fs
	6			1	1	0	32-bit MSB justified	H/L	≥64fs
	7			1	1	1	32-bit I^2S compatible	L/H	≥64fs
TDM128		0	1	0	0	0	N/A	↑	128fs
				0	0	1	N/A	↑	128fs
	8			0	1	0	24-bit MSB justified	↑	128fs
	9			0	1	1	24-bit I^2S compatible	↓	128fs
	10			1	0	0	24-bit LSB justified	↑	128fs
	11			1	0	1	32-bit LSB justified	↑	128fs
	12			1	1	0	32-bit MSB justified	↑	128fs
	13			1	1	1	32-bit I^2S compatible	↓	128fs
TDM256		1	0	0	0	0	N/A	↑	256fs
				0	0	1	N/A	↑	256fs
	14			0	1	0	24-bit MSB justified	↑	256fs
	15			0	1	1	24-bit I^2S compatible	↓	256fs
	16			1	0	0	24-bit LSB justified	↑	256fs
	17			1	0	1	32-bit LSB justified	↑	256fs
	18			1	1	0	32-bit MSB justified	↑	256fs
	19			1	1	1	32-bit I^2S compatible	↓	256fs
TDM512		1	1	0	0	0	N/A	↑	512fs
				0	0	1	N/A	↑	512fs
	20			0	1	0	24-bit MSB justified	↑	512fs
	21			0	1	1	24-bit I^2S compatible	↓	512fs
	22			1	0	0	24-bit LSB justified	↑	512fs
	23			1	0	1	32-bit LSB justified	↑	512fs
	24			1	1	0	32-bit MSB justified	↑	512fs
	25			1	1	1	32-bit I^2S compatible	↓	512fs

(Shaded settings are not available)

Table 13. Audio Interface Format

Note 32. BICK that is input to each channel must be longer than the bit length of setting format.

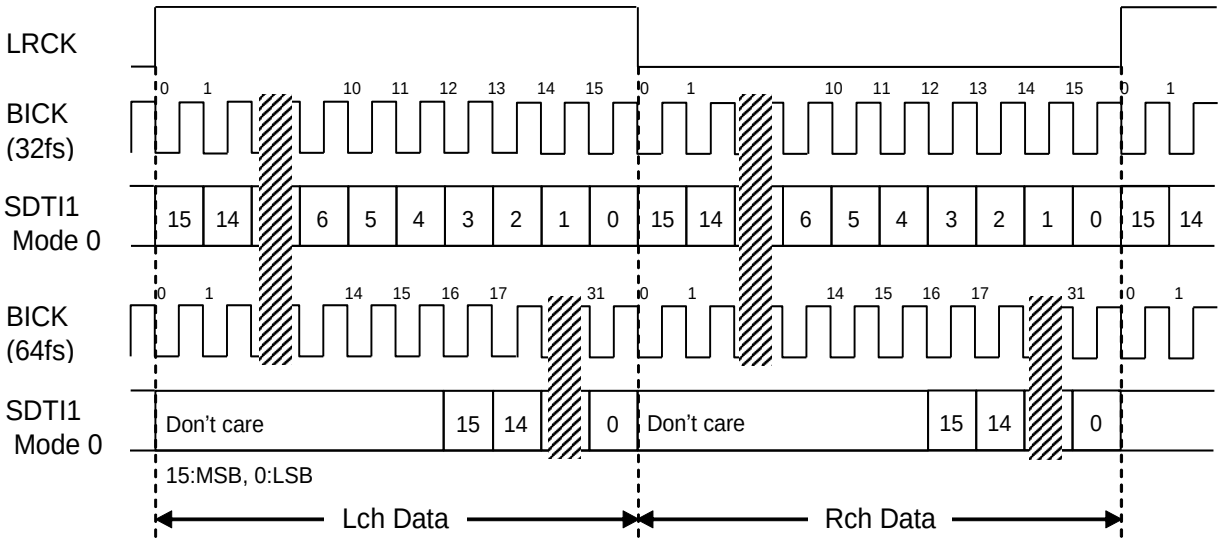


Figure 18. Mode 0 Timing

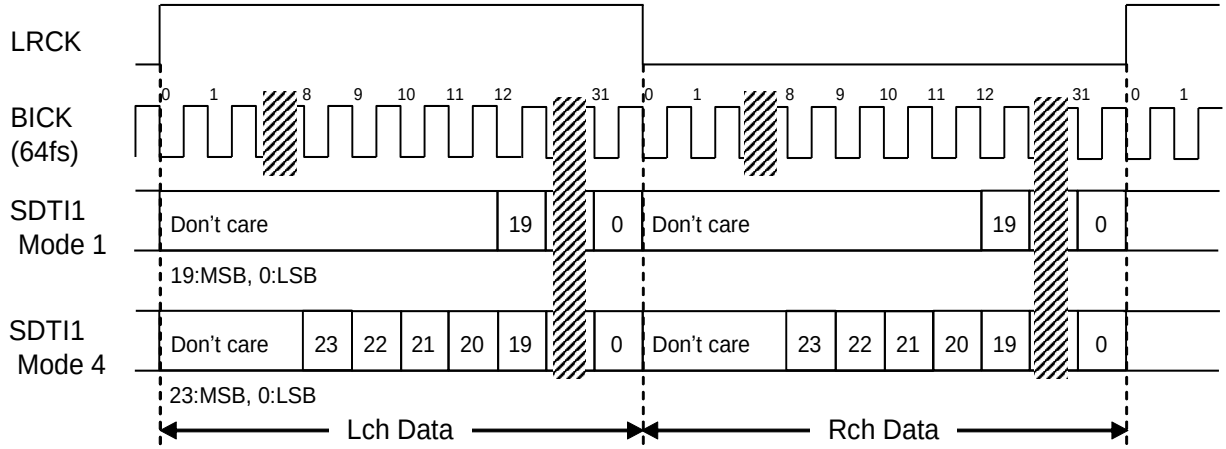


Figure 19. Mode 1/4 Timing

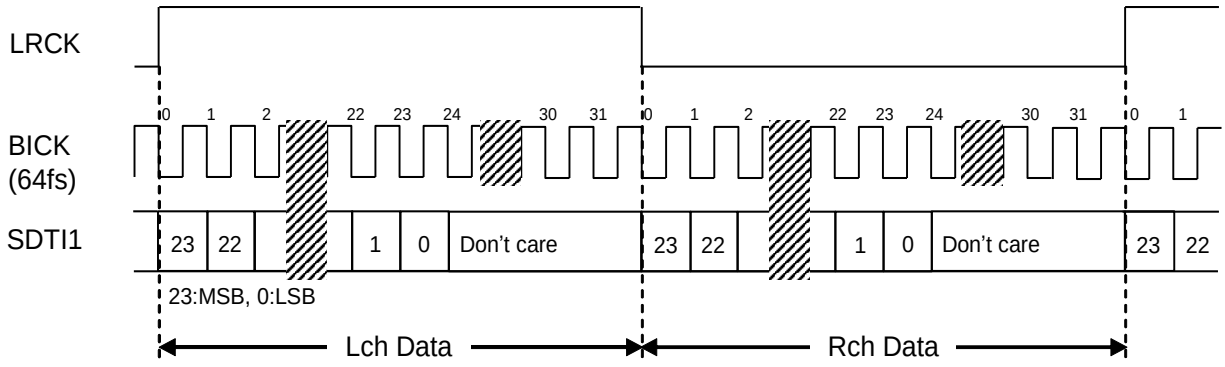


Figure 20. Mode 2 Timing

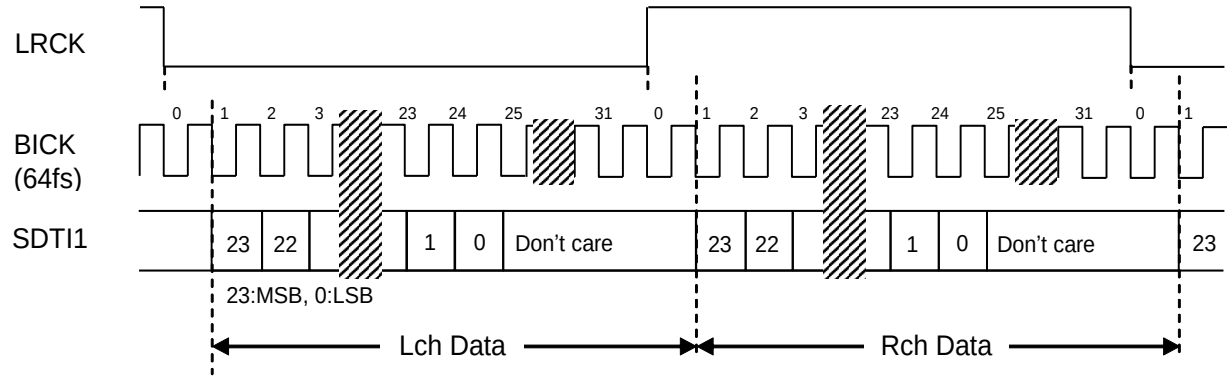


Figure 21. Mode 3 Timing

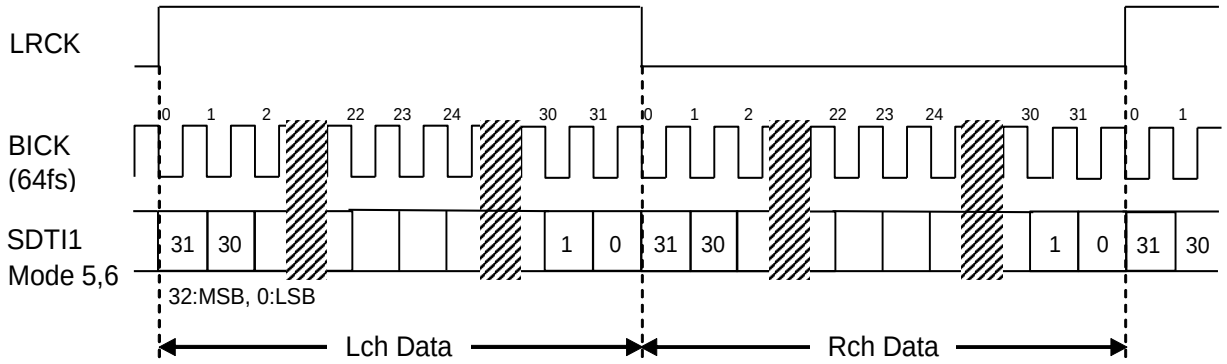


Figure 22. Mode 5/6 Timing

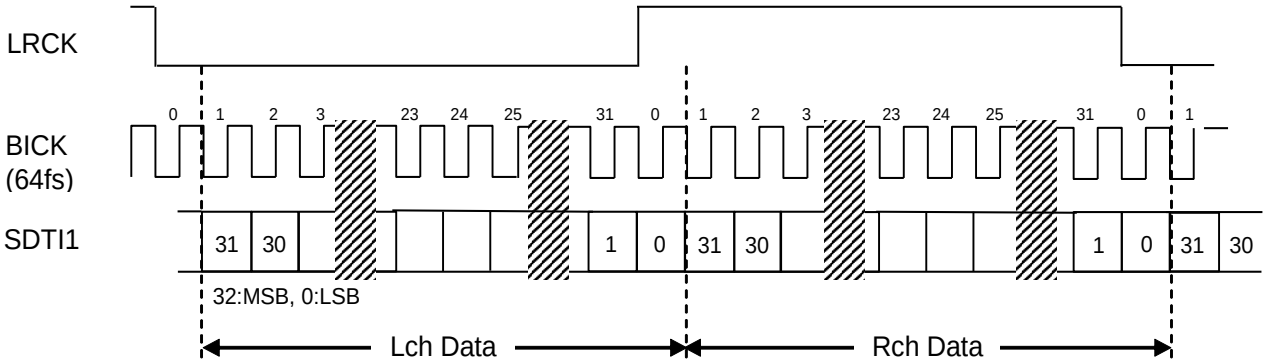


Figure 23. Mode 7 Timing

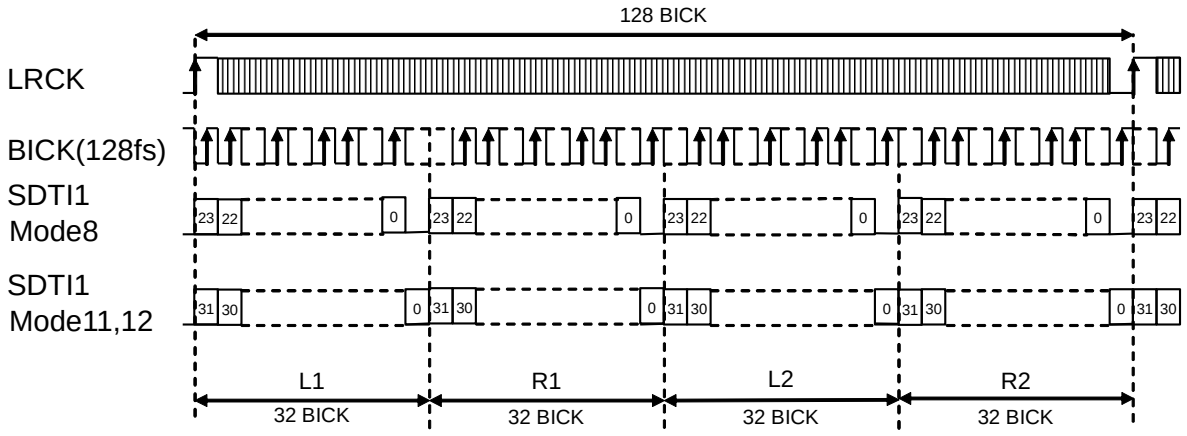


Figure 24. Mode 8/11/12 Timing

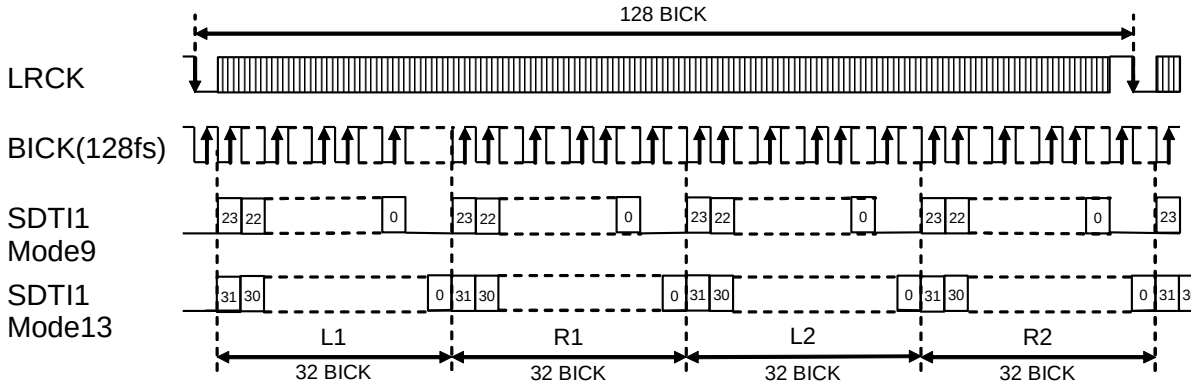


Figure 25. Mode 9/13 Timing

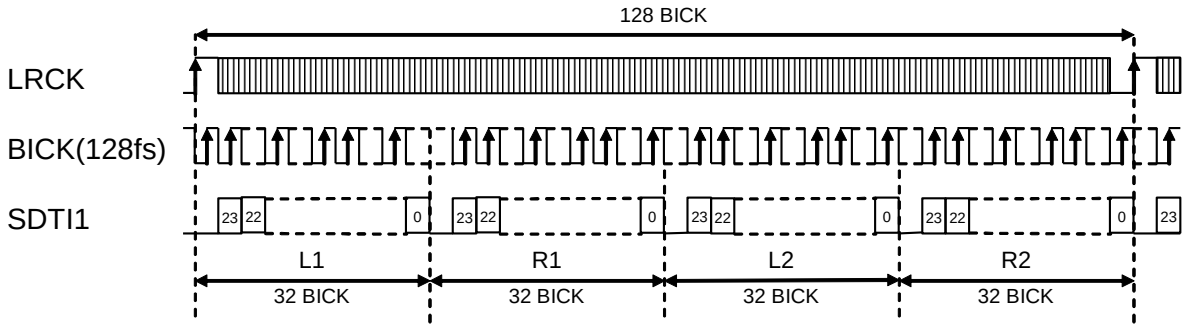


Figure 26. Mode 10 Timing

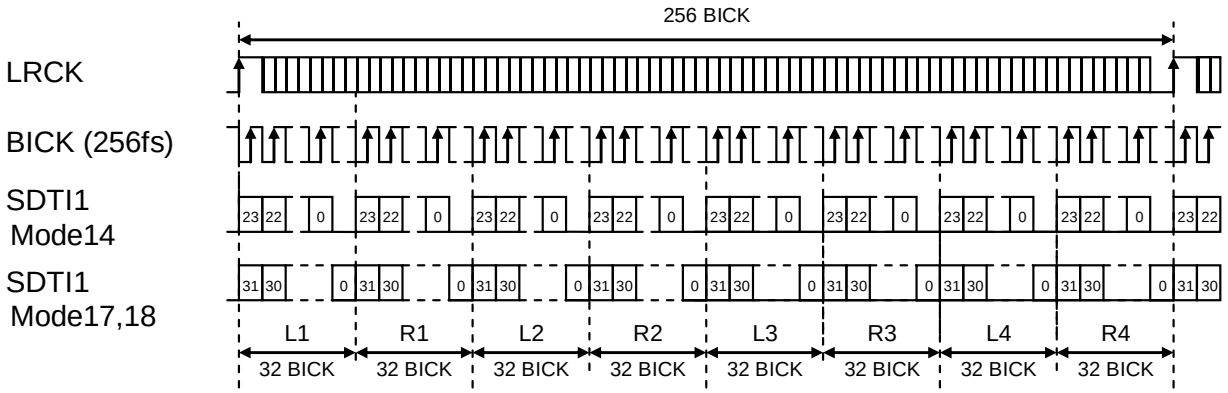


Figure 27. Mode 14/17/18 Timing

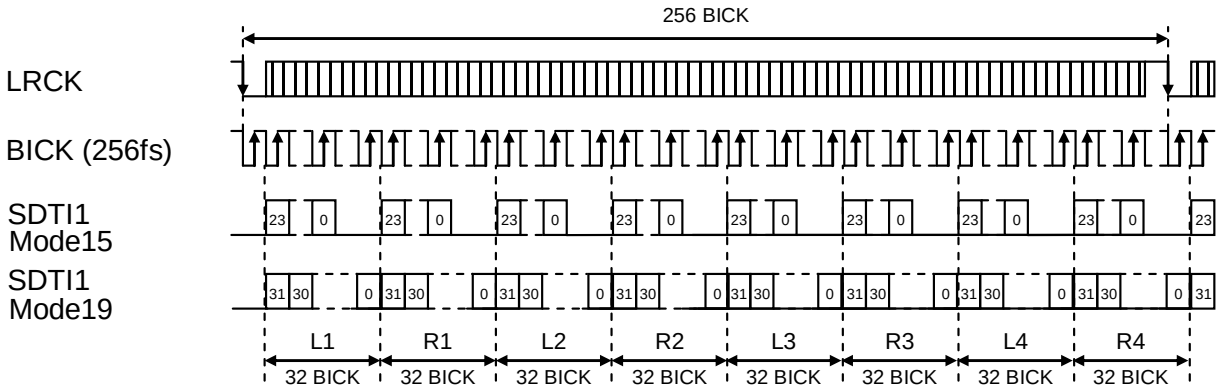


Figure 28. Mode 15/19 Timing

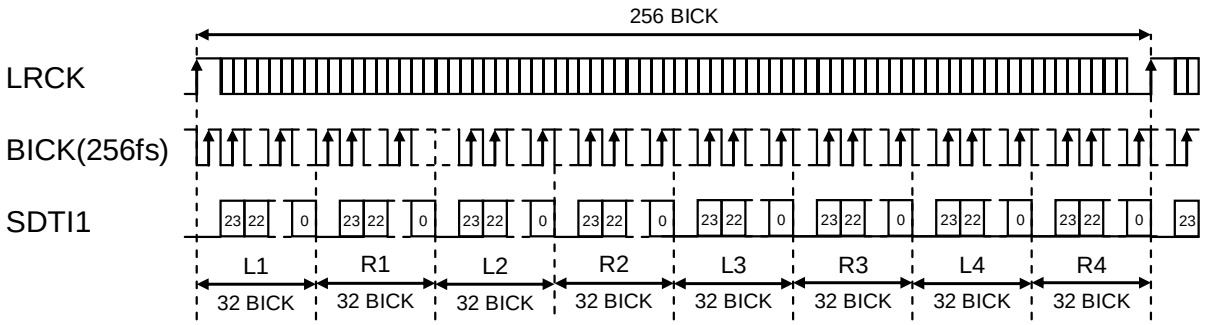


Figure 29. Mode 16 Timing

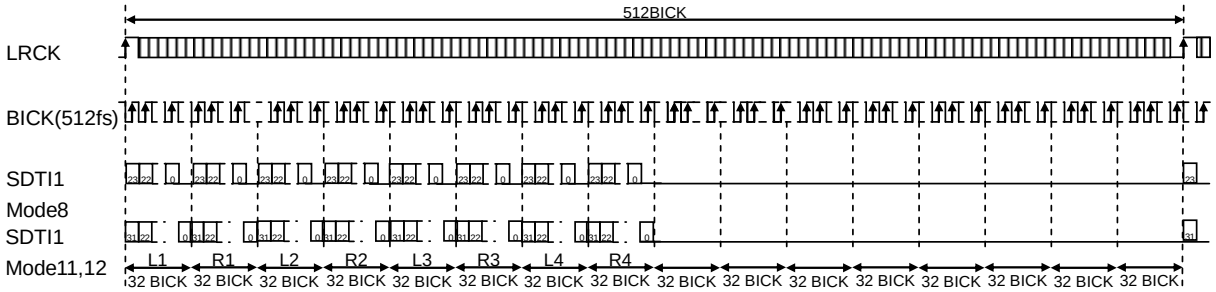


Figure 30. Mode 20/23/24 Timing

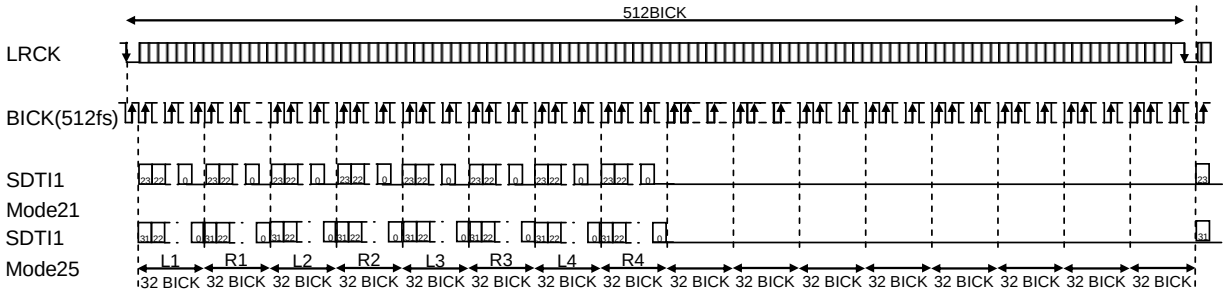


Figure 31. Mode 21/25 Timing

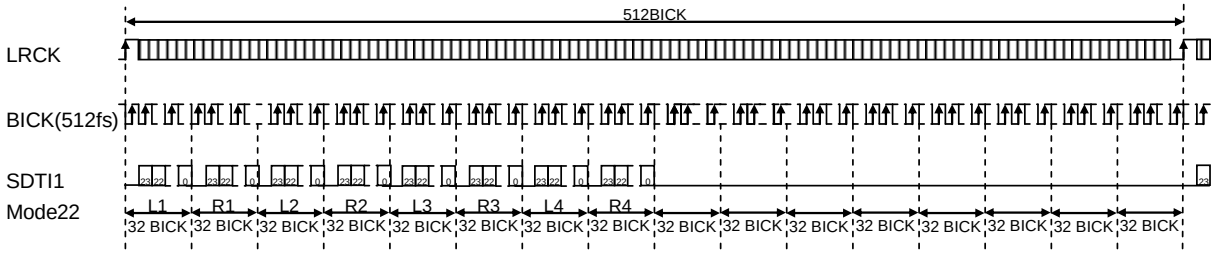


Figure 32. Mode 22 Timing

[1]-1. Data Select

One data cycle of SDTI1 for each format are defined as below. SDS2-0 bits control playback channel of each DAC.

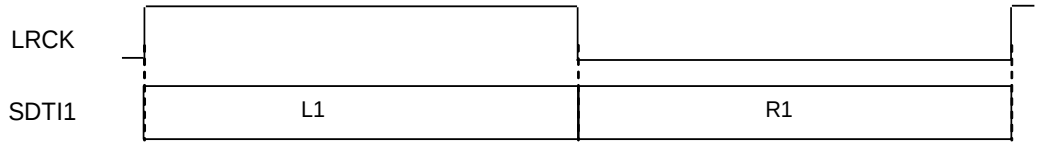


Figure 33. Data Slot in Normal Mode

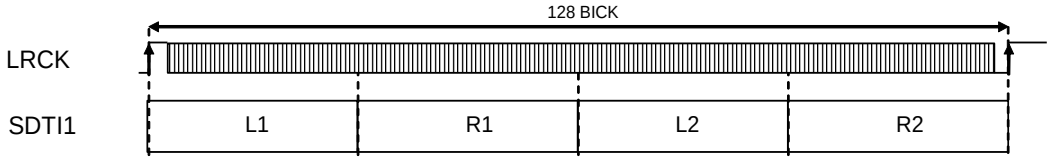


Figure 34. Data Slot in TDM128 Mode

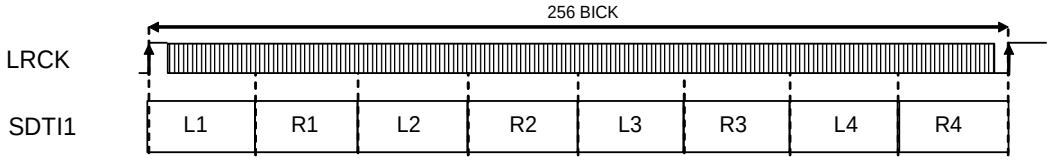


Figure 35. Data Slot in TDM256 Mode

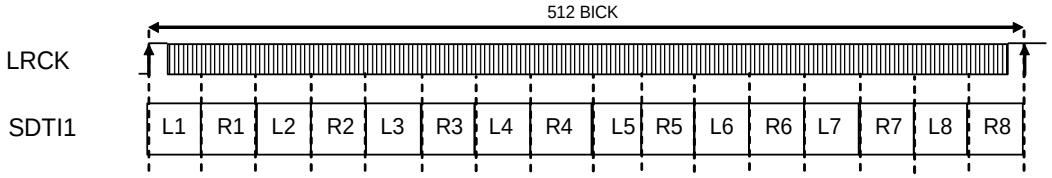


Figure 36. Data Slot in TDM512 Mode

	SDS2	SDS1	SDS0	DAC	
				Lch	Rch
Normal	*	*	*	L1	R1
TDM128	*	0	0	L1	R1
	*	0	1	L2	R2
TDM256	0	0	0	L1	R1
	0	0	1	L2	R2
	0	1	0	L3	R3
	0	1	1	L4	R4
TDM512	0	0	0	L1	R1
	0	0	1	L2	R2
	0	1	0	L3	R3
	0	1	1	L4	R4
	1	0	0	L5	R5
	1	0	1	L6	R6
	1	1	0	L7	R7
	1	1	1	L8	R8

(*: Do not care)

Table 14. Data Select

[1]-2. Daisy Chain

AK4452 is available for Daisy Chain structure. Set DCHAIN bit to “1” or DCHAIN pin to “H” to enable Daisy Chain mode. Daisy Chain supports TDM512/256 mode.

(1)TDM512 mode
Figure 37 shows example of TDM512 mode Daisy Chain structure (TDM1-0 bits= “11”). 16ch data is input to the second AK4452’s SDTI1 pin from a DSP. Connect the second AK4452’s TDMO1 pin to the first AK4452’s SDTI1 pin.

Figure 38 shows data I/O example of TDM512 mode. SDTI1 (L8, R8) data is the input for the DAC of the second AK4452, and the second AK4452 outputs the data from TDMO1 by shifting 2ch. The first AK4452 accepts SDTI1 (L7, R7) data as input data of DAC. DIF2-0 bits setting of both first AK4452 and the second AK4452 must be the same.

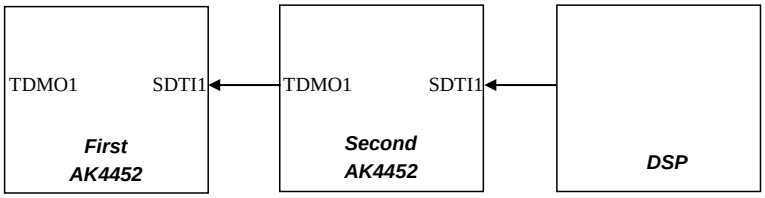


Figure 37. Daisy Chain (TDM512/256 Mode)

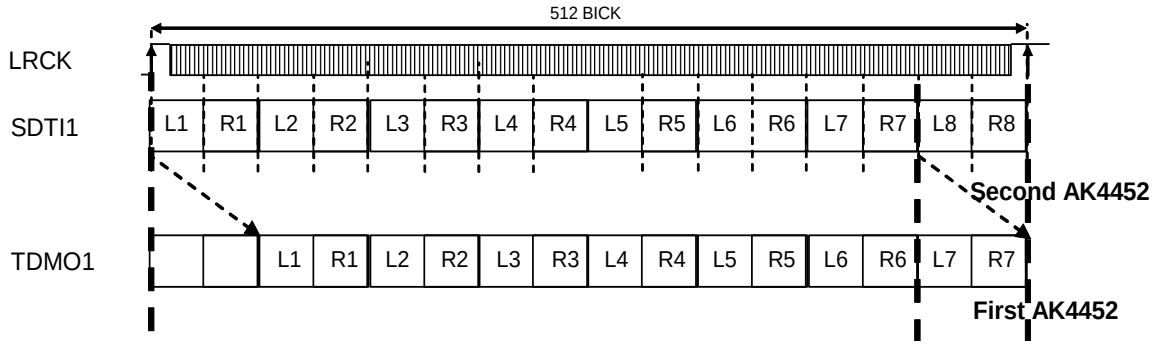


Figure 38. Daisy Chain (TDM512 Mode)

(2)TDM256 mode

Figure 37 shows example of TDM256 mode Daisy Chain structure (TDM1-0 bits= “10”). 8ch data is input to the second AK4452’s SDTI1 pin from a DSP. Connect the second AK4452’s TDMO1 pin to the first AK4452’s SDTI1 pin.

Figure 39 shows data I/O example of TDM256 mode. SDTI1 (L4, R4) data is the input for the DAC of the second AK4452, and the second AK4452 outputs the data from TDMO1 by shifting 2ch. The first AK4452 accepts SDTI1 (L3, R3) data as input data of DAC. DIF2-0 bits setting of both first AK4452 and the second AK4452 must be the same.

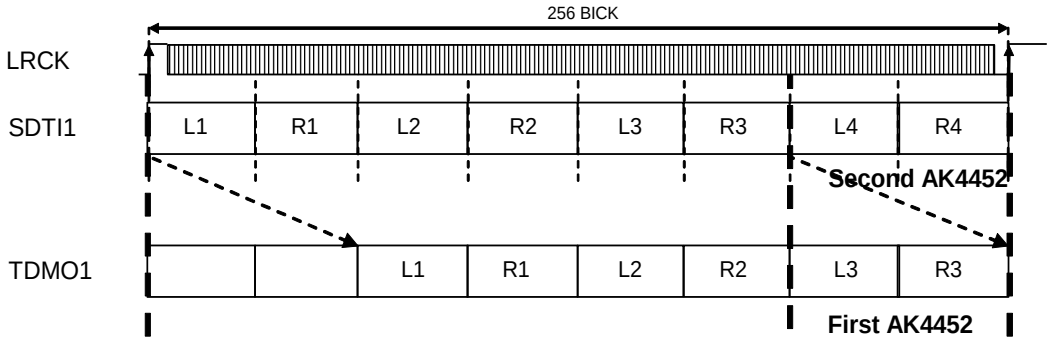


Figure 39. Daisy Chain (TDM256 Mode)

[2] DSD Mode

2ch Data is shifted in via the DSDL1 and DSDR1 pins using DCLK inputs. DSD data is supported by both Normal mode (Figure 40) and Phase Modulation mode (Figure 41). Input data is clocked in on a rising or falling edge of DCLK that is set by DCKB bit.

The frequency of DCLK is variable at 64fs, 128fs and 256fs by setting DSDSEL1-0 bits.

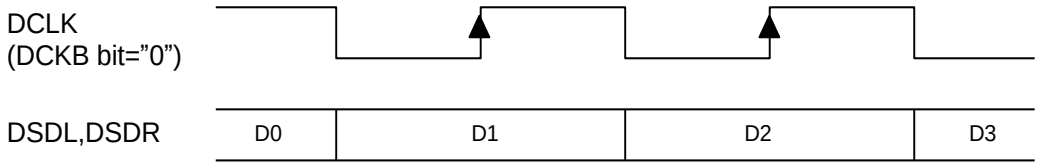


Figure 40. DSD Mode Timing (Normal Mode)

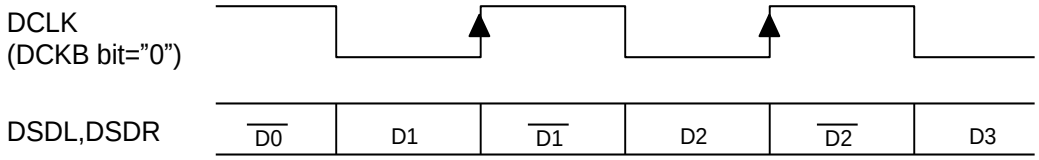


Figure 41. DSD Mode Timing (Phase Modulation Mode)

■ D/A Conversion Mode (PCM Mode, DSD Mode) Switching Timing

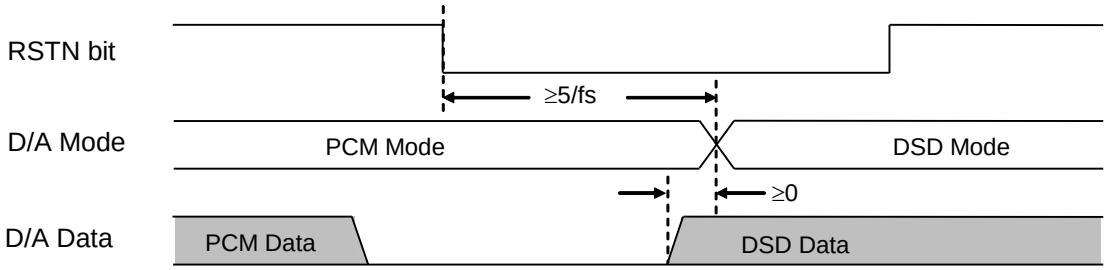


Figure 42. D/A Mode Switching Timing (PCM to DSD)

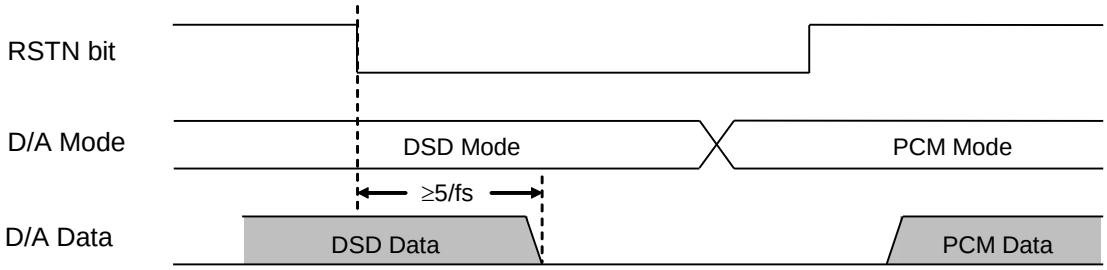


Figure 43. D/A Mode Switching Timing (DSD to PCM)

Note 33. The signal range is defined as 25% ~ 75% duty ratios in DSD mode. DSD signal must not go beyond this duty range at the SACD format book (Scarlet Book).

■ Digital Filter (PCM mode)

Four digital filters are available for playback, providing a choice of different sound colors. These digital filters are selected by SD bit, SLOW bit and SSLOW bit.

SSLOW	SD bit	SLOW bit	Mode	
0	0	0	Sharp roll-off filter	
0	0	1	Slow roll-off filter	
0	1	0	Short delay Sharp roll-off filter	(default)
0	1	1	Short delay Slow roll-off filter	
1	*	*	Super Slow Roll-off Mode	

Table 15. Digital Filter Setting (*: don't care)

The slowest frequency characteristics setting is when SSLOW bit = "1".

■ De-emphasis Filter (PCM mode)

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and is enabled or disabled with DEM11-10 bits (DEM bits).

DEM11-10 bits control de-emphasis mode of DAC. DEM bits settings are invalid in DSD mode. This mode is only valid in PCM Normal Speed Mode.

DEM11	DEM10	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 16. De-emphasis Control

■ Output Volume (PCM mode, DSD mode)

The AK4452 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each DAC can be set by ATT7-0 bits (register 03-04H), respectively (Table 17). Input data is attenuated from 0dB to -127dB including Mute. The transition between set values is a soft transition, thus no switching noise is occurred.

ATT7-0bits (register03-04H)	Attenuation Level	
FFH	+0dB	(default)
FEH	-0.5dB	
FDH	-1.0dB	
:	:	
:	:	
02H	-126.5dB	
01H	-127.0dB	
00H	MUTE (-∞)	

Table 17. Attenuation level of Digital Attenuator

Transition time between set values of ATL/R7-0 bits can be selected by the ATS1-0 bits (Table 18). The transition between set values is a soft transition in Mode0/1/2/3 eliminating switching noise in the transition. The register settings are maintained when switching the mode between PCM and DSD modes.

Mode	ATS1	ATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 18. Transition Time between Set Values of ATT7-0 bits

The transition between set values is a soft transition of 4080 levels in mode 0. It takes 4080/fs (92.5ms @fs=44.1kHz) from FFH to 00H. If the PDN pin goes to “L”, ATT7-0 bits are initialized to FFH.

If the digital volume is changed during reset, the volume will be changed to the setting value after releasing the reset. If the volume is changed in 5/fs after releasing a reset, the volume is changed immediately without soft transition.

In DSD mode, the digital volume is set to MUTE by setting ATT7-0 bits = “02H” or “01H”.

■ Out of Band Noise Reduction Filter (PCM mode, DSD mode)

The AK4452 has an out of band noise reduction filter that can change frequency response. This FIR filter attenuates out of band noise and may reduce degradation of the analog characteristics caused by a switching regulator, etc. Best performance should be achieved by clean linear regulated AVDD/VREF power supplies and the default setting of the FIR2-0 bits. These conditions are included in the Analog Characteristics specs. FIR2-0 bits set the frequency for noise attenuation. The filter characteristics will differ in DSD direct mode compared with other modes (Table 19).

FIR2-0 bits	FIR filter Mode	FIR filter		
		Except DSD direct mode	DSD direct mode	
000	0	1/4*[1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0]	1/2*[1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0]	(default)
001	1	1/4*[1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 1]	1/2*[0 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0]	
010	2	1/4*[1 0 1 0 0 0 0 0 0 0 0 0 0 1 0 1]	1/2*[0 0 1 0 0 0 0 0 0 0 0 0 0 1 0 0]	
011	3	1/4*[1 0 0 1 0 0 0 0 0 0 0 0 1 0 0 1]	1/2*[0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0]	
100	4	1/4*[1 0 0 0 1 0 0 0 0 0 0 1 0 0 0 1]	1/2*[0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0]	
101	5	1/4*[1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1]	1/2*[0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0]	
110	6	1/4*[1 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1]	1/2*[0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 0]	
111	7	1/4*[1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 1]	1/2*[0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0]	

Table 19. FIR Filter Setting

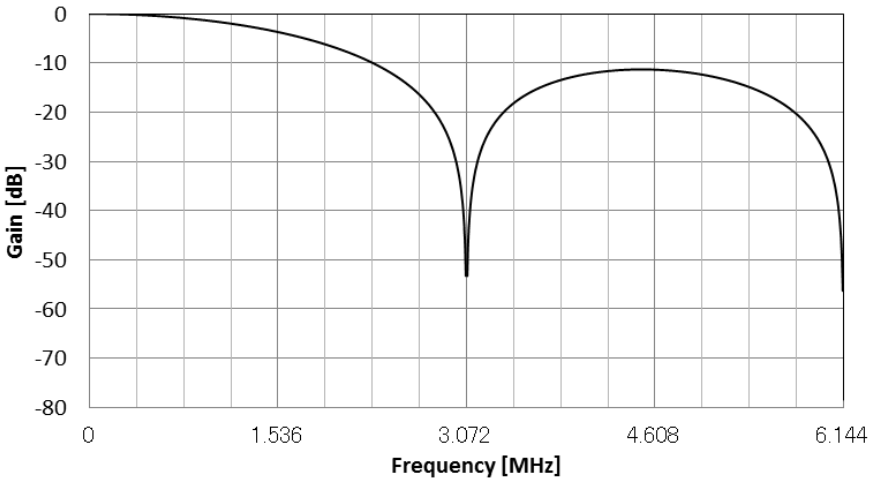


Figure 44. Mode0 FIR Filter (Except DSD direct mode)

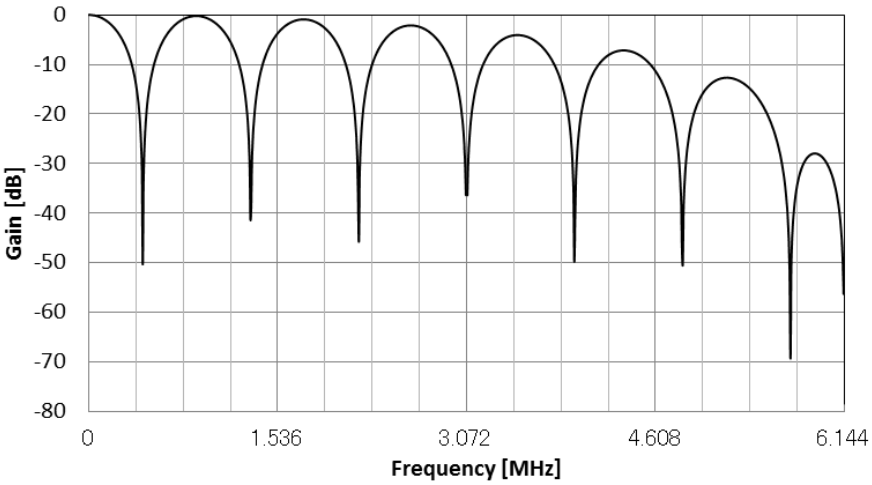


Figure 45. Mode1 FIR Filter (Except DSD direct mode)

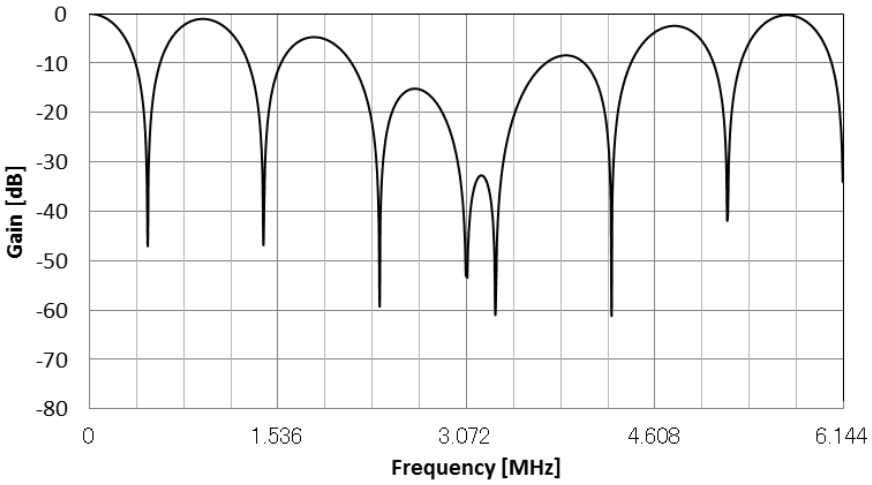


Figure 46. Mode2 FIR Filter (Except DSD direct mode)

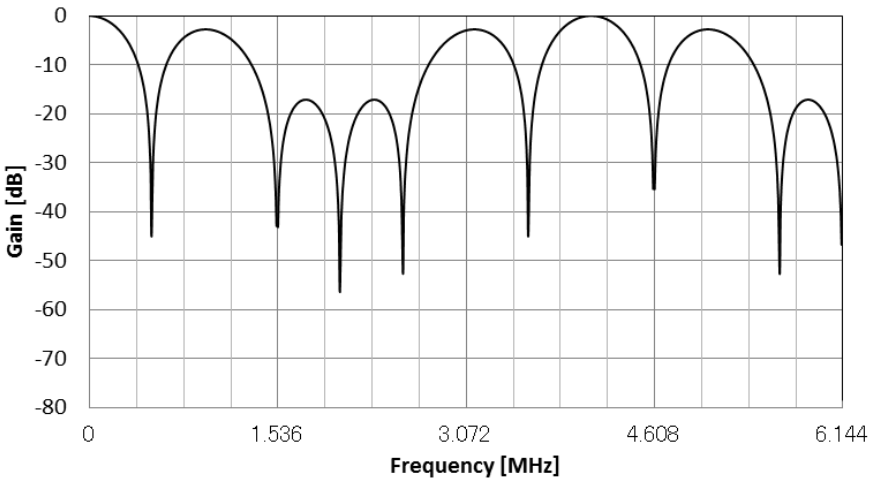


Figure 47. Mode3 FIR Filter (Except DSD direct mode)

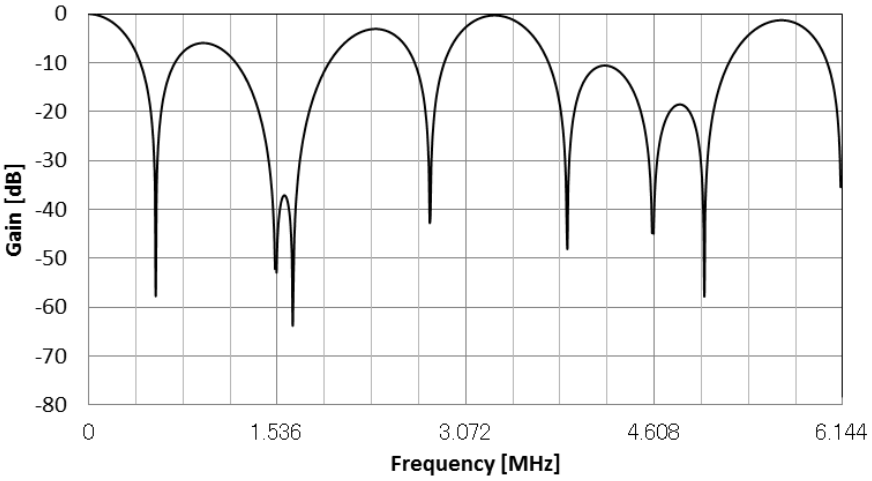


Figure 48. Mode4 FIR Filter (Except DSD direct mode)

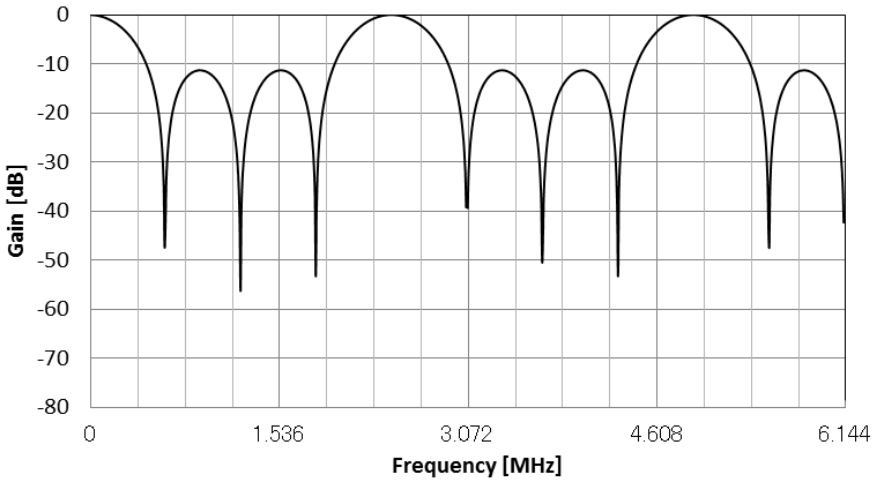


Figure 49. Mode5 FIR Filter (Except DSD direct mode)

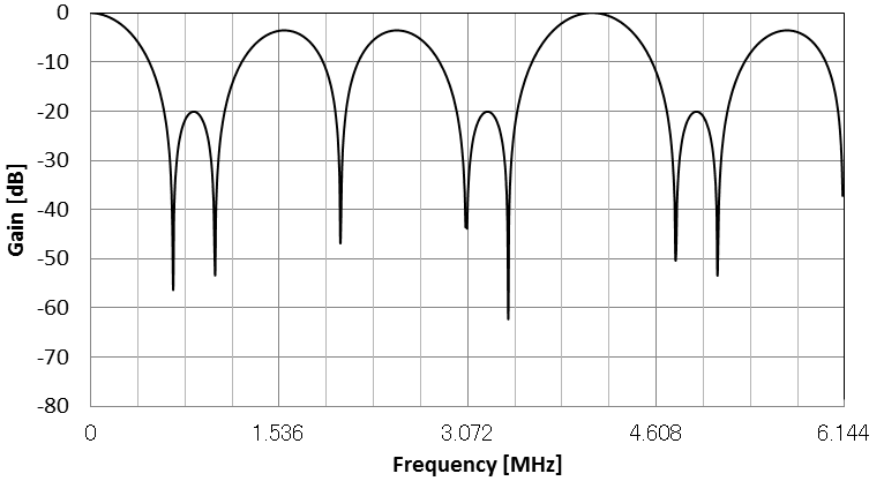


Figure 50. Mode6 FIR Filter (Except DSD direct mode)

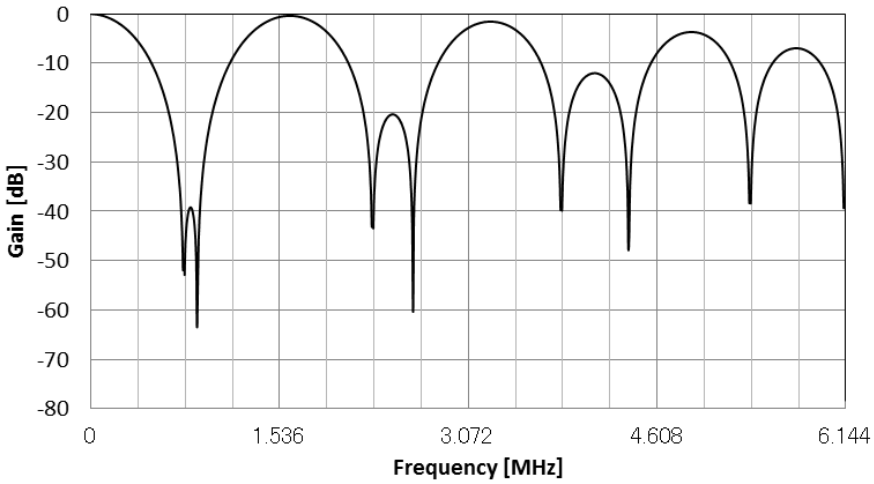


Figure 51. Mode7 FIR Filter (Except DSD direct mode)

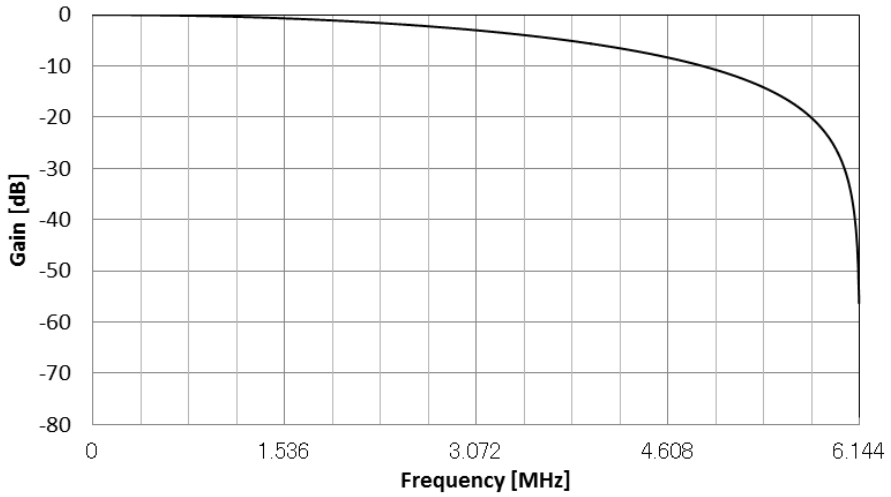


Figure 52. Mode0 FIR Filter (DSD direct mode)

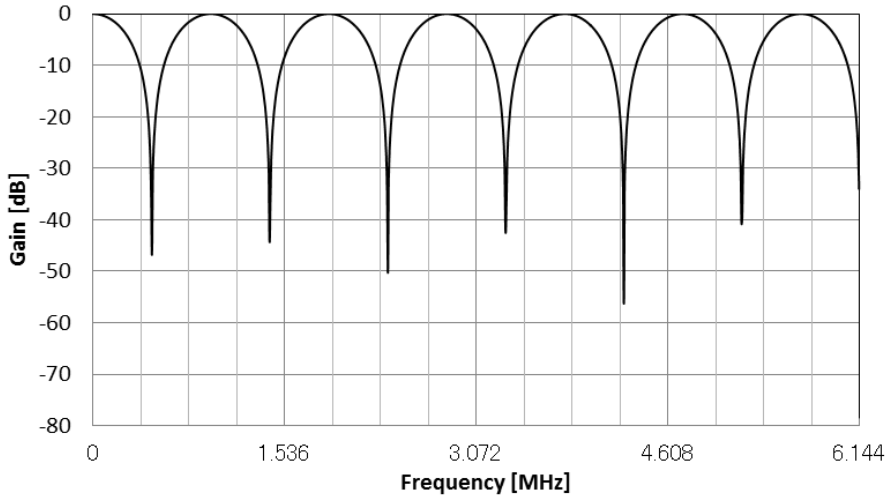


Figure 53. Mode1 FIR Filter (DSD direct mode)

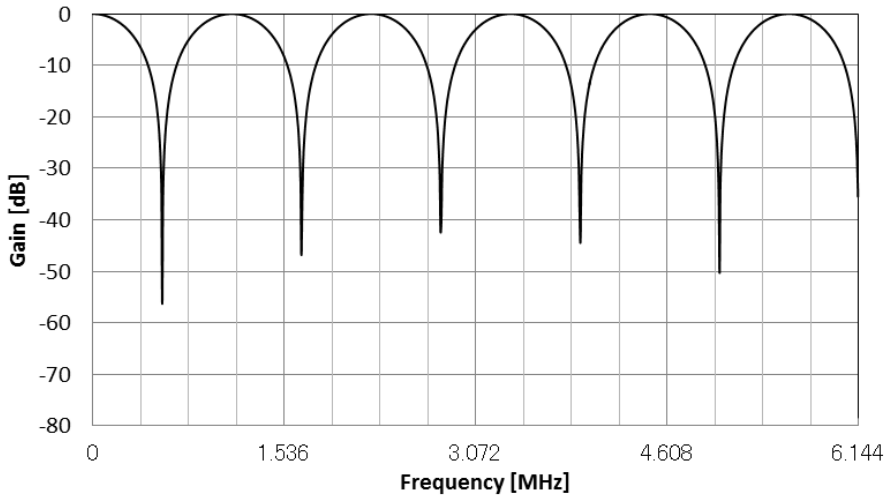


Figure 54. Mode2 FIR Filter (DSD direct mode)

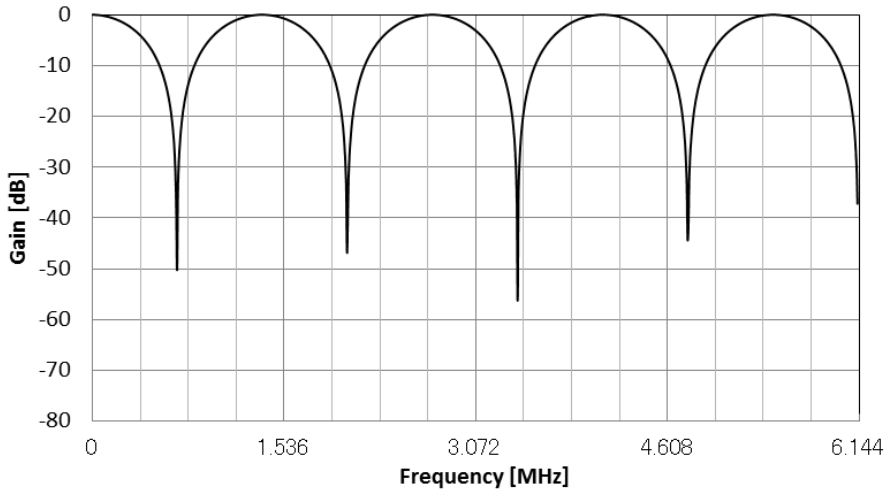


Figure 55. Mode3 FIR Filter (DSD direct mode)

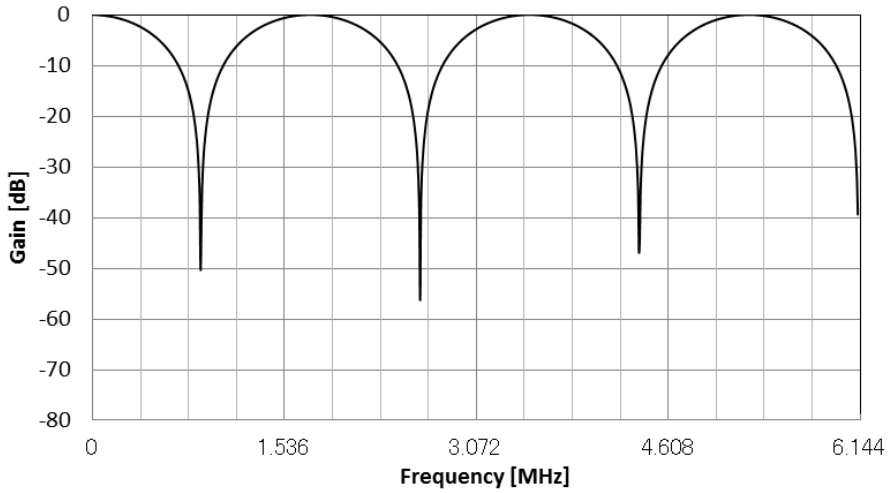


Figure 56. Mode4 FIR Filter (DSD direct mode)

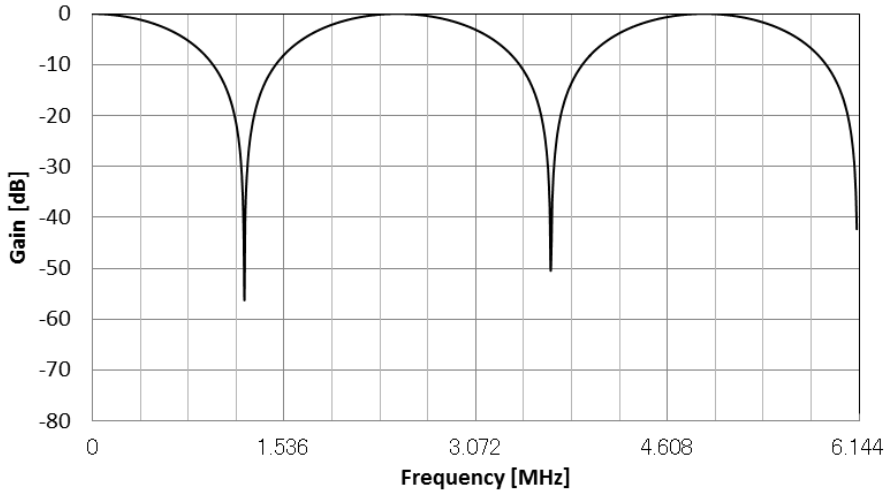


Figure 57. Mode5 FIR Filter (DSD direct mode)

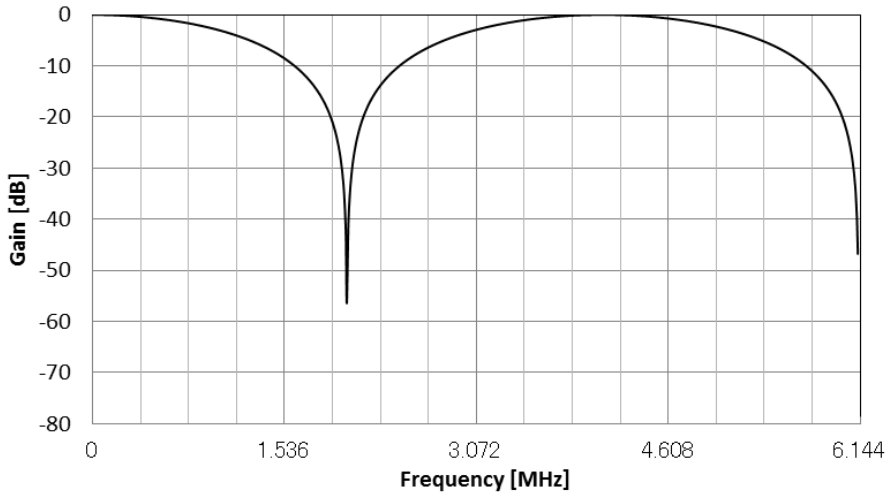


Figure 58. Mode6 FIR Filter (DSD direct mode)

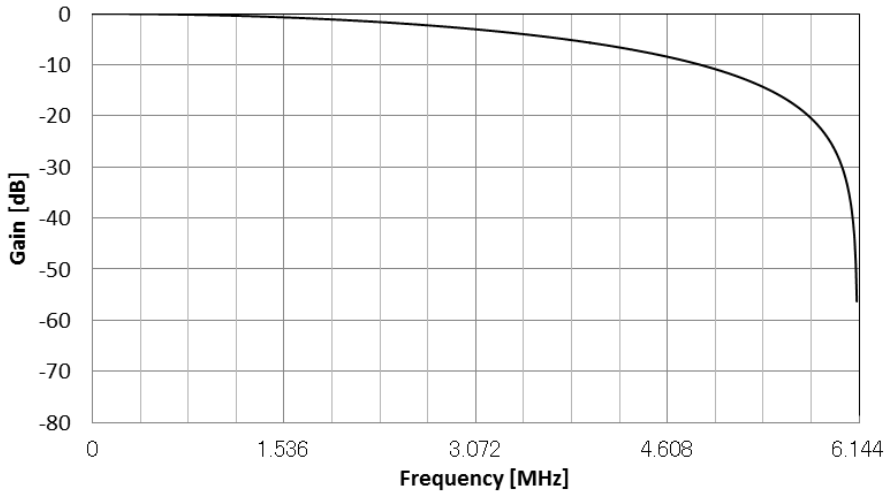


Figure 59. Mode7 FIR Filter (Except DSD direct mode)

■ Zero Detection (PCM mode, DSD mode)

When zero detection function is enabled, the DZF pin goes to "H" if the input data at each channel is continuously zeros for 8192 LRCK cycles. Zero detection channels (AOUTL1N/P and AOUTR1N/P pins) can be selected by 08H registers (L1 bit, R1 bit). The DZF pin immediately returns to "L" if the input data of each channel is not zero. If the RSTN bit is "0", the DZF pins of both channels go to "H". The DZF pin of both channels go to "L" after 4 ~ 5/fs when RSTN bit returns to "1". The DZFB bit can invert the polarity of the DZF pin. If all channels are disabled, the DZF pin outputs "Not zero". Zero detection function is disabled when DSDD bit = "1".

DZFB bit	Data	DZF pin
0	Not zero	L
	Zero detect	H
1	Not zero	H
	Zero detect	L

Not zero: One of the zero detection channels set by L1 bit and R1 bit does not detect zero.
Zero detect: All zero detection channels set by L1 bit and R1 bit detect zero.

Table 20. DZF Pin Function

■ LR Channel Output Signal Select (PCM mode, DSD mode)

Select output signal combination of L and R channels by this function.
Input and output signal combination of the AK4452 can be set by MONO1 bit and SELLR1 bit. The output signal phase of DAC is controlled by INVL and INVR bits. With these settings, sixteen output signal combinations are available. These settings are available for any audio format.

MONO1 bit	SELLR1 bit	INVL1 bit	INVR1 bit	L1ch Out	R1ch Out
0	0	0	0	L1ch In	R1ch In
		1	0	L1ch In Invert	R1ch In
		0	1	L1ch In	R1ch In Invert
		1	1	L1ch In Invert	R1ch In Invert
0	1	0	0	R1ch In	L1ch In
		1	0	R1ch In Invert	L1ch In
		0	1	R1ch In	L1ch In Invert
		1	1	R1ch In Invert	L1ch In Invert
1	0	0	0	L1ch In	L1ch In
		1	0	L1ch In Invert	L1ch In
		0	1	L1ch In	L1ch In Invert
		1	1	L1ch In Invert	L1ch In Invert
1	1	0	0	R1ch In	R1ch In
		1	0	R1ch In Invert	R1ch In
		0	1	R1ch In	R1ch In Invert
		1	1	R1ch In Invert	R1ch In Invert

Table 21. Output Select for DAC

■ Sound Quality Adjustment (PCM mode, DSD mode)

The sound quality of the AK4452 can be controlled by SC1-0 bits. The analog characteristics are guaranteed when Setting 1. However, they are not guaranteed in Setting 2 and 3.

SC1	SC0	Sound Mode	
0	0	Analog internal current, normal (Setting1)	(default)
0	1	Analog internal current, maximum (Setting2)	
1	0	Analog internal current, minimum (Setting3)	
1	1	Reserved	

Table 22. Sound Quality Select Mode

■ DSD Full Scale (FS) Signal Detection Function

The AK4452 has a full scale signal detection function for each channel in DSD mode. When the input data of each channel (DSDL1, DSDR1) is continuously "0" (-FS) or "1" (+FS) for 2048 cycles, the AK4452 detects a full scale signal and outputs "1" on the DML1 and DMR1 bits. The output data is muted if a full scale signal is detected. When DSDD bit = "0", the output data is changed in soft transition, and the output data is changed without soft transition when DSDD bit = "1". A recovering condition to normal operation mode from full scale detection status is selected by DMC bit if DDM bit = "1".

When DMC bit = "0", the AK4452 will return to normal operation automatically by inputting a normal signal. When DMC bit = "1", the AK4452 will return to normal operation mode by writing "1" to DMRE bit.

DSDD bit	Mode	Status after Detection	
0	Normal path	DSD Mute	(default)
1	Volume pass	PD	

Table 23. DSD Mode and The Device Status after Full Scale Detection (DDM bit= "0")

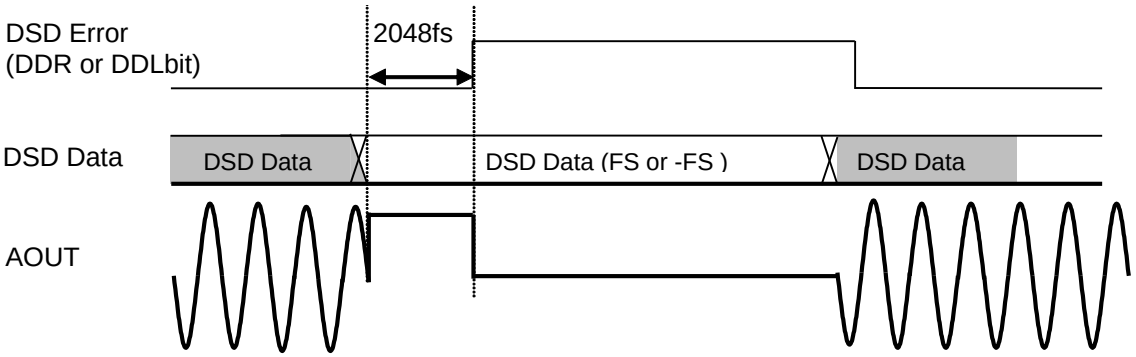


Figure 60. Analog Output Waveform when DSD FS is Detected (DSDD bit= "1")

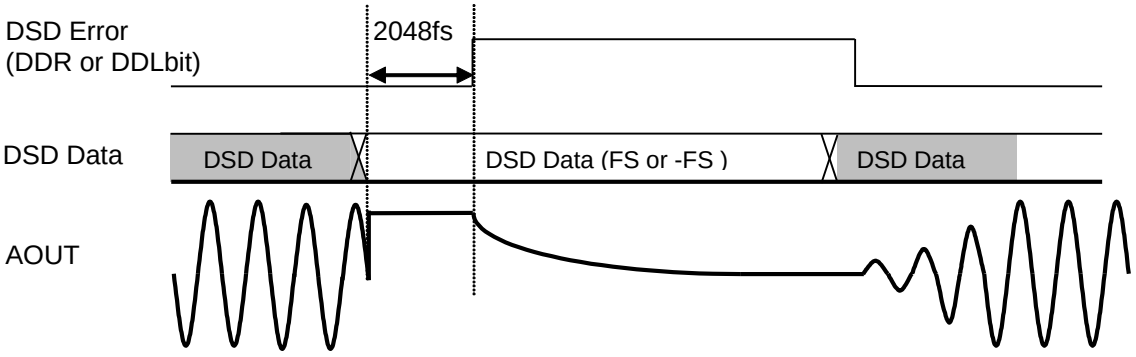
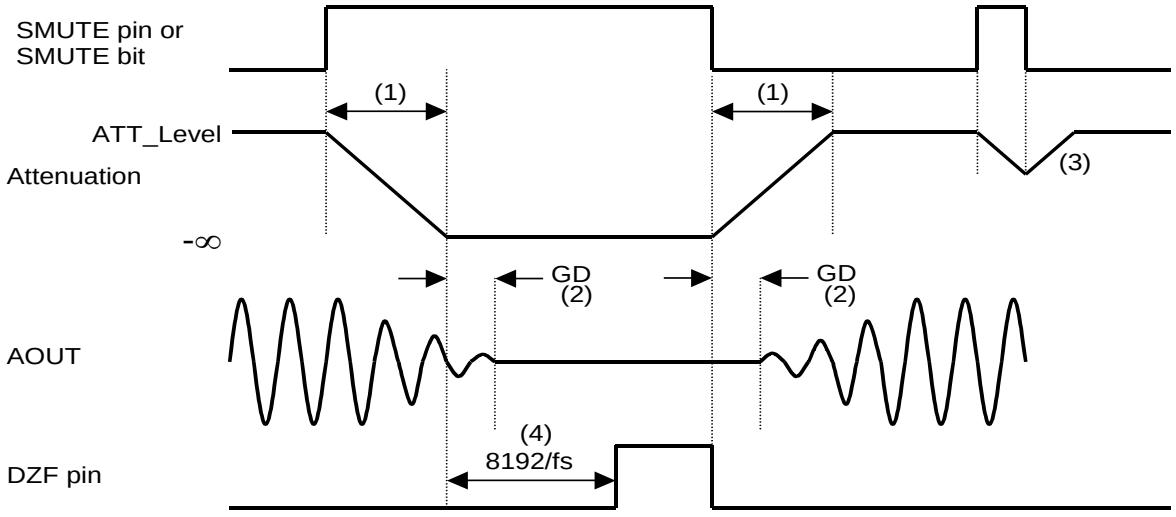


Figure 61. Analog Output Waveform when DSD FS is Detected (DSDD bit= "0")

■ Soft Mute Operation (PCM mode, DSD mode)

The soft mute operation is performed at digital domain. When the SMUTE pin goes to "H" or set SMUTE bit to "1", the output signal is attenuated by −∞ during ATT_DATA × ATT transition time from the current ATT level. When the SMUTE pin is returned to "L" or the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating −∞, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time. For example, this time is 4080LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.

(2) The analog output corresponding to the digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data for a zero detection channel is continuously zeros for 8192 LRCK cycles, the DZF pin goes to "H". The DZF pin immediately returns to "L" if input data are not zero.

Figure 62. Soft Mute Function

■ Error Detection

Three types of error can be detected in I^{2}C mode when the LDOE pin = "H". (Table 24) When the error is detected, all circuits are powered-down and the analog outputs become floating (Hi-Z) state. In I2C mode, the AK4452 does not generate acknowledge (ACK) in error status. Once the error is detected the AK4452 does not return to normal operation automatically even if the error condition is removed so restart the AK4452 by the PDN pin.

No	Error	Error Condition
1	Internal Reference Voltage Error	Internal reference voltage is not powered up.
2	LDO Over Voltage Detection	LDO voltage > 2.2 ~ 2.5V
3	LDO Over Current Detection	LDO current < 40 ~ 110mA

Table 24. Error Detection

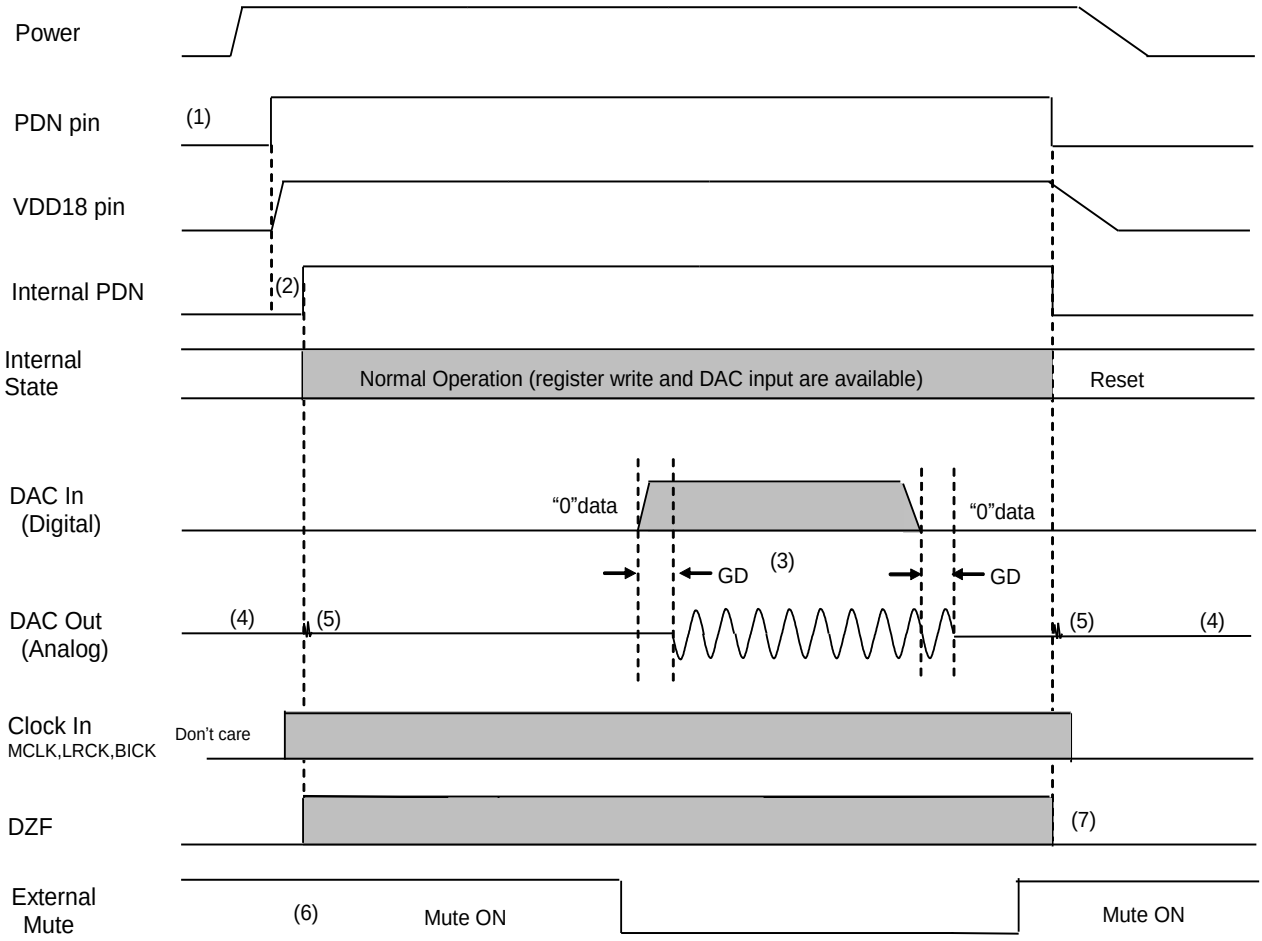
In I^{2}C mode, the AK4452 does not generate acknowledge (ACK) in error status.

■ System Reset

The AK4452should be reset once by bringing the PDN pin = "L" upon power-up. In PCM (DSD) mode, the AK4452 exits this system reset (power-down mode) by MCLK and LRCK (DCLK) after the PDN pin = "H". The AK4452 detects a rising edge of MCLK first, and then the analog block exits power-down mode by a rising edge of LRCK (DCLK). The digital block exits power-down mode after the internal counter counts MCLK for 4/fs.

■ Power Down Function

The AK4452 is placed in power-down mode by bringing the PDN pin "L" and the analog outputs become floating (Hi-Z) state. Power-up and power-down timings are shown in Figure 63.



Notes:

(1) After AVDD and TVDD are powered-up, the PDN pin should be "L" for 150ns.

(2) After PDN pin = "H", the internal LDO power-up if the LDOE pin = "H". The internal circuits will be powered up after shutdown switch is ON in the end of a counter by the internal oscillator (10ms(max)). If the LDOE pin = "L", the shutdown switch is activated after the AK4452 is powered up. The internal circuits will be powered up in 1msec (max) after the activation of the shutdown switch.
During this period, digital output and digital in/output pins may output an instantaneous pulse (max. 1us). Therefore, referring the output of digital pins and data transmission with a device on the same 3-wire serial/I^2C bus as the AK4452 should be avoided in this period to prevent system errors.

(3) The analog output corresponding to digital input has group delay (GD).

(4) Analog outputs are floating (Hi-Z) in power down mode.

(5) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.

(6) Mute the analog output externally if click noise (5) adversely affect system performance
The timing example is shown in this figure.

(7) The DZF pin is "L" in the internal power-down mode.

Figure 63. Power down/up Sequence Example

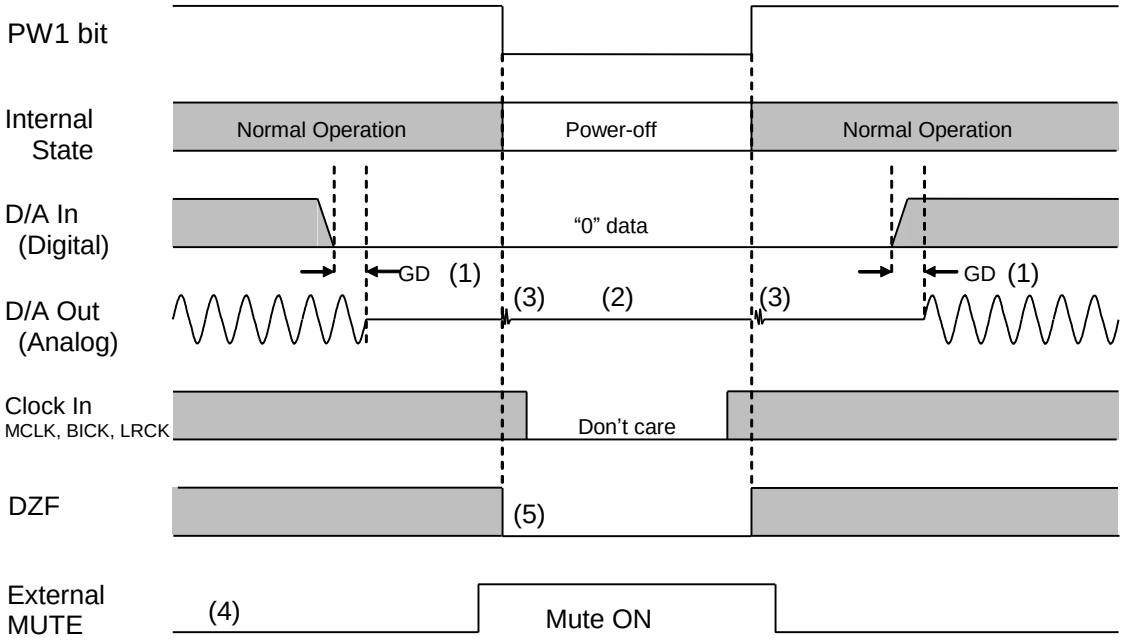
■ Power Off and Reset Functions

RSTN	PW1	DAC	Register	Digital	Analog Output DAC
1	0	OFF	Hold	Off	Hi-Z
1	1	ON	Hold	On	normal
0	0	OFF	Hold	Off	Hi-Z
0	1	ON	Hold	Off	VREFH/2

Table 25. Power Off and Reset Function

(1) Power OFF Function 1 (PW1 bit)

The DAC can be powered down immediately by setting PW1 bit to "0". In this time, all circuits except registers are powered down and the analog output goes to floating state (Hi-z). Figure 64 shows a timing example of power-on and power-down.



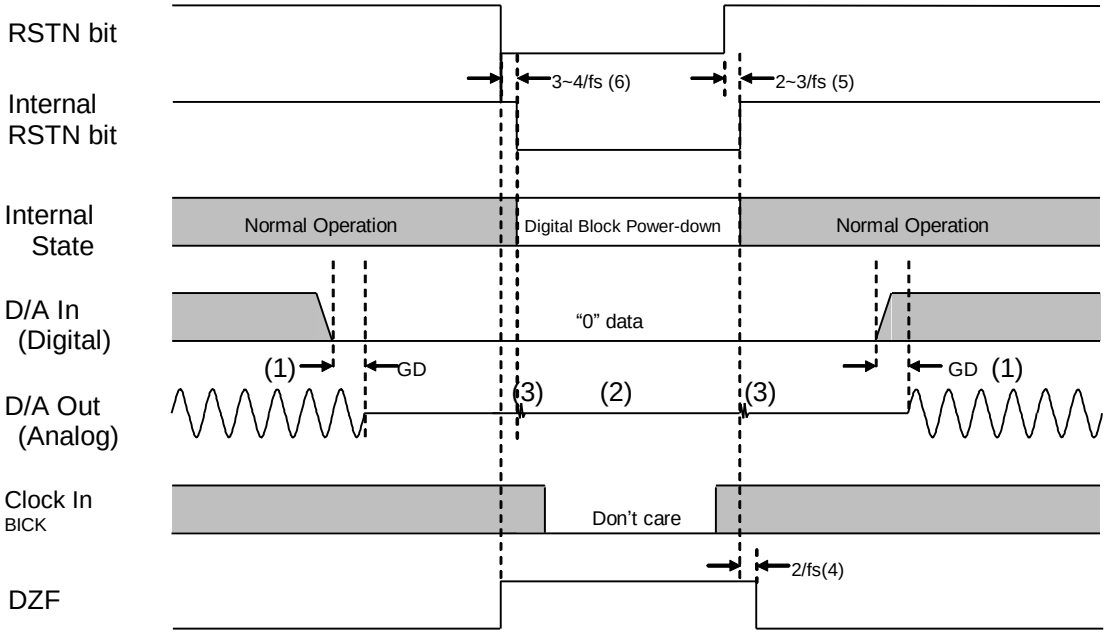
Notes:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs are floating (Hi-Z) in power down mode.
(3) Small pop noise occurs at the edges("↑ ↓") of the internal timing of PW1 bit. This noise is output even if "0" data is input.
(4) Mute the analog output externally if click noise (3) adversely affect system performance.
(5) The DZF pin outputs "L", in power down mode (PW1 bit = "0").

Figure 64. Power-off/on Sequence Example

(2) Reset Function (RSTN bit)

The DAC can be reset by setting RSTN bit to "0" but the internal registers are not initialized. In this time, the corresponding analog outputs go to VREFH/2 and the DZF pin outputs "H" if clocks (MCLK, BICK and LRCK) are input. Figure 65 shows an example of reset sequence by RSTN bit.



Notes:

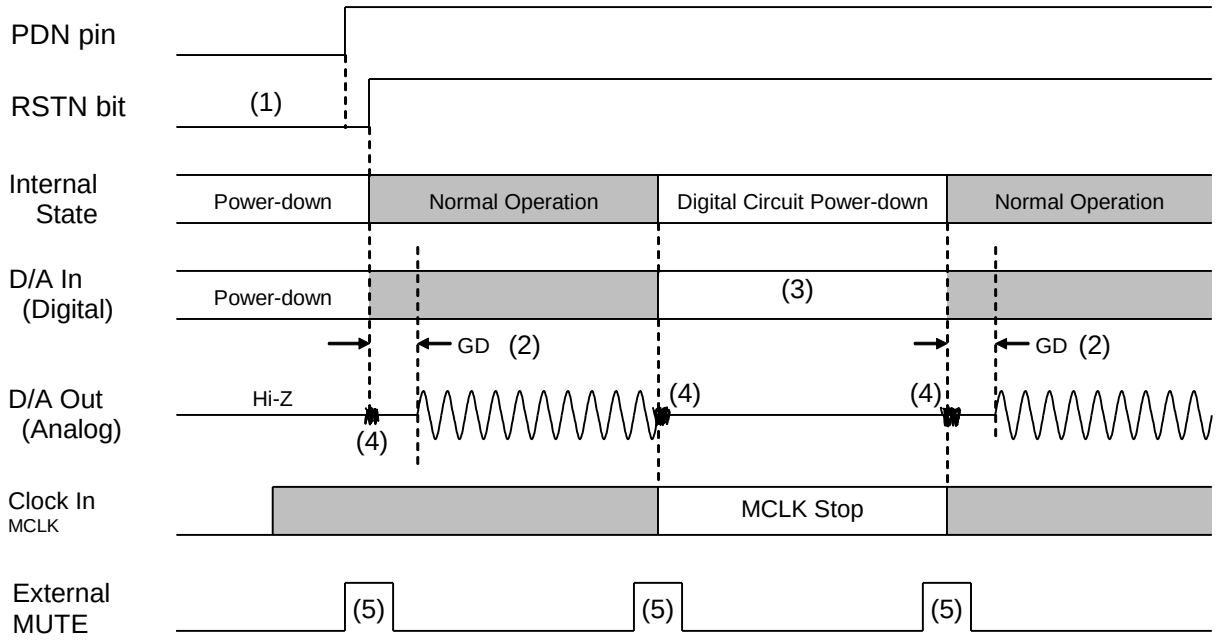
(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs are floating (Hi-Z) in power down mode.
(3) Small pop noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The DZF pin goes to "H" on the falling edge of RSTN bit and goes to "L" in 2/fs after a rising edge of the internal RSTN.
(5) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN bit "1".

Figure 65. Reset Sequence Example 1

Note: When using both reset (RSTN bit = "0") and DAC power-off bits (PW1 bit), power-off bits should be set to "0" before RSTN bit.

(3) Reset Function (MCLK Stop)

When the MCLK stops for more than 10us during operation (PDN pin = "H"), the AK4452 is placed in reset state and the analog output goes to floating state (Hi-Z). When the MCLK is restarted, reset state is released and the AK4452 returns to normal operation mode. Zero detection function is disabled while the MCLK is stopped. Figure 66 shows a reset sequence by stopping the MCLK.



Notes:

(1) After the AK4452 is powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) The digital data input can be stopped. Click noise after MCLK is input again can be reduced by inputting "0" data during this period.
(4) Click noise occurs within 3 ~ 4LRCK from the riding edge ("↑") of the PDN pin or MCLK inputs. This noise is output even if "0" data is input.
(5) Mute the analog output externally if click noise (4) adversely affect system performance.

Figure 66. Reset Sequence Example 2

■ Clock Synchronization and BICK Edge Detection Functions

● Synchronization Function (Analog Output Phase Synchronization)
This function synchronizes analog output phase by suppressing the phase difference of the AK4452 and other AKM devices with synchronization function to within 3/256fs. Analog output phase synchronization function becomes valid when input data at all channels are continuously “0” for 8192 times if SYNCE bit is set to “1” during operation in PCM mode or when RSTN bit is set to “0”.

Example) In the case of using the AK4452 with the AK4458 (Figure 67)

The AK4452 and the AK4458 have synchronization function. The output phase difference between the AK4452’s output (AOUT1LP/N_2, AOUT1RP/N_2) and the AK4458’s output (AOUT1-4LP/N_8, AOUT1-4RP/N_8) will be within 3/256fs.

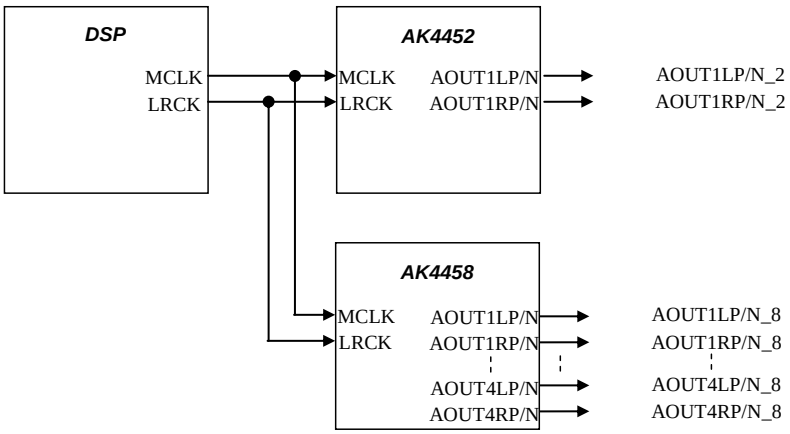


Figure 67. System Example of Clock Synchronization Function

■ Parallel Mode

Parallel mode is available by setting the I2C pin = "H", and the PS pin = "H". Audio interface format of the parallel mode is controlled by TDM1-0 pins and DIF pin (Table 26). Daisy Chain mode is also available by setting the DCHAIN pin = "H". In parallel mode, the clock setting mode is always in auto setting mode (ACKS mode is enabled and fixed internally).

Zero detection function is not available in parallel mode. All functions controlled exclusively by Serial mode are only available in their default register settings.

TDM1 pin	TDM0 pin	DIF pin	Mode
0	0	0	Mode6 (Table 13)
0	0	1	Mode7 (Table 13)
0	1	0	Mode12 (Table 13)
0	1	1	Mode13 (Table 13)
1	0	0	Mode18 (Table 13)
1	0	1	Mode19 (Table 13)
1	1	0	Mode24 (Table 13)
1	1	1	Mode25 (Table 13)

Table 26. Parallel Mode

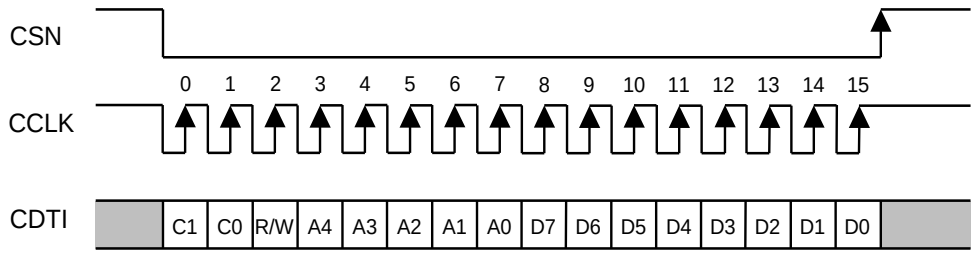
■ Serial Control Interface

The AK4452's functions are controlled through registers. The registers may be written by two types of control modes. The internal registers are controlled in 3-wire serial control mode when the I2C pin = "L", and in I^2C bus control mode when the I2C pin = "H" and the PS pin = "L".

(1) 3-wire Serial Control Mode (I2C pin = "L")

The internal registers may be written through the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address, Read/Write (1bit, Fixed to "1", Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz (max).

The internal registers are initialized by setting the PDN pin = "L". In serial mode, an internal timing circuit is reset by setting RSTN bit = "0" but register values are not initialized.



C1-C0: Chip Address (C1= CAD1 pin, C0= CAD0 pin)
R/W: Read/Write (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 68. 3-wire Serial Control I/F Timing

* The AK4452 does not support read commands in 3wire serial control mode.
* When the AK4452 is in power down mode (PDN pin = "L"), writing into the control registers is prohibited.
* The control data cannot be written when the CCLK rising edge is 15 times or less or 17 times or more during CSN is "L".

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4452 supports the fast-mode I²C-bus (max: 400kHz, Ver1.0).

1. WRITE Operations

Figure 69 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 75). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1-0 (device address bits). This bits identifies the specific device on the bus. The hard-wired input pins (CAD1-0 pins) set these device address bit (Figure 70). If the slave address matches that of the AK4452, the AK4452 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 76). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4452. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 71). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 72). The AK4452 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 75).

The AK4452 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4452 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 14H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 77) except for the START and STOP conditions.

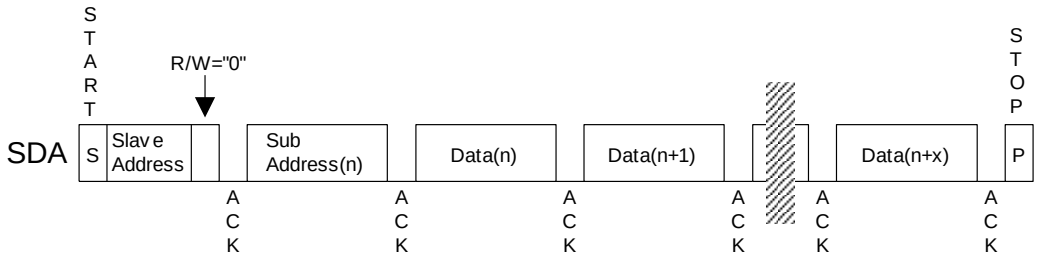


Figure 69. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(These CAD1-0 should match with CAD1-0 pins)

Figure 70. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 71. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 72. Byte Structure After The Second Byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4452. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 14H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4452 supports two basic read operations: Current Address Read and Random Address Read.

2-1. Current Address Read

The AK4452 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4452 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4452 ceases transmission.

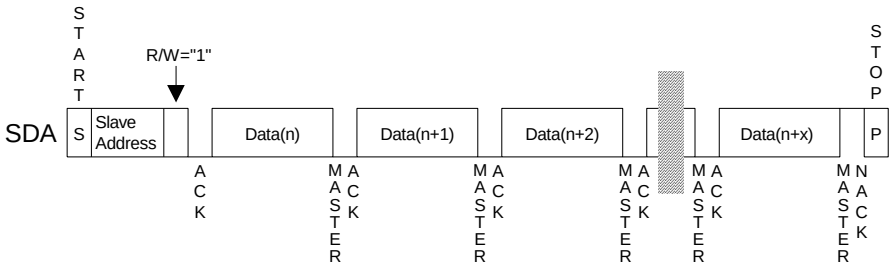


Figure 73. Current Address Read

2-2. Random Address Read

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4452 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4452 ceases transmission.

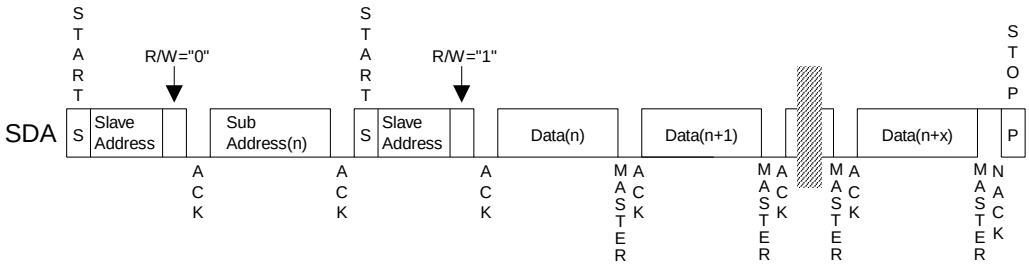


Figure 74. Random Address Read

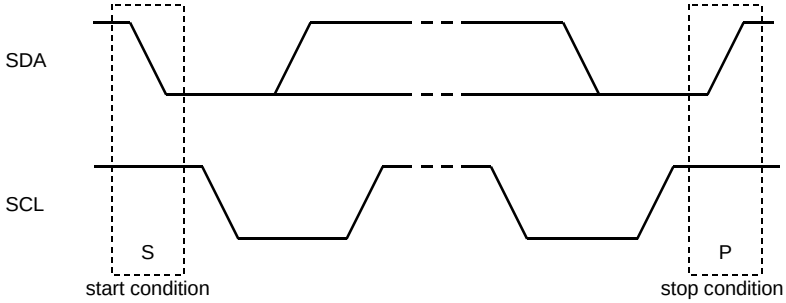


Figure 75. START and STOP Conditions

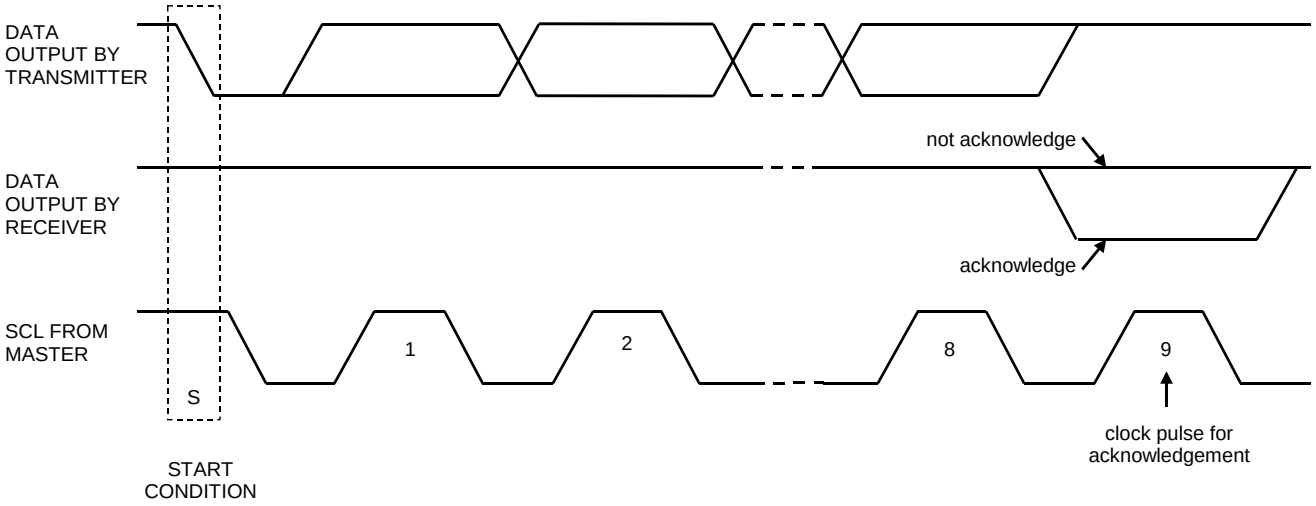


Figure 76. Acknowledge on the I^2C-Bus

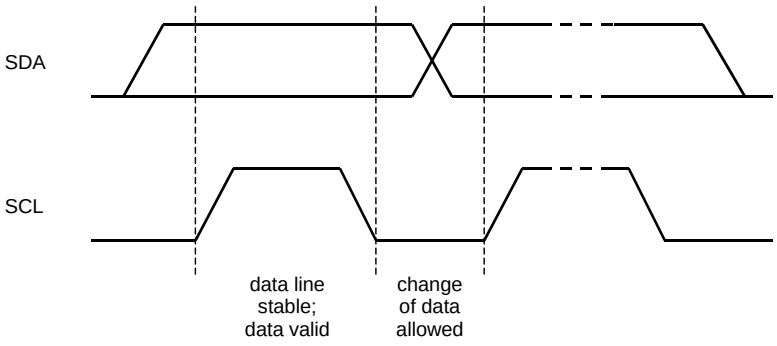


Figure 77. Bit Transfer on the I^2C-Bus

■ Function List

Available functions are different in PCM mode and in DSD mode.

Function	Default	Address	Bit	PCM	DSD
Attenuation Level	0dB	03-04H	ATT7-0	Y	Y
Audio Data Interface Modes	32bit MSB justified	00H	DIF2-0	Y	-
Data Zero Detect Enable	Disable	08H	L1/R1	Y	Y
Minimum delay Filter Enable	Sharp roll-off filter	01-02H	SD	Y	-
Slow Roll-off Filter Enable			SLOW	Y	-
Short delay Filter Enable				Y	-
De-emphasis Response	OFF	01H	DEM1-0	Y	-
Soft Mute Enable	Normal Operation	01H	SMUTE	Y	Y
DSD/PCM Mode Select	PCM mode	02H	D/P	Y	Y
Master Clock Frequency Select at DSD mode	512fs	02H	DCKS	-	Y
MONO mode Stereo mode select	Stereo	02H	MONO	Y	Y
Inverting Enable of DZF	"H" active	02H	DZFB	Y	Y
The data selection of L channel and R channel	R channel	02H,05H 0DH	SELLR1	Y	Y
The data selection of DAC	Normal	0A-0BH	SDS1/2	Y	-
Data Invert Mode	OFF	05H	INVL1/R1	Y	Y
Clock Synchronization	Enable	07H	SYNCE	Y	-

Table 27. Function List (Y: Available, -: Not available)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	0	0	0	0	DFS2	SSLOW
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL0
07H	Control 5	0	0	0	0	0	0	1	SYNCE
08H	Sound Control	L1	R1	0	0	0	0	SC1	SC0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	1	PW1	0	1
0BH	Control 7	ATS1	ATS0	0	SDS0	1	1	DCHAIN	0
0CH	Control 8	0	0	0	0	0	FIR2	FIR1	FIR0
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	1	0	1	0	0	0	0
0FH	Reserved	1	1	1	1	1	1	1	1
10H	Reserved	1	1	1	1	1	1	1	1

Note 34. Data must not be written into addresses from 11H to 1FH.

Note 35. When the PDN pin is set to “L”, all registers are initialized to their default values.

Note 36. When RSTN bit is set to “0”, only the internal timing circuit is reset but register values are not initialized.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF2	DIF1	DIF0	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

RSTN: Internal Timing Reset
0: Reset (default)
Internal clock timings are reset, but all other registers are not reset to their default value and R/W access is still allowed.
1: Normal Operation

DIF2-0: Audio Data Interface Modes (Table 13)
Default value is “110” (Mode 6: 32-bit MSB justified).

ACKS: Master Clock Frequency Auto Setting Mode Enable (PCM only)
0: Disable : Manual Setting Mode (default)
1: Enable : Auto Setting Mode
When ACKS bit = “1”, the sampling frequency and MCLK frequency are detected automatically.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	SD	DFS1	DFS0	DEM11	DEM10	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	1	0

SMUTE: Soft Mute Enable.
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM11-0: DAC1 De-emphasis Response (Table 16)
Default value is “01” (OFF).

DFS1-0: Sampling Speed Control (Table 2)
Default value is “00” (Normal Speed). See also register address 05H for DFS2.
A click noise occurs when switching DFS2-0 bits setting.

SD: Short delay Filter Enable. (Table 12)
0: Sharp roll-off filter
1: Short delay filter (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	DP	0	DCKS	DCKB	MONO1	DZFB	SELLR1	SLOW
R/W		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SLOW: Slow Roll-off Filter Enable. (Table 12)
0: Sharp roll-off filter (default)
1: Slow roll-off filter

SELLR1: The data selection of DAC1 L channel and R channel, when MONO mode (Table 21)
0: All channel output L channel data. (default)
1: All channel output R channel data.
Settings of MONO1 bit, INVL1 bit and INVR1 bit should also be considered when setting this bit.

DZFB: Inverting Enable of DZF (Table 20)
0: DZF pin goes "H" at Zero Detection (default)
1: DZF pin goes "L" at Zero Detection

MONO1: DAC1 enters monaural output mode when MONO bit = "1". (Table 21)
0: Stereo mode (default)
1: MONO mode

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge. (default)
1: DSD data is output from DCLK rising edge.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs (default)
1: 768fs

DP: DSD/PCM Mode Select
0: PCM Mode (default)
1: DSD Mode
The AK4452 must be reset by RSTN bit when changing DP bit setting.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level (Table 17)
Initial value is "FF" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Control 4	INVL1	INVR1	0	0	0	0	DFS2	SSLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SSLOW: Digital Filter Bypass Mode Enable (Table 15)
0: Enable digital filter selected by SD and SLOW bits (default)
1: Super Slow Roll-off Mode

DFS2: Sampling Speed Control (Table 2)
Default value is "0" (Normal Speed). See also register address 01H for DFS1-0.
A click noise occurs when switching DFS2-0 bits setting.

INVL1: AOUTL1 Output Phase Inverting Bit
INVR1: AOUTR1 Output Phase Inverting Bit
0: Normal (default)
1: Inverted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL1-0: DSD sampling speed control (Table 10)
Default value is “00”.

DSDD: DSD play back path control (Table 11)
Default value is “0”.

DMRE: DSD mute release
0: Hold (default)
1: Mute Release
This register is only valid when DDM bit = “1” and DMC bit = “1”. It releases a mute state when DSD data is muted by DDM and DMC bits.

DMC: DSD mute control
0: Auto Return (default)
1: Mute Hold
This register is only valid when DDM bit = “1”. It selects the process when DSD data level drops under full scale while DSD data is muted by DDM bit.

DMR1/DML1
This register output detection flag when the signal level of the DSDR1/L1 pin is full scale.

DDM: DSD data mute
0: Disable (default)
1: Enable
The AK4452 has a function that mutes the output when DSD data is all “1” or “0” for 2048 samplings (1/fs). This register controls the DSD mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Control 5	0	0	0	0	0	0	1	SYNCE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

SYNCE: SYNC Mode Enable
0: SYNC Mode Disable
1: SYNC Mode Enable (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Sound Control	L1	R1	0	0	0	0	SC1	SC0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SC1-0: Sound Control (Table 22)
Default value is “00”.

L1, R1: Zero Detect Flag Enable Bit for the DZF pin
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DSDSEL1-0: DSD Sampling Speed Control (Table 10)
Default value is "00".

DSDF: DSD Filter Select (Table 12)
Default value is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 6	TDM1	TDM0	SDS1	SDS2	1	PW1	0	1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

PW1: Power Down control for DAC
PW1: Power management for DAC
0: DAC power OFF
1: DAC power ON (default)

SDS2-0: DAC Data Select
0: Normal Operation
1: Output Other Slot Data (Table 14)
Default value is "000".

TDM1-0: TDM Mode Select (Table 13)
Default value is "00".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Control 7	ATS1	ATS0	0	SDS0	1	1	DCHAIN	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	0

DCHAIN: Daisy Chain Mode Enable
0: Daisy Chain Mode Disable (default)
1: Daisy Chain Mode Enable

SDS2-0: DAC Data Select
0: Normal Operation
1: Output Other Slot Data (Table 14)

ATS1-0: DAC Digital attenuator transition time setting (Table 18)
Default value is “00”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Control 8	0	0	0	0	0	FIR2	FIR1	FIR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

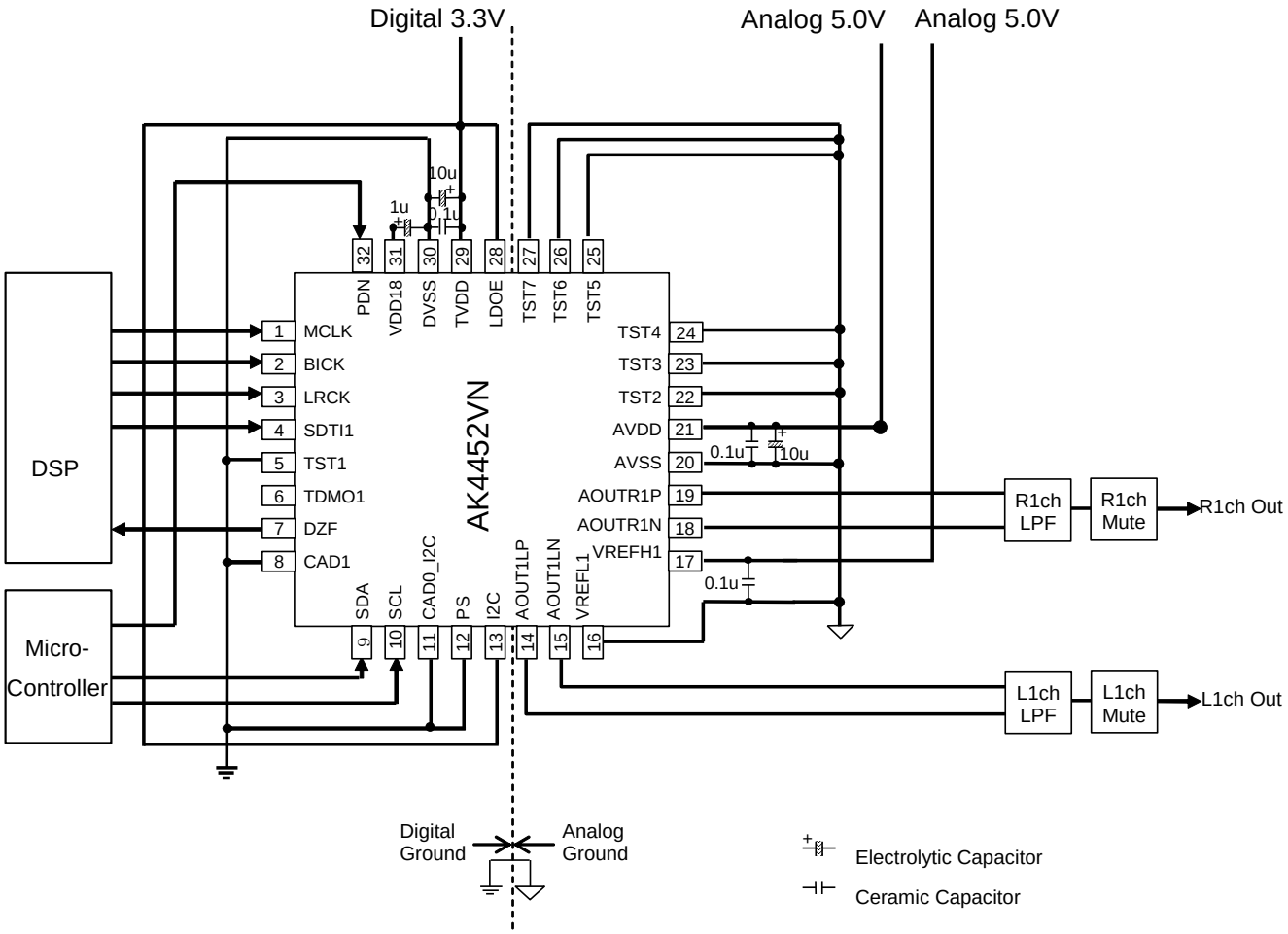
FIR2-0: FIR Filter Control (Table 19)
Default value is “000”.

10. Recommended External Circuits

■ Typical Connection Diagram

Figure 78 and Figure 79 show system connection diagram, and Figure 80 shows the analog output circuit example.

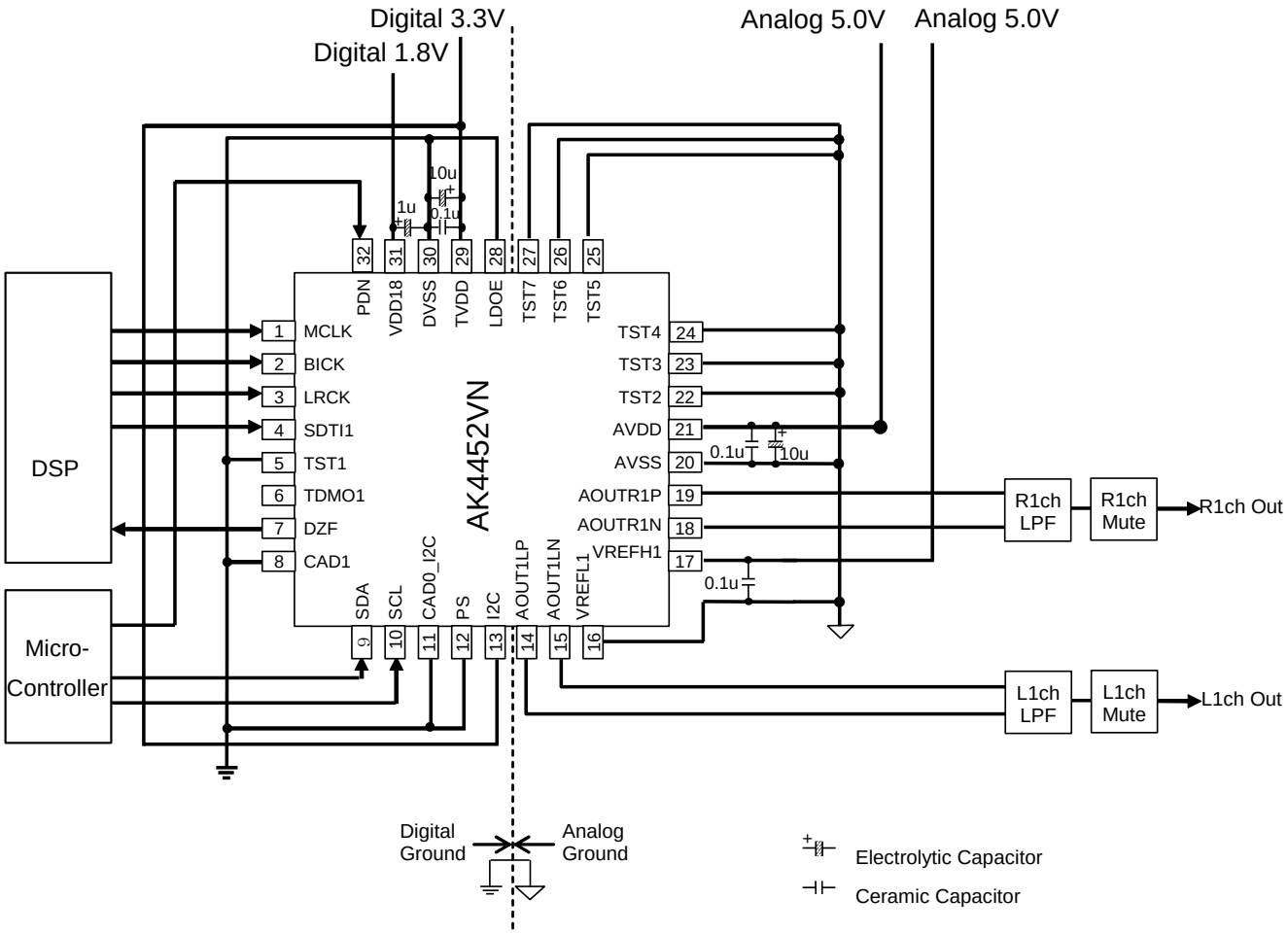
(1) LDOE pin = "H", I²C-bus Control Mode(I2C pin = "H")



Notes:
- Chip Address = "00". BICK = 64fs, LRCK = fs
- Power lines of AVDD and VREFH1 should be distributed separately from LDO and etc. while keeping low impedance. If it is not possible, it is recommended to connect a LPF composed by a 10Ω resistor and a 220uF capacitor between VREFL1 and VREFH1.
- DVSS and AVSS must be connected to the same potential.
- All digital input pins should not be allowed to float.

Figure 78. Typical Connection Diagram (AVDD=5V, TVDD=3.3V)

(2) LDOE pin = "L", I²C-bus Control Mode(I2C pin = "H")



Notes:

- Chip Address = "00". BICK = 64fs, LRCK = fs
- Power lines of AVDD and VREFH1 should be distributed separately from LDO and etc. while keeping low impedance. If it is not possible, it is recommended to connect a LPF composed by a 10Ω resistor and a 220uF capacitor between VREFL1 and VREFH1.
- DVSS and AVSS must be connected to the same potential.
- All digital input pins should not be allowed to float.

Figure 79. Typical Connection Diagram (AVDD=5V, TVDD=3.3V, VDD18=1.8V)

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and TVDD respectively. AVDD are supplied from the analog supply of the system and TVDD is supplied from the digital supply of the system. **DVSS and AVSS must be connected to the same potential.** Decoupling capacitors especially small ceramic capacitors for high frequency should be placed as near as possible to the supply pin.

2. Voltage Reference

The differential voltage between the VREFH1 pin and the VREFL1 pin sets the analog output range. The VREFH1 pin is normally connected to AVDD, and the VREFL1 pin is normally connected to AVSS. VREFH1 and VREFL1 should be connected with a 0.1µF ceramic capacitor as near as possible to the pin to eliminate the effects of high frequency noise. All signals, especially clocks, should be kept away from the VREFH1 and VREFL1 pins in order to avoid unwanted noise coupling into the AK4452.

3. Analog Outputs

The analog outputs are full differential outputs and 2.8Vpp (typ, VREFH1 – VREFL1 = 5V) centered around VREFH/2. The differential outputs are summed externally, adding voltage V_{AOUT} is calculated as (AOUT+) – (AOUT–). If the summing gain is 1, the output range is 5.6Vpp (typ, VREFH1 – VREFL1= 5V). The bias voltage of the external summing circuit is supplied externally. PCM input data format is 2's complement. The output voltage (V_{AOUT}) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H(@24bit).

The output level is determined by the 1-bit signal duty ratio in DSD input mode. The output level is positive full scale when the duty is 100% (all "1") and the output level is negative full scale when the duty is 0% (all "0"). In ideal case, a 0V voltage is output when the input signal duty is 50%.

The internal switched - capacitor filters attenuate the noise generated by the delta -sigma modulator beyond the audio pass band. Figure 80 shows an example of differential outputs and LPF circuit example by a single op-amp.

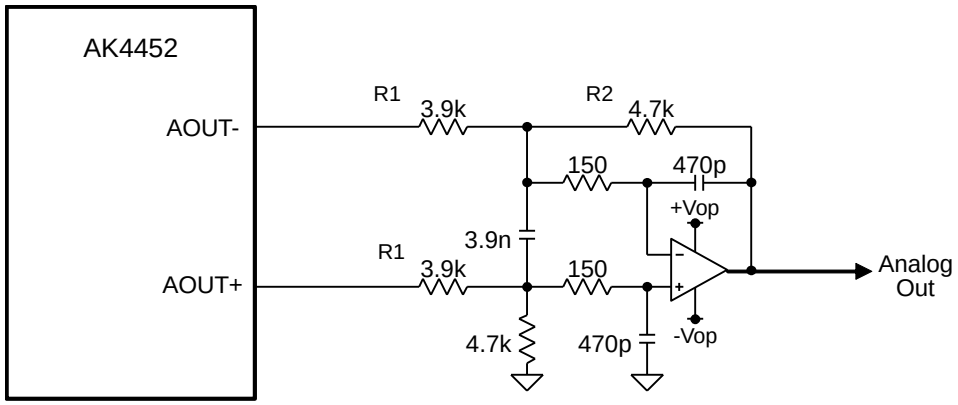


Figure 80. External LPF Circuit Example 1 for PCM (fc = 99.0kHz, Q=0.680)

R1	3.3k	3.9k	3.9k	4.3k	4.7k	5.6k
R2	3.3k	4.7k	5.6k	6.8k	8.2k	12.0k
GAIN(dB)	0	1.620665	3.142468	3.980809	4.83432	6.619864
DC Load (MAX)	3.8k	4.0k	3.5k	3.6k	3.6k	3.8k

Table 28. External LPF Circuit Example 1 for PCM

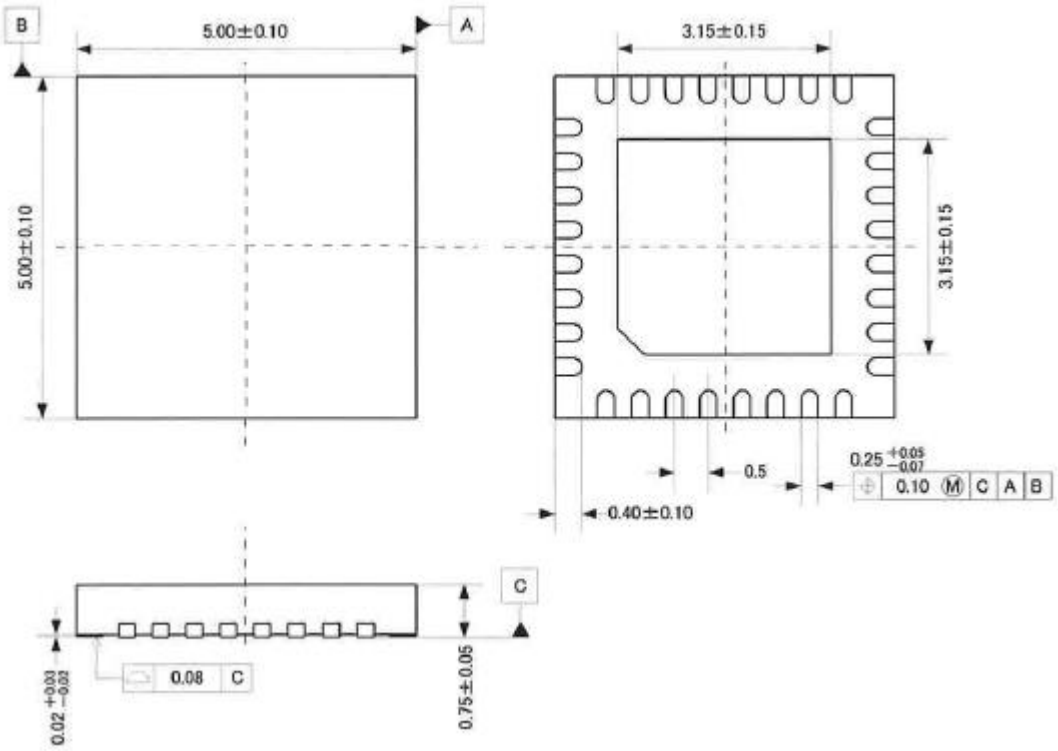
Frequency Response	Gain
20kHz	–0.036dB
40kHz	–0.225dB
80kHz	–1.855dB

Table 29. Frequency Response of External LPF Circuit Example 1 for PCM

11. Package

■ Outline Dimensions

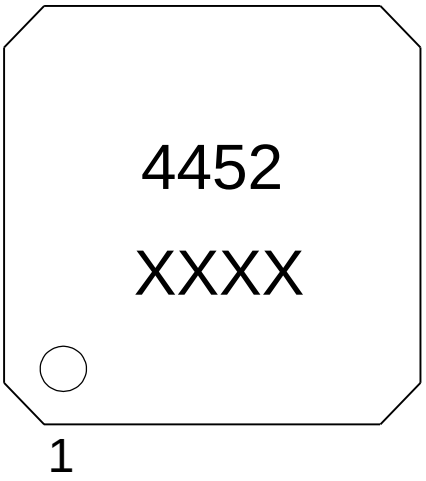
32-pin QFN (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

■ Marking



1) Pin #1 indication
2) Date Code: XXXX (4 digits)
3) Marking Code: 4452

12. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
15/02/23	00	First Edition		
15/03/21	01	Description Addition	9	■ Handling of Unused Pin TDMO1 was added.
			10	Note 7: A description was added. "at the same time"
		Error Correction	76	Figure 70 was changed.
		Description Addition	77	Figure 71 was added.
15/08/26	02	Error Correction	13, 15	Sharp Roll-Off Filter, fs=44.1kHz, DF + SCF, FR: 0 ~ 20kHz, max=0.1dB
			13, 15	Short Delay Sharp Roll-Off Filter, fs=96kHz, DF + SCF, FR: 0 ~ 40kHz, max=0.1dB
		Description Addition	13 to 16	Description of Pass band spec of -3.0dB was added.
		Description Delete	13 to 16	Frequency Response of -3.0(-6.0)dB was deleted.
		Description Addition	27	[Table 3] 384kHz, 128fs 49.152 was added.
		Description Change	53	Figure 52 and Figure 53 was changed.
		Description Addition	56	■ Power Down Function Description (2) was changed.

Date (Y/M/D)	Revision	Reason	Page	Contents
		Error Correction	62	C1-C0: Chip Address C1= CAD0 pin → CAD1 pin
			63	The most significant [remove “seven”] [add “five”] bits of the slave address
			68	Correct default value = 0 on table and description. Clarify description
17/07/11	03	Description Delete	13	Note 17 (It is the pass band gain amplitude of ⋯) was deleted.
		Description Addition	14	Figure 2 and Figure 3 were added.
			16	Figure 4 and Figure 5 were added.
			18	Figure 6 and Figure 7 were added.
			20	Figure 8 and Figure 9 were added.
			32	Table 7 was changed.
			49	■ Out of Band Noise Reduction Filter Description was changed.
			57	■ Sound Quality Adjustment Table 22 was changed

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